Isamu Arthur Poy

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Education

University of California, San Diego — San Diego, California
M.S. Computer Engineering — *Start in Fall 2021*

University of Toronto — Toronto, Ontario
B.A.Sc. Computer Engineering (with honours) — *Sep. 2017 – June 2021*

Technical Skills

Languages: Python, C/C++, Java, JavaScript, SQL, MATLAB, Verilog, System Verilog, Arm Assembly
Frameworks/Tools: ReactJS, Git, Linux, ROS, Vivado, Quartus
Libraries: PyTorch, Tensorflow, Pandas, NumPy, Bootstrap

Work Experience

FPGA Research — May 2020 – Sep. 2020
University of Toronto — *Toronto, Ontario*
- Designed FPGA debugging hardware on AXI-Lite; funded by Alibaba, Xilinx, and Fidus Systems.
- Work inspired by Microsoft Research to debug mapped streams on MPSoC FPGAs.
- Paper published to FPGA '21, and serves as the foundation for FPGA debugging on data centers.
- Successfully delivered technical presentation of work to over 150 research associates at FPGA '21.

Robotics Research — June 2019 – Aug 2019
Hong Kong University of Science and Technology — *Hong Kong*
- Developed interfaces for eye-gaze controlled robotic wheelchair in Python and Tensorflow.
- Introduced practical application of novel appearance-based eye tracking algorithm.
- Paper published to EMBC '21, a leading biomedical engineering conference.

Machine Learning Research — May 2018 – Aug 2018
Nagasaki University — *Nagasaki, Japan*
- Developed VGG16 network to detect healthy and sick trees with images collected from Nagasaki City.
- Trained model to distinguish ill trees with greater than 80% accuracy.
- Research submitted as paper for European Journal of Environmental and Civil Engineering.

Projects

H.263 Image Compression System | *Python, Verilog, FPGA* — Jan. 2021 – May 2021
- Tested an H.263 image compression hardware on Xilinx FPGAs.
- Designed serial communication between PC and FPGA for lossless data transfer.
- Tested hardware to facilitate communication between two remote FPGAs.

Debug Governors | *System Verilog, ModelSim, AXI-Lite, Git, FPGA* — May 2020 – Sep. 2020
- Designed a memory mapped interface for the Debug Governor to serve as a debugger tool for FPGAs.
- Refactored existing code to follow a datapath and controlpath structure in System Verilog.
- Paper accepted to FPGA '21, the premier conference in FPGAs, as a publication.

Dog Breed Classifier | *Python, PyTorch* — May 2020 – Aug. 2020
- Developed a dog breed image classifier for a project on Convolutional Neural Networks.
- Utilized transfer learning on existing models such as AlexNet and YOLO.
- Utilized the Stanford Dogs Data-set, and achieved testing accuracy of 90% on 11 different breeds.

Robotic Wheelchair | *Python, Tensorflow, ROS, Arduino* — June 2019 – Aug. 2019
- Developed an eye-gaze control robotic wheelchair, and used Arduino board to create user interface.
- Tested algorithms on wheelchair robot in Shenzhen, China.

Competitions

The Data Open (2021)

- Competed in Citadel's invitational summer datathon in a team of 4 remotely.
- Utilized Pandas libraries to identify second-order impacts of Airbnb rental data for the U.S South region.

Spoken Languages

Spoken Languages: English, Japanese