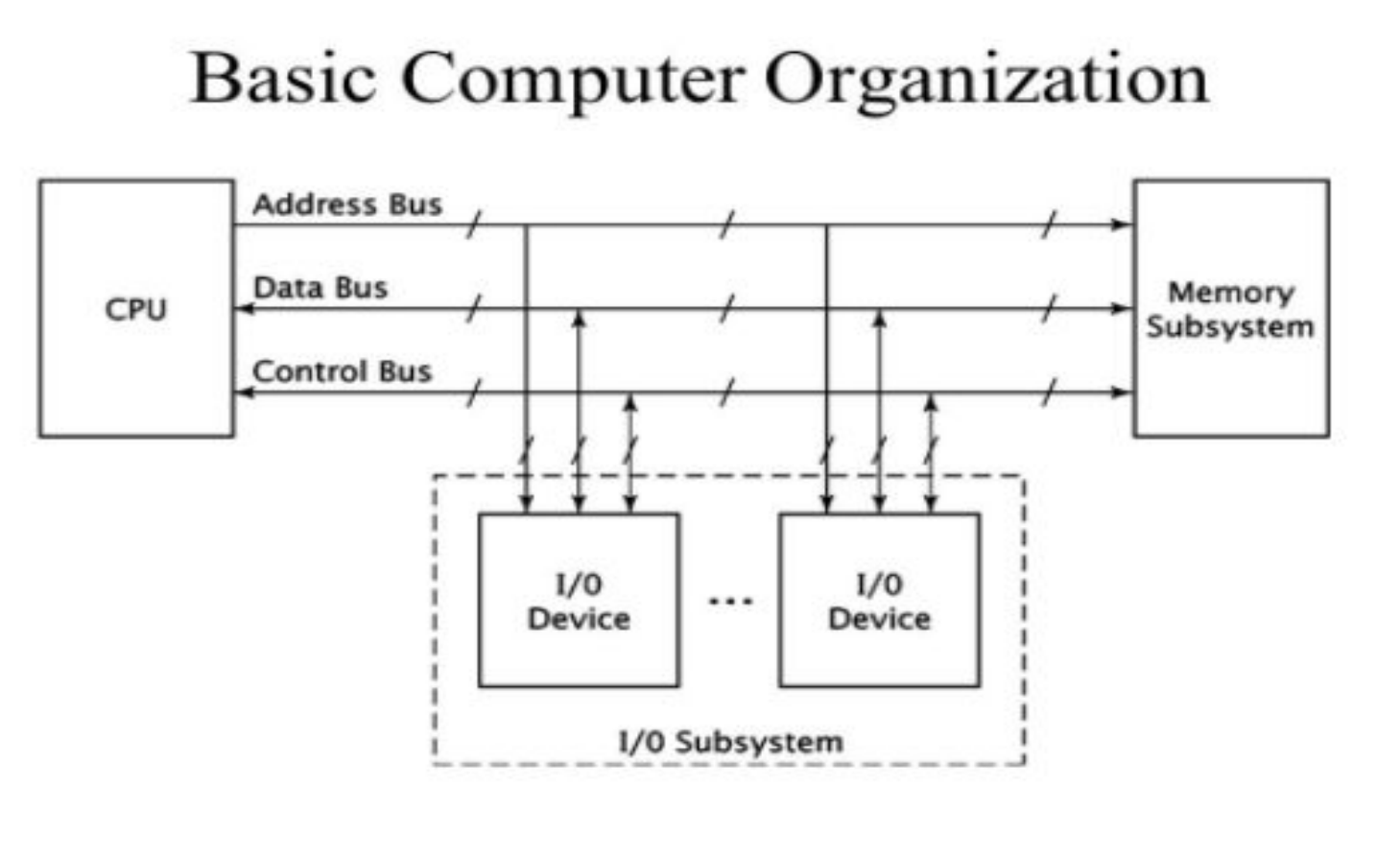
CHAPTER 2

Basic Computer Organization



Contd..

- This organization has 3 sub systems: CPU, memory sub-system and I/O sub-system.
- CPU performs various operations and controls the computer.
- Memory sub-system is used to store programs being executed by the CPU along with the necessary data.
- The I/O sub-system allows the CPU to interact with input and output devices such as keyboards, monitors, etc.

System Bus

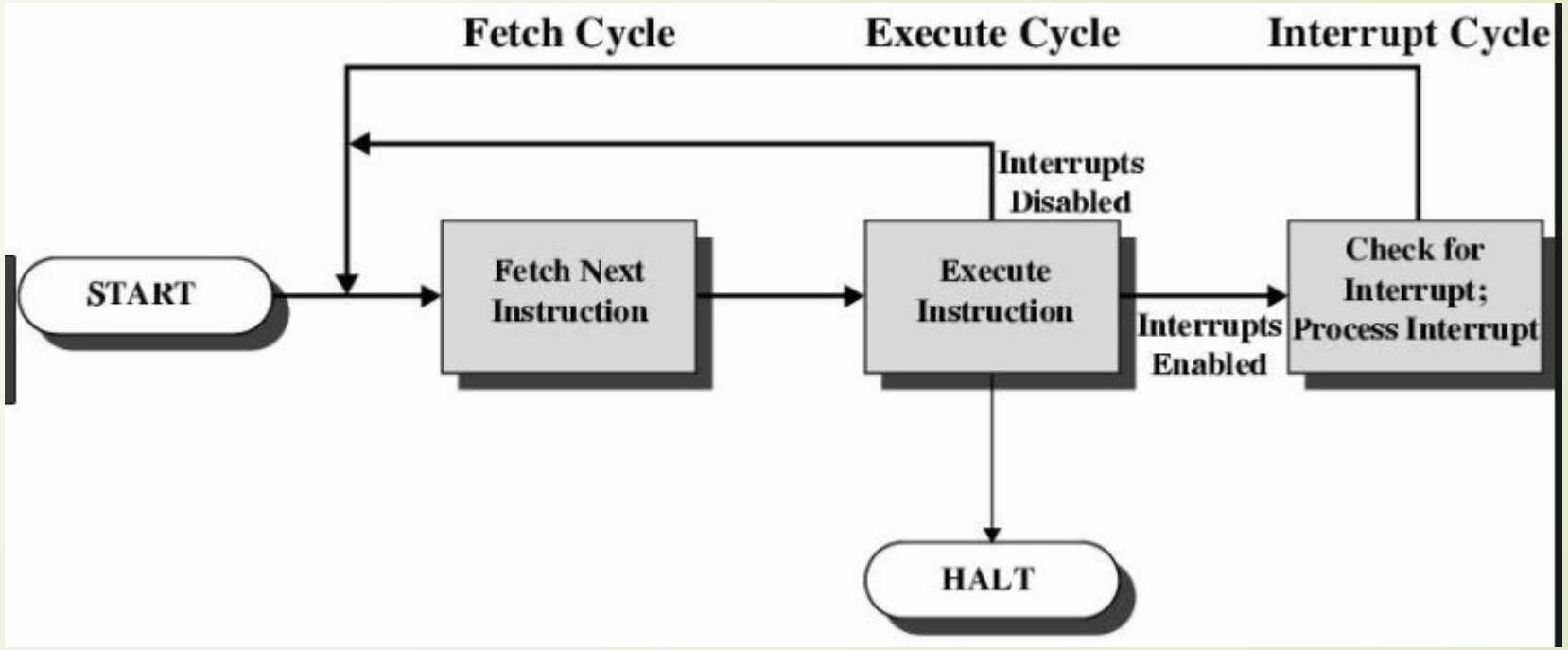
A bus is basically a collection of wires, chips and slots inside the computer through which data and signals can be transmitted to and fro between the computer and peripherals.

- Data Bus:
  =>provides path for moving data between the microprocessor and the peripherals.
  =>The data bus consists of number of separate lines, generally 8, 16, 32 or 64. The number of lines is referred to as width of data bus.
  =>Since, each line carries only 1 bit at a time, the number of lines determine how many bits can be transmitted at a time.
  =>bidirectional, **Microprocessor** can read data from memory or write data to the memory.
- Address bus:
  =>provides path for address.
  =>For eg: if the CPU requires reading a word (8, 16, 32 or 64 bits of data) from memory, it puts the address of desired word on the address bus.
  => Unidirectional because the **microprocessor** is addressing a specific memory location. No outside devices can not write into **Microprocessor.**
  => also used to address I/O ports.

Contd...

- Control bus:
  =>used to control the access and use of data and address lines.
  =>carry control and synchronization signals from CPU to peripherals and also do the same from peripherals to CPU.
  =>bidirectional
  Some of the control signals are:
  - memory read
  - memory write
  - I/O read
  - I/O write
  - bus request
  - bus grant
  - Interrupt request
  - Interrupt acknowledge

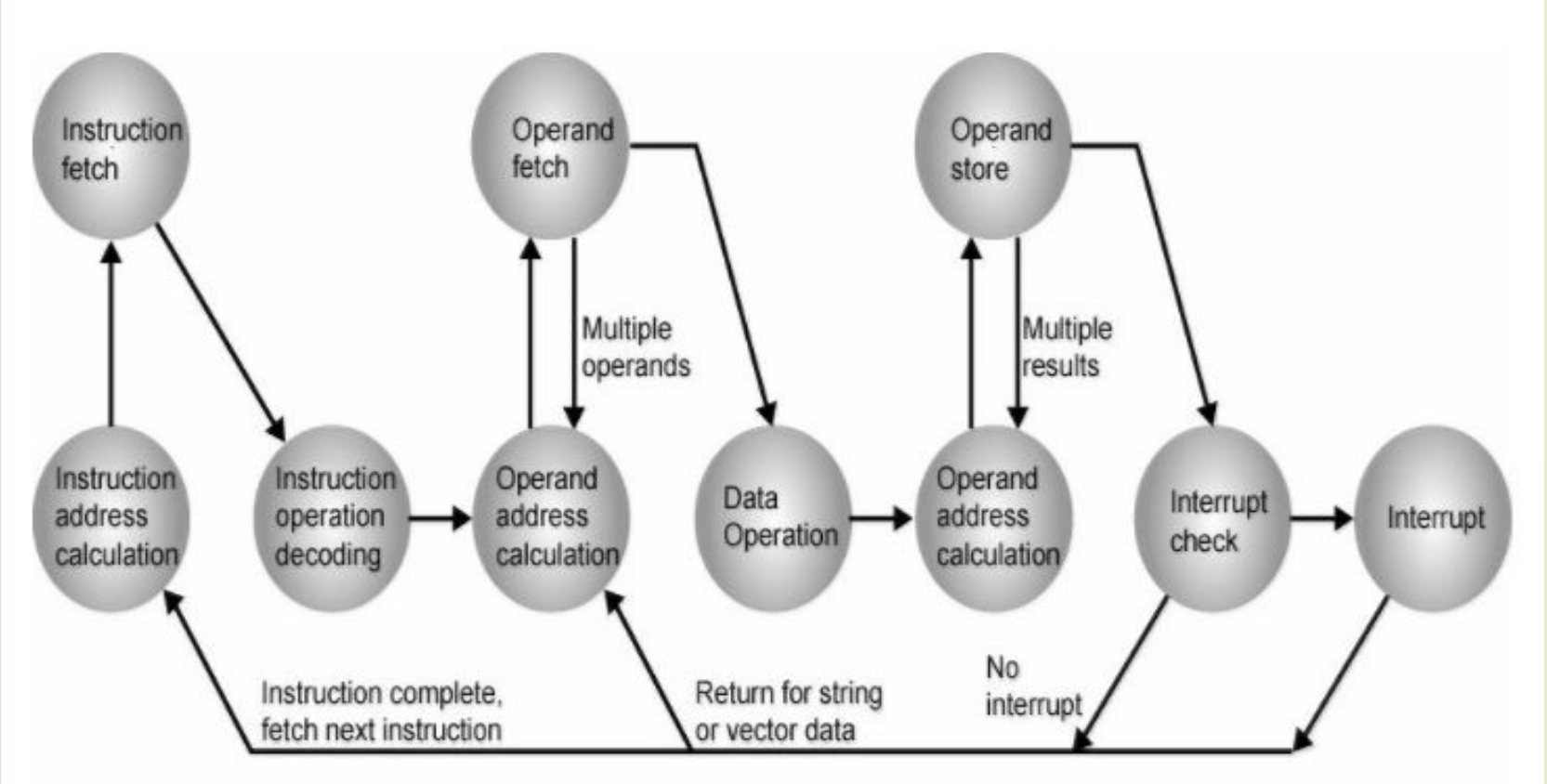
Instruction cycle



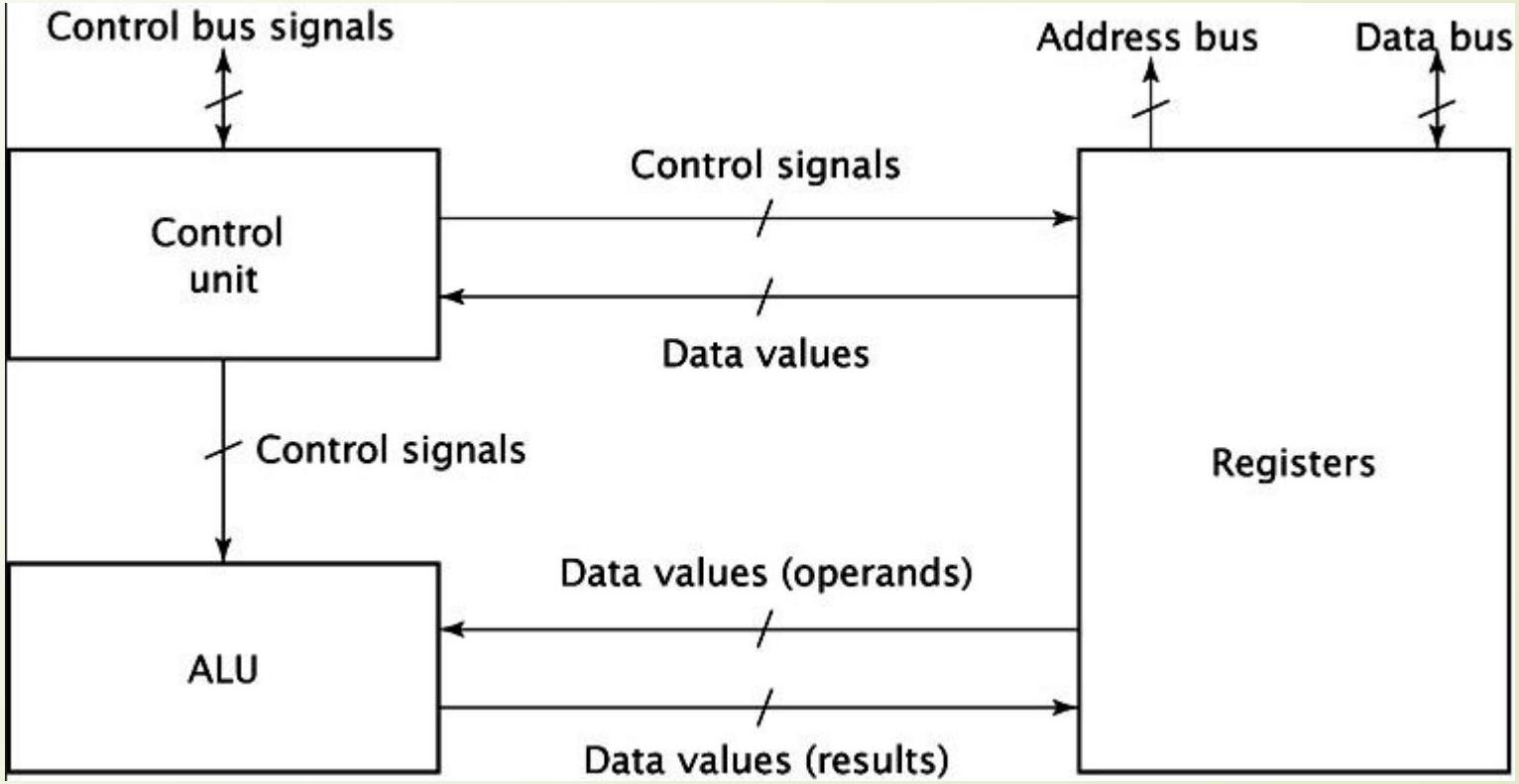
Contd..

- The instruction cycle is the procedure a microprocessor goes through to process an instruction.
- First, microprocessor fetches or reads instructions from memory. (microprocessor outputs address of instruction on the address bus)
  =>The register PC holds the address of next instruction to be fetched. Before the CPU outputs the address onto the address bus, it retrieves the address from PC.
  =>Memory sub-system inputs this address and places the corresponding instruction into system data bus.
  =>The CPU, then reads the instruction code from the system data bus.
- Then, it decodes the instruction determining which instruction it has fetched.
- Finally, it performs the operation necessary to execute the instruction.
- Each of these functions i.e. fetch, decode and execute consist of a sequence of one or more operations.

Contd…(instruction cycle state diagram)



CPU organization

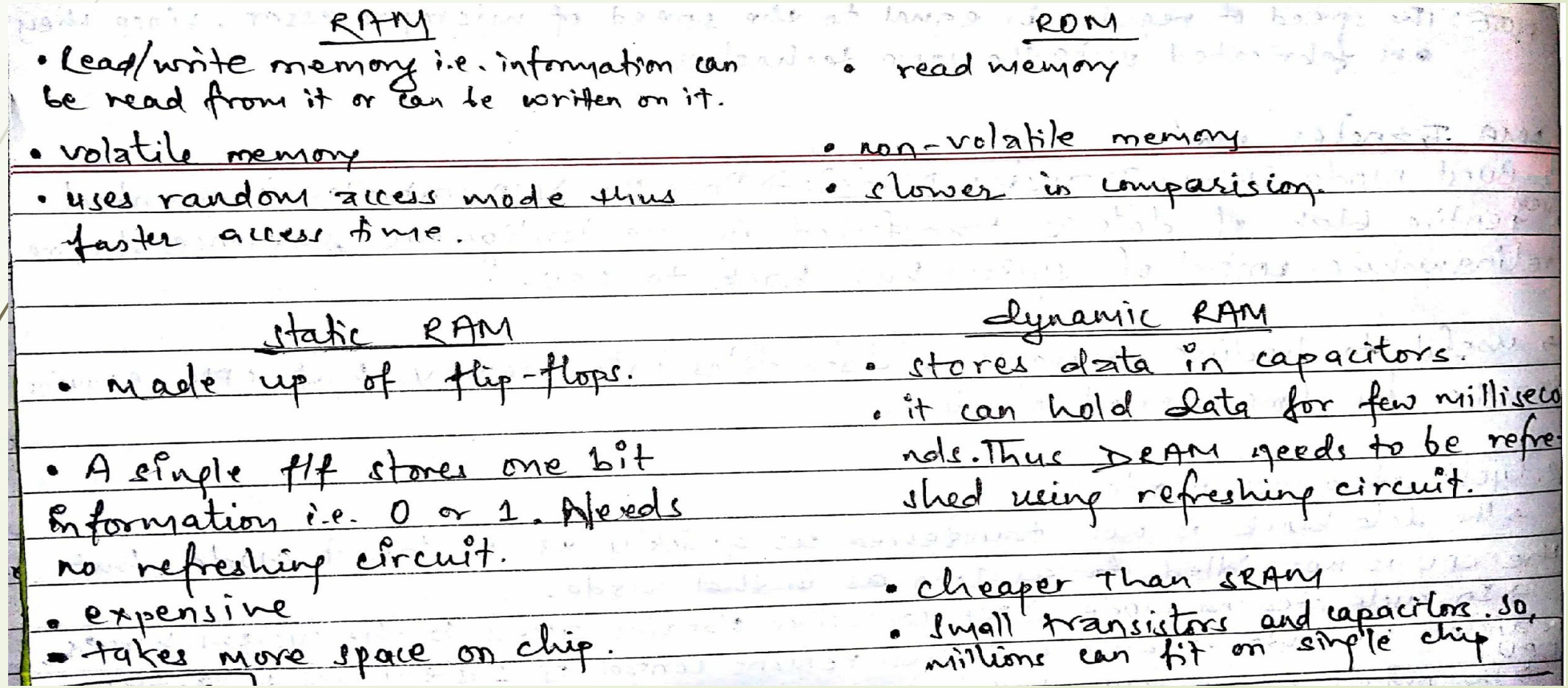


Contd...

- The register section includes the set of register and a bus(or other communication mechanism). It also contains other register which are not accessible directly by the programmer.
- ALU performs the arithmetic and logical operation which obtains its operand from the register section and stores the result back to it.
  =>Since, the ALU must complete its operation within a single clock cycle, it is constructed using only combinational circuit.
- The control unit generates the internal control signal that causes the register to load data, increment or clear content, output content, causes ALU to perform correct function.
  =>also generate signal for the system control bus such as READ, WRITE, IO/M(bar) signal.

Memory Subsystem Organization and Interfacing:

- Types of memory chips:



RAM

- Read/write memory i.e. information can be read from it or can be written on it.
- volatile memory
- uses random access mode thus faster access time.

static RAM

- made up of flip-flops.
- A single flf stores one bit information i.e. 0 or 1. Needs no refreshing circuit.
- expensive
- takes more space on chip.

ROM

- read memory
- non-volatile memory
- slower in comparision.

dynamic RAM

- stores data in capacitors.
- it can hold data for few milliseco nds. Thus DRAM needs to be refre- shed using refreshing circuit.
- cheaper than SRAM
- small transistors and capacitors. So, millions can fit on single chip

Contd...

ROM

↳ Programmable ROM

- can be programmed by user by means of proper equipment.
- the content of this type of memory cannot be changed unless it is erased by special device.

↳ Erasable PROM:

- can be programmed by using PROM programmer.
- Its memory can be erased by exposing chip to UV light.
- However chip should be removed from microcomputer system for programming.

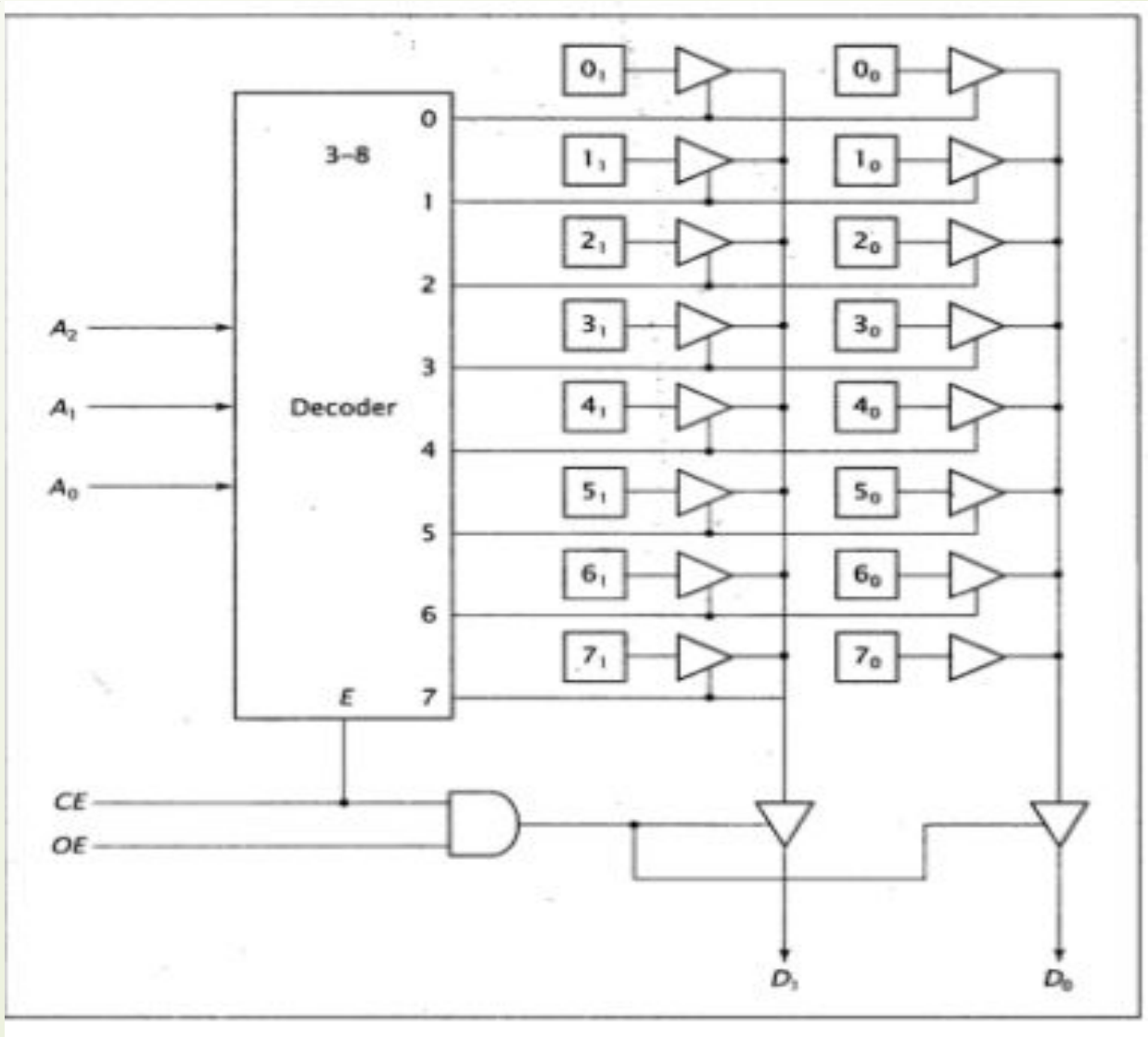
↳ Electrically EPROM:

- can be erased and programmed without removing the chip from the microcomputer system.
- content of EEPROMs can be erased electrically.

Internal Chip Organization:

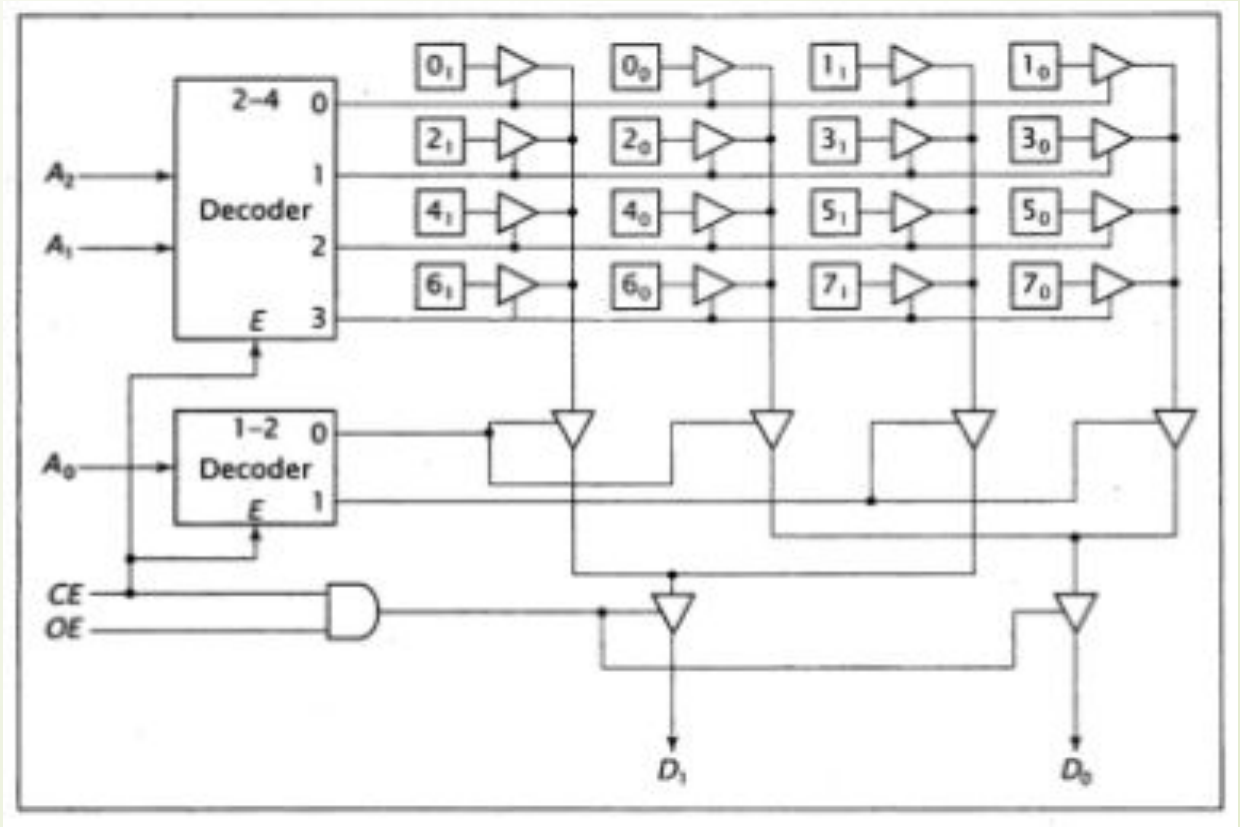
- Consider an 8 x 2 ROM chip:
  =>Address line = 3
  =>Data lines = 2
  =>16 bits of internal storage
- If CE = 0, decoder is disabled and no location is selected.
- If CE = 1and OE= 1,tri-state buffer for that location cell is enabled and data is output from the chip.

Contd..


3-8
Decoder
0
1
2
3
4
5
6
7
E
A_2
A_1
A_0
CE
OE
0_1
1_1
2_1
3_1
4_1
5_1
6_1
7_1
0_0
1_0
2_0
3_0
4_0
5_0
6_0
7_0
D_1
D_0

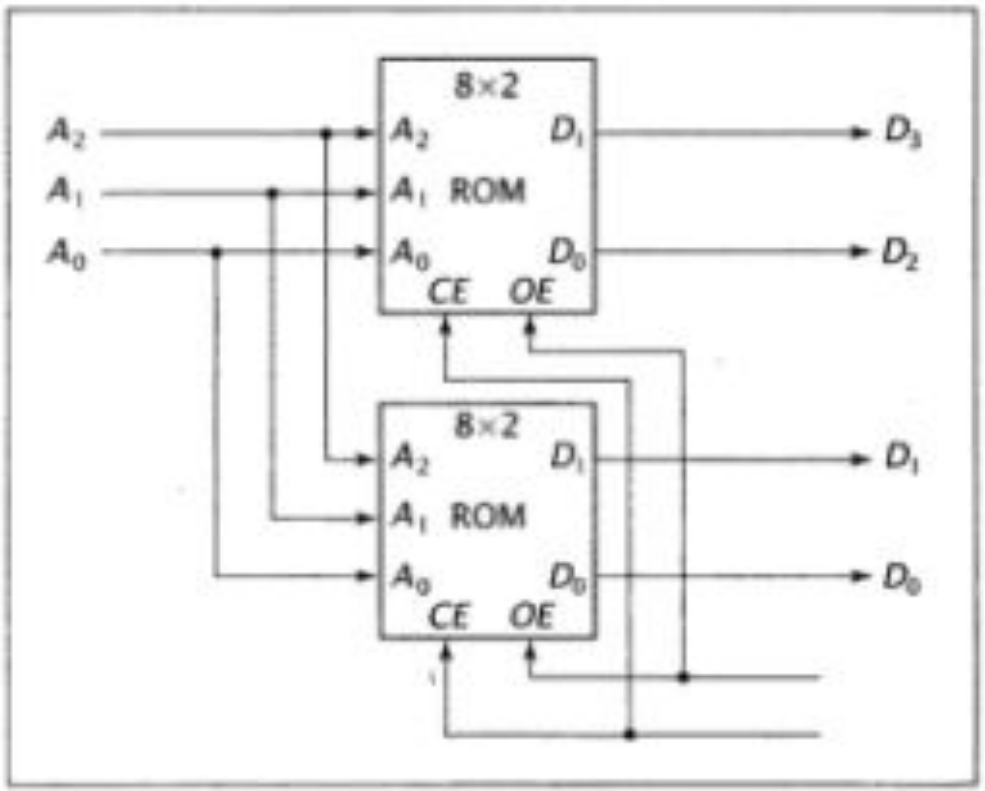
As the number of locations increases, the size of address decoder needed, becomes extremely large. To remedy this problem, the memory chip can be designed using multiple dimension of decoding.

Consider two dimensional organization of the same 8 x 2 ROM chip:

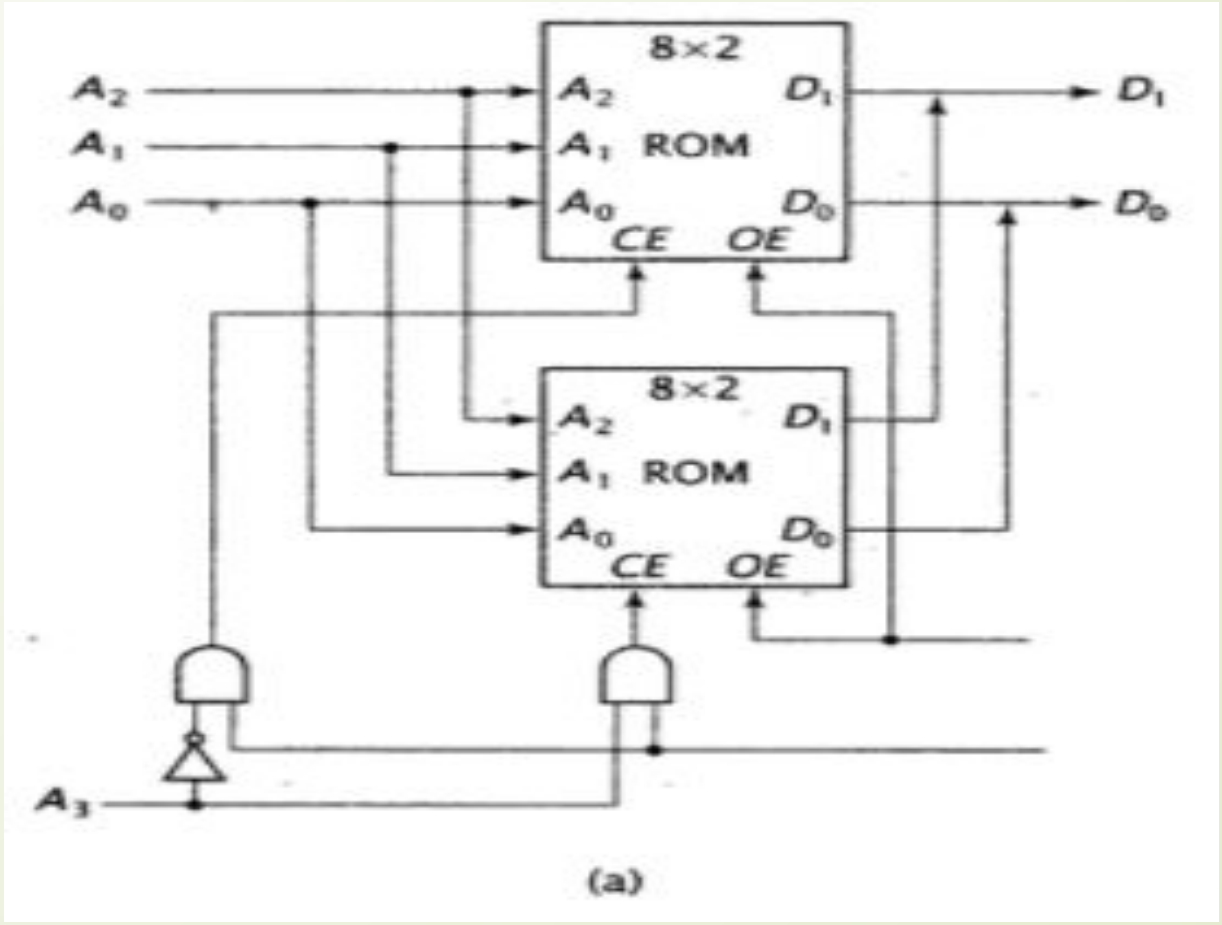


Contd..

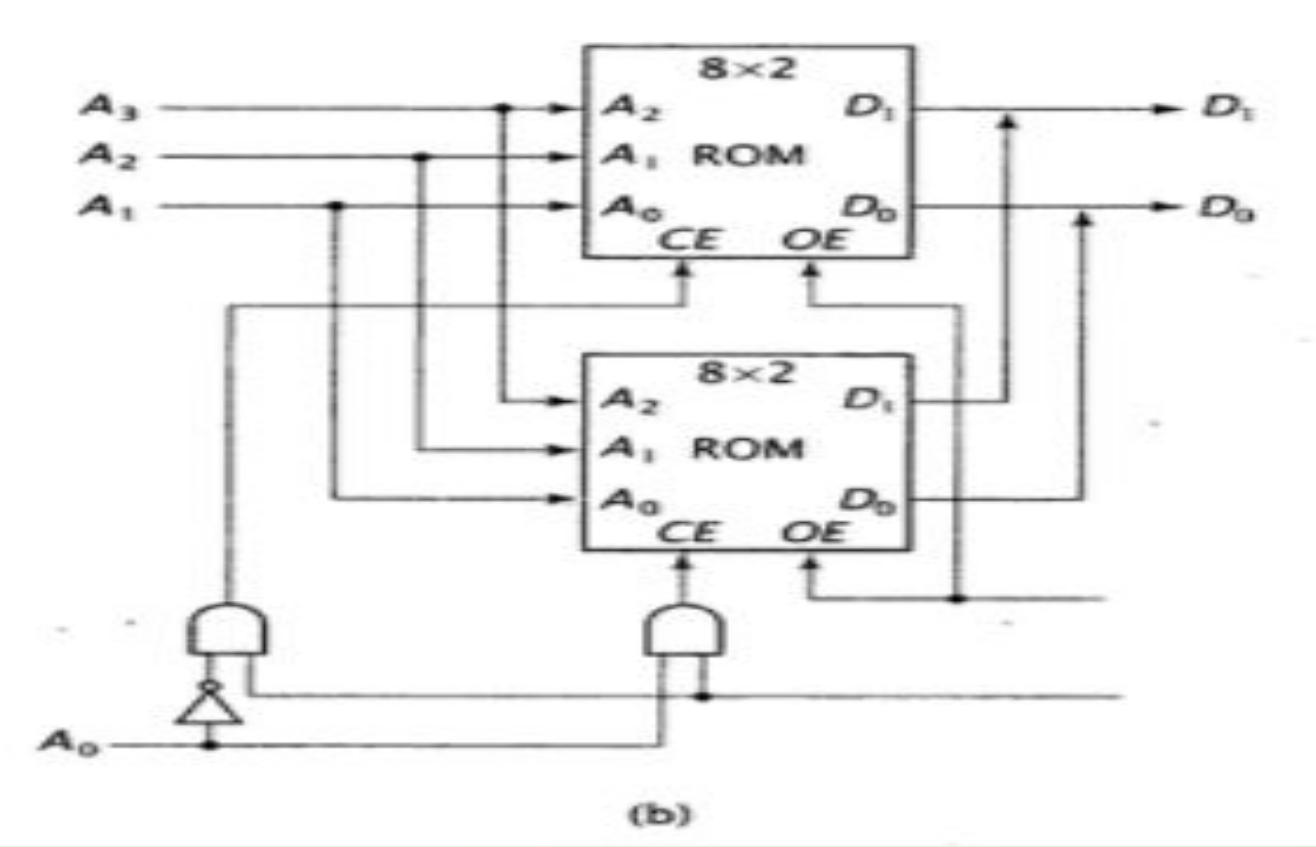
An 8 × 4 memory subsystem constructed from two 8 × 2 ROM chips



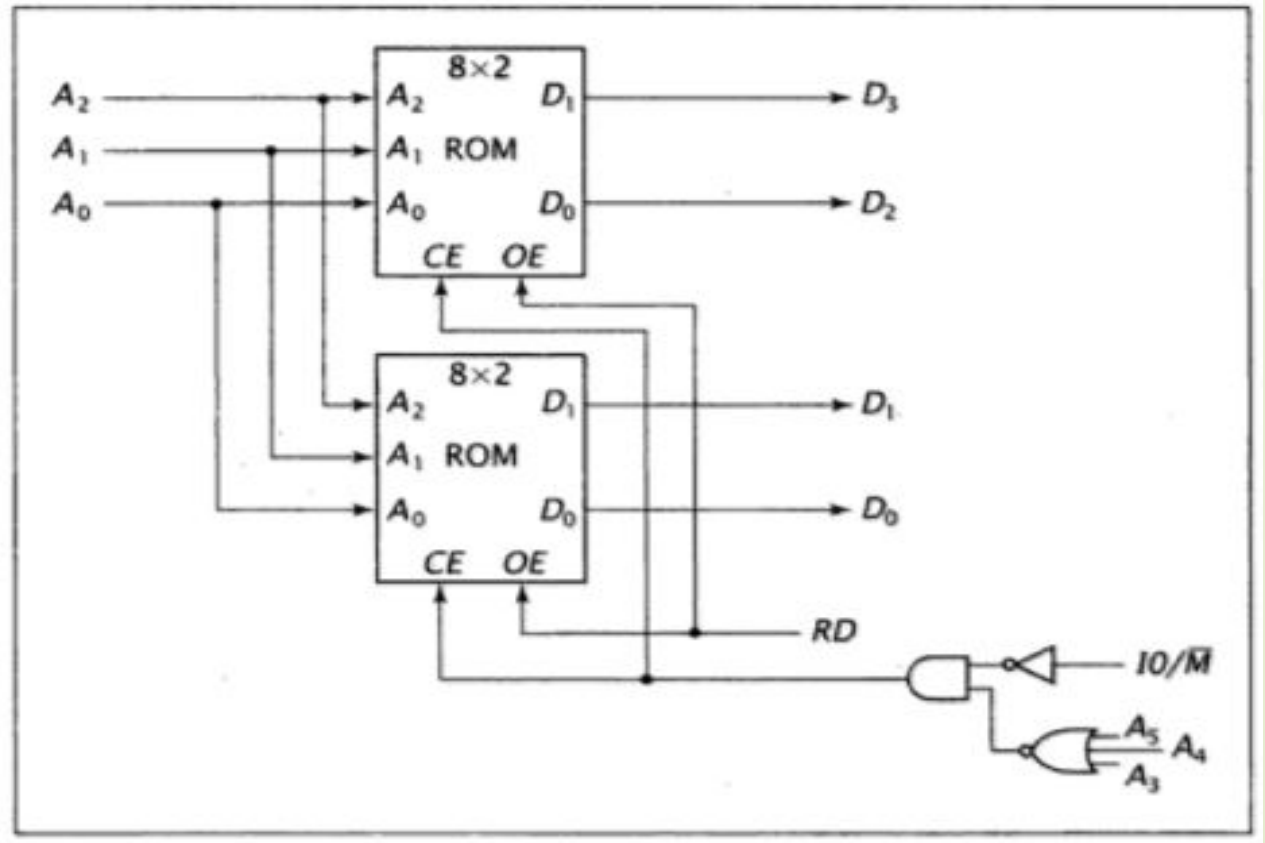
Construct a 16 x 2 memory subsystem from two 8 x 2 ROM chips with:
a. high-order interleaving and
b. low-order interleaving



Contd...

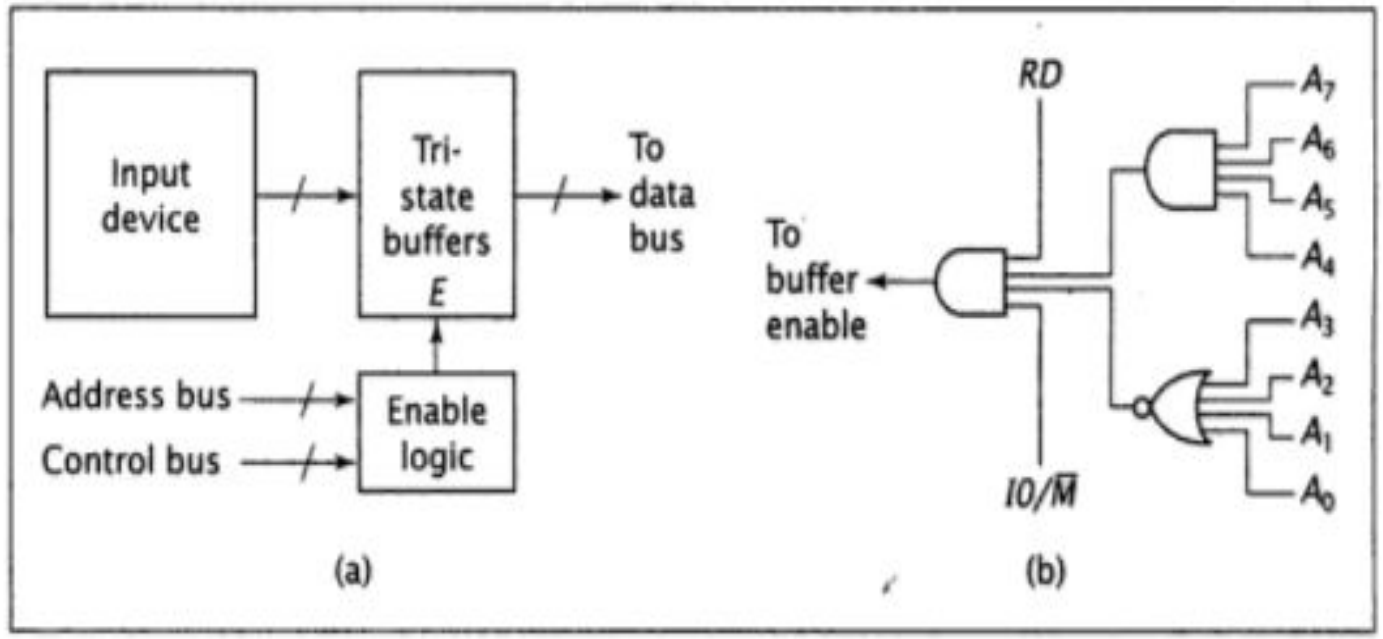

8×2
A3
A2
A1
A2
A1
A0
ROM
D1
D0
CE
OE
D1
D0
8×2
A2
A1
A0
ROM
D1
D0
CE
OE
A0
(b)

Construct a 8 x 4 memory subsystem from two 8 x 2 ROM chips with control signals.
=>Assume system with 6-bit address bus
=>A_2, A_1, A_0 select location within memory chips.
=>A_5, A_4, A_3 must be 000 for the chips to be active
=>RD or RD' drives OE
=>IO/M(bar) signal supplied by processors that use isolated I/O



I/O subsystem organization and Interfacing

An input device: (a) with its interface and (b) the enable logic for the tri-state buffers



Contd..

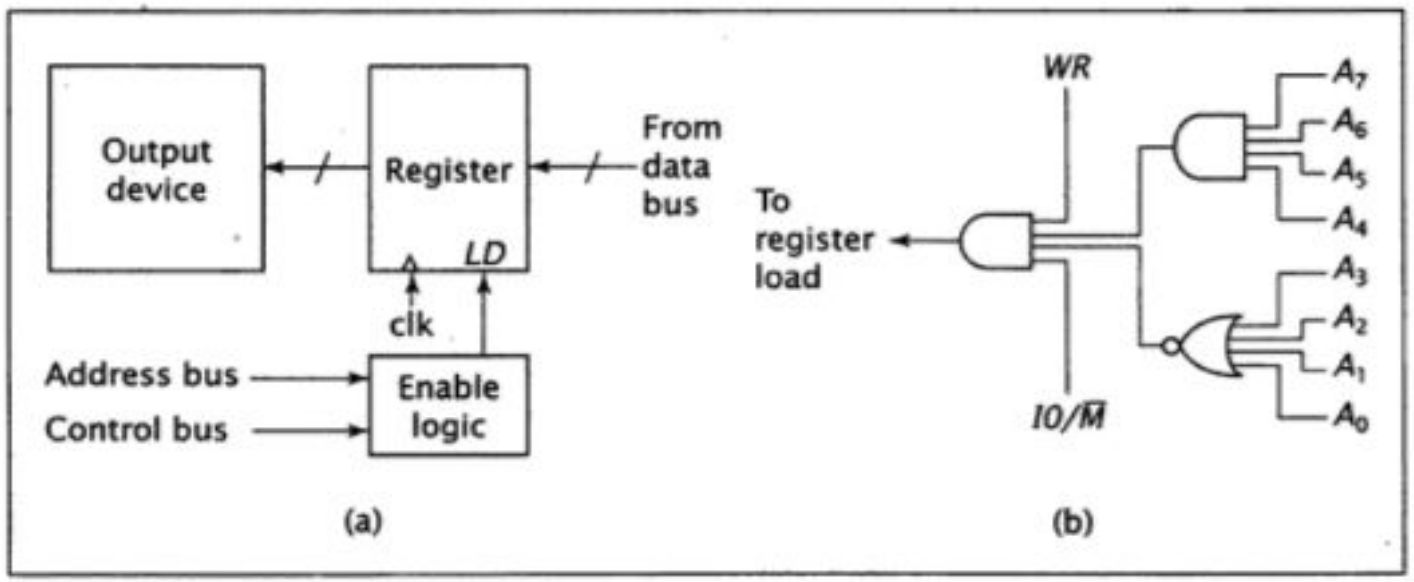
- The data from the input device goes to the tri-state buffer.
- When the values on the address bus and control bus are correct, the buffers are enabled and data passes onto the data bus.
- The CPU, then can read these data.
- The key to this design is the enable logic.
  =>For the input device, the read signal (RD) should be asserted.
  =>Figure (b) shows the enable logic for an input device at address 11110000 with 8-bit address and control signals RD and IO/Memory(I0/M(bar))

Contd...

- For the interface circuit for an output device, the tri-state buffer is replaced by a register.
- The tri-state buffers are used in input device interface to make sure that no more than one device writes data to the bus at any time.
- Since, the o/p devices read data from the bus, they do not need buffers so that data can be made available to all output devices.

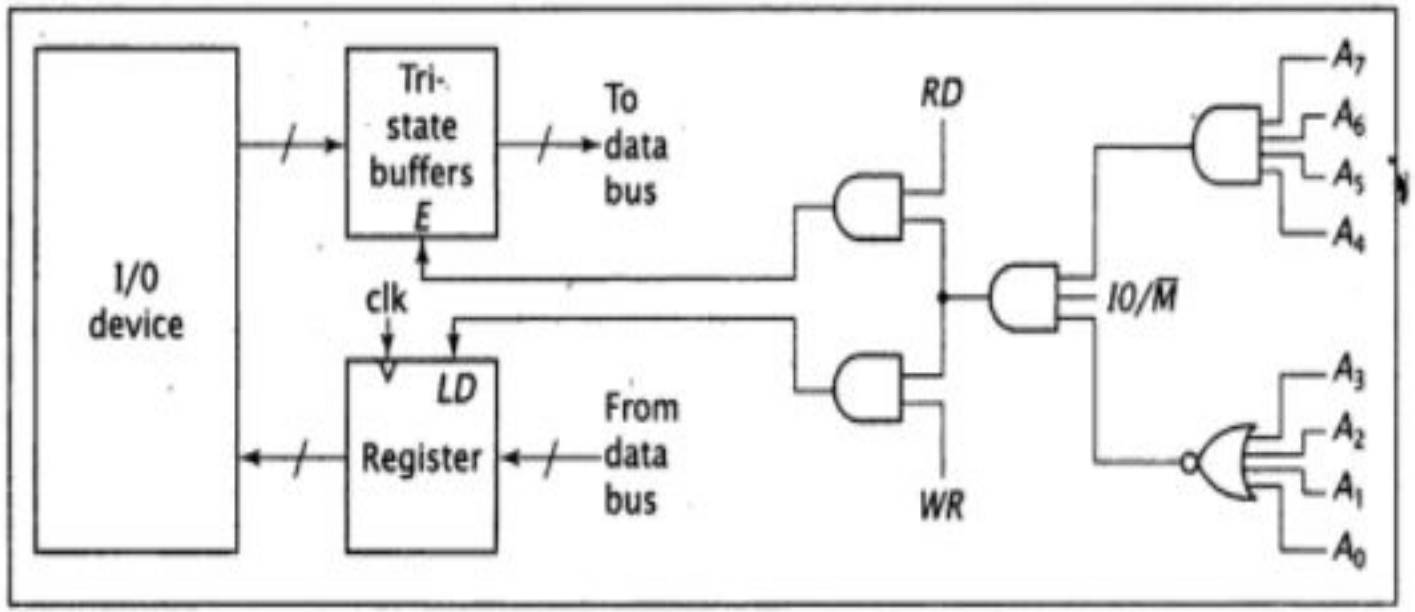
Contd...

An output device: (a) with its interface and (b) the load logic for the register

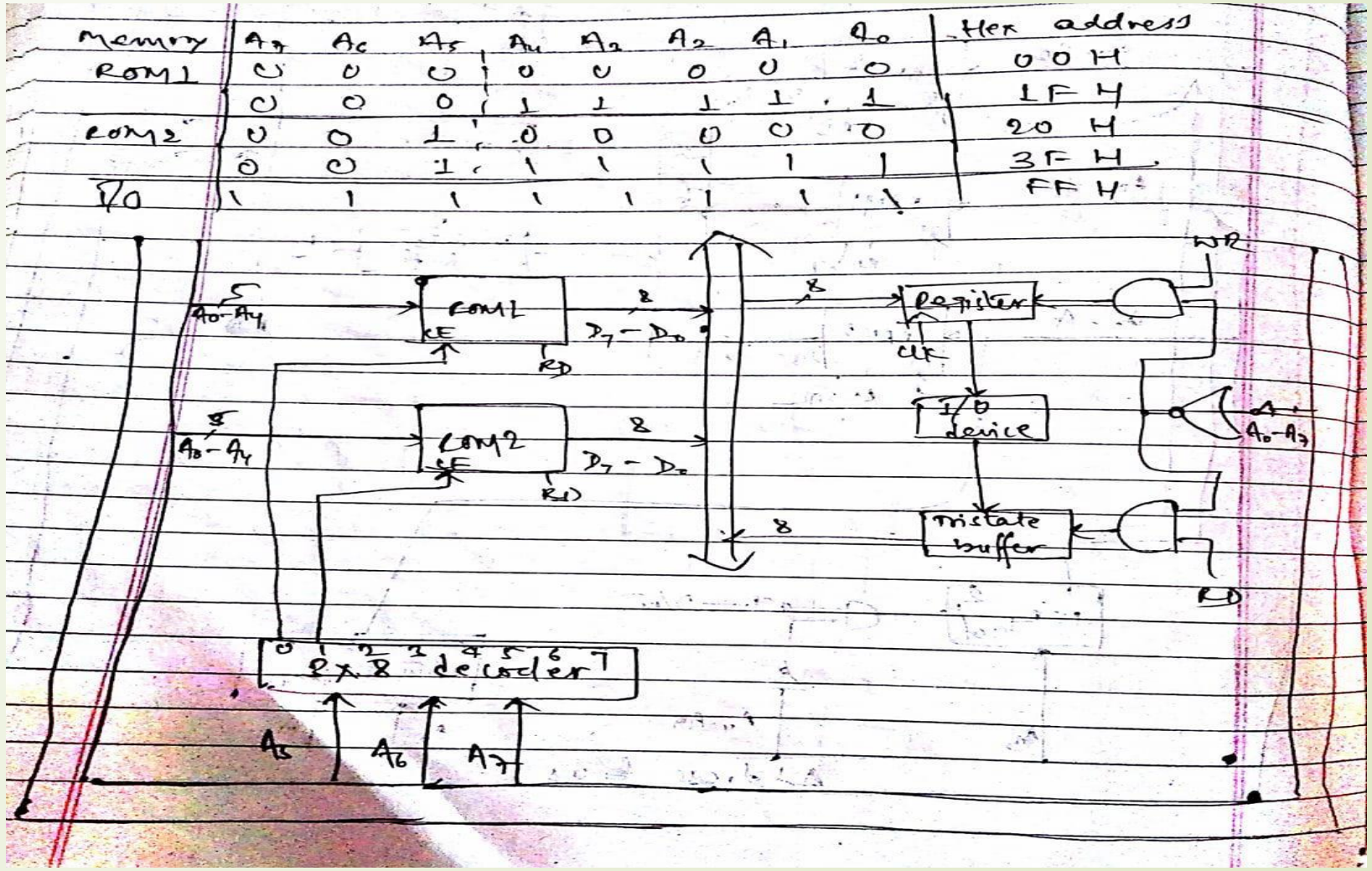


Contd...

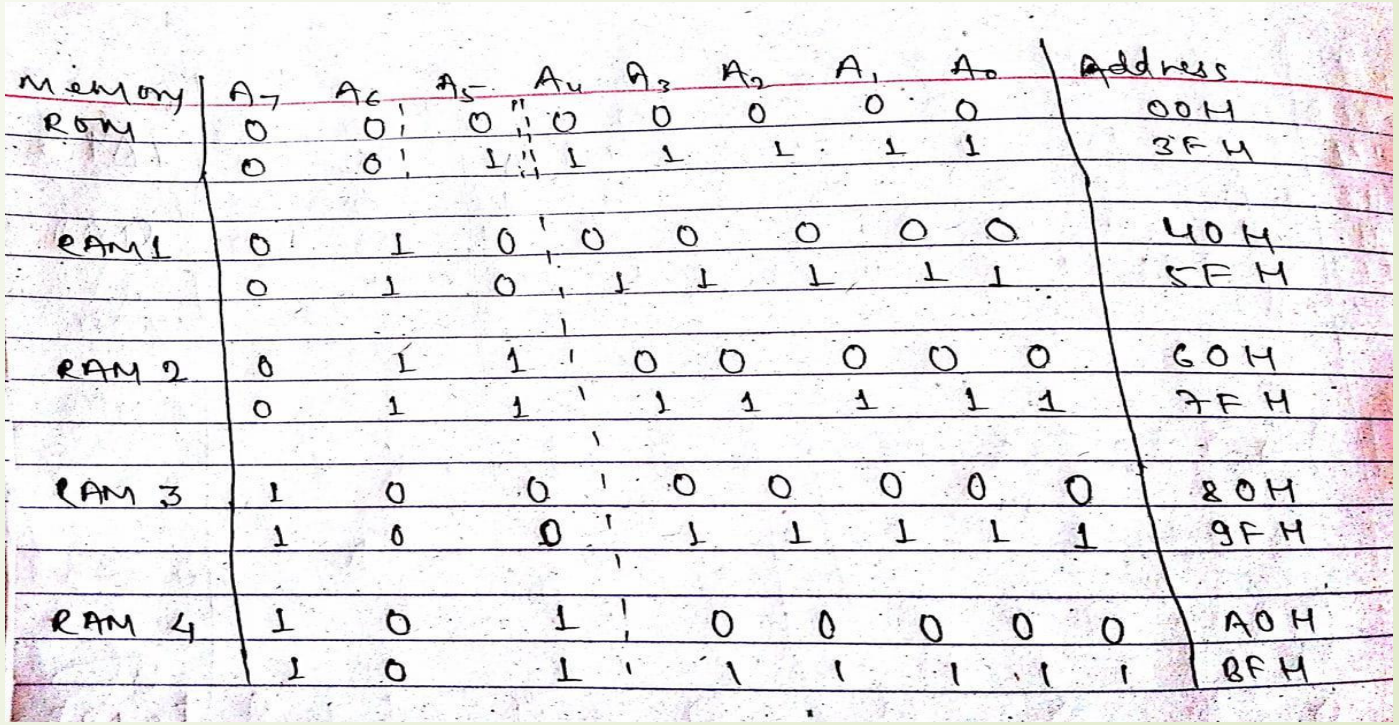
A bidirectional input/output device with its interface and enable/load logic



A CPU with 8-bit data bus and 8-bit address bus uses memory mapped I/O. It has 32 byte of ROM at 00H and 32 byte of ROM at 20H. It also has an I/O device at FFH. Show the load logic and enable logic.

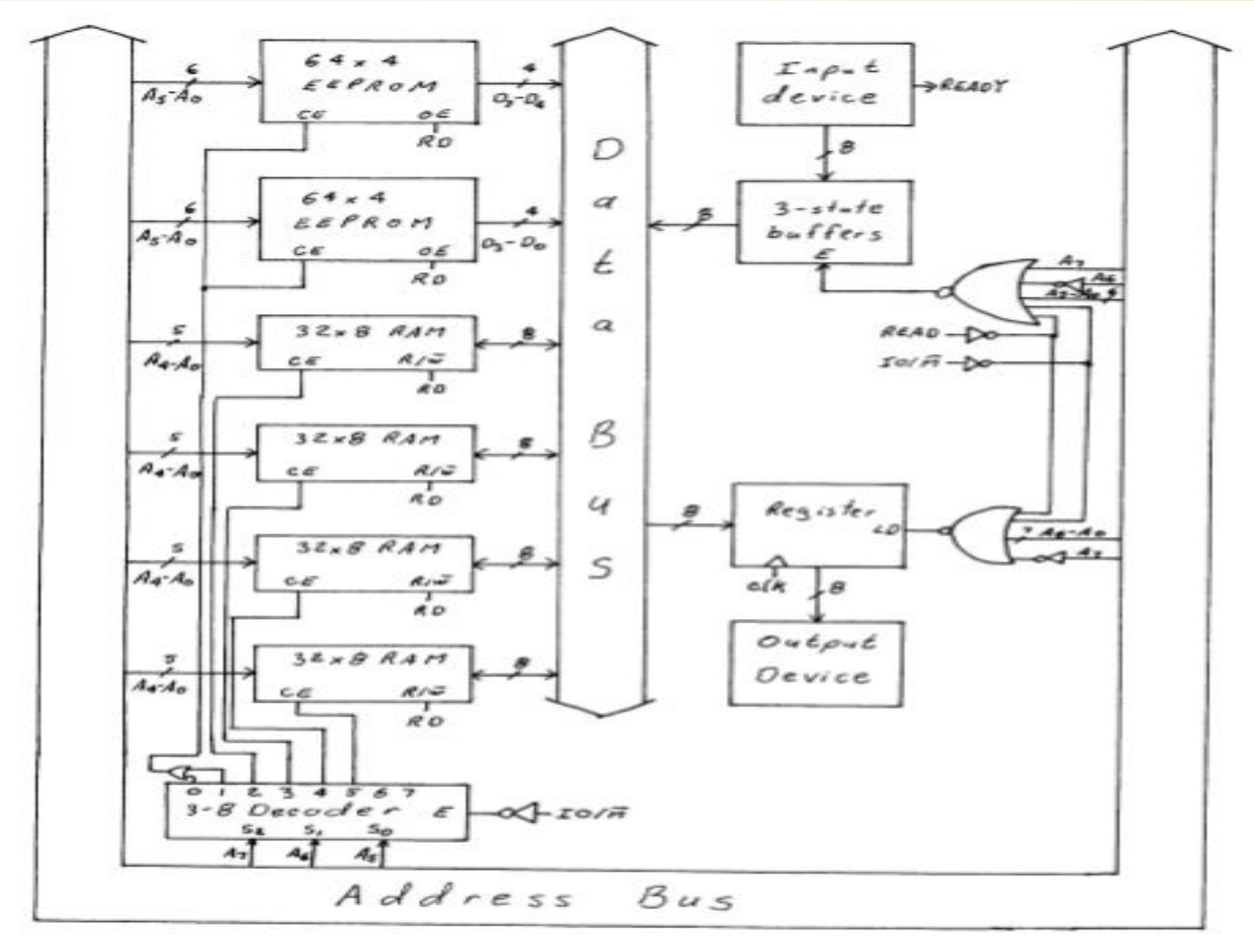


Computer with 8-bit data bus and 8-bit control bus uses isolated I/O. It has 64 bytes of ROM starting at 00H constructed using 64 x 4 chips; 128 bytes of RAM, starting at address 40H constructed using 32 x 8 chips; an input device with Ready at address 40H and output with an ready at 80H.

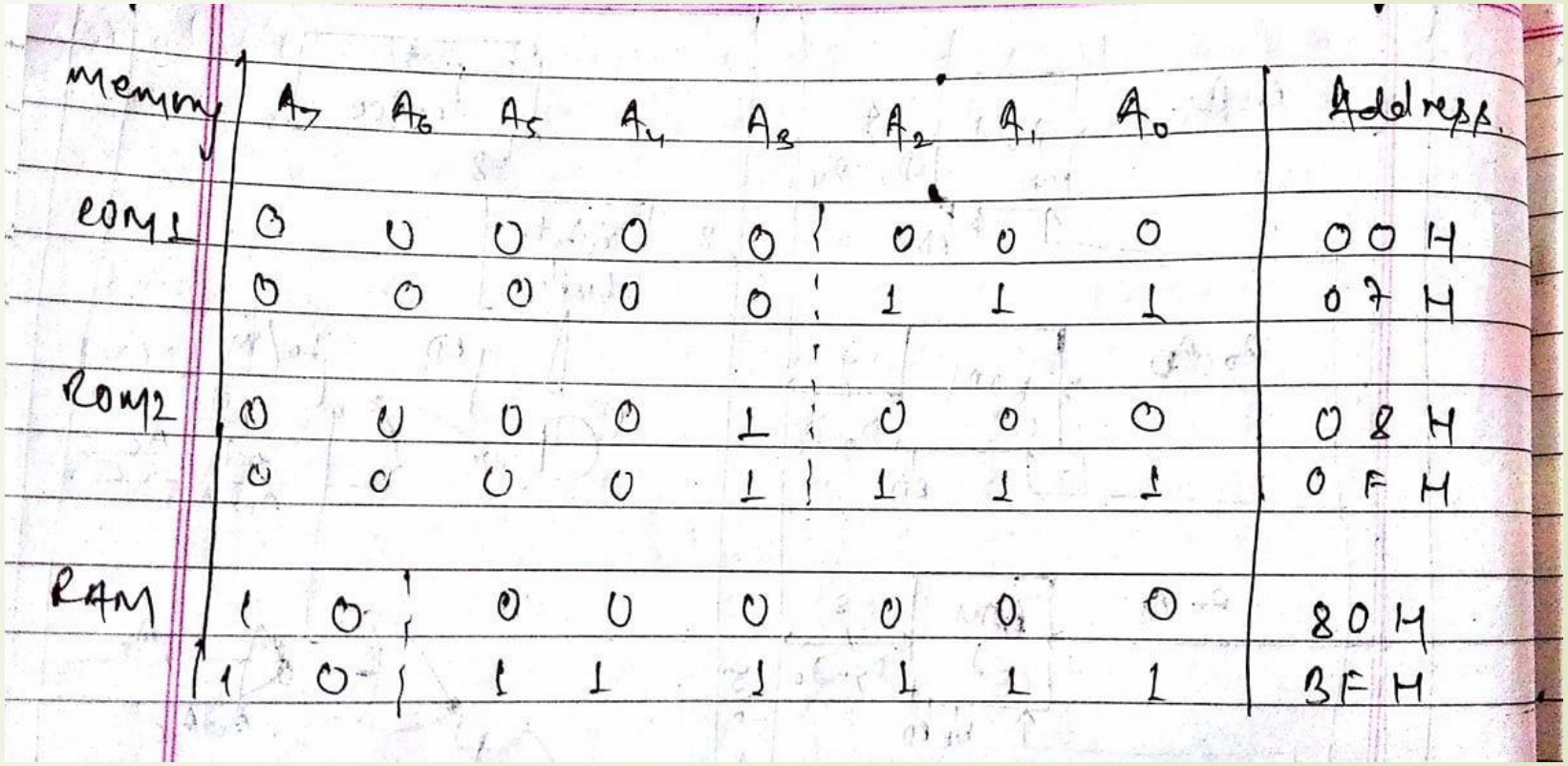


Memory	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address
ROM	0	0	0	0	0	0	0	0	00H
	0	0	1	1	1	1	1	1	3FH
RAM 1	0	1	0	0	0	0	0	0	40H
	0	1	0	1	1	1	1	1	5FH
RAM 2	0	1	1	0	0	0	0	0	60H
	0	1	1	1	1	1	1	1	7FH
RAM 3	1	0	0	0	0	0	0	0	80H
	1	0	0	1	1	1	1	1	9FH
RAM 4	1	0	1	0	0	0	0	0	A0H
	1	0	1	1	1	1	1	1	BFH

Contd..

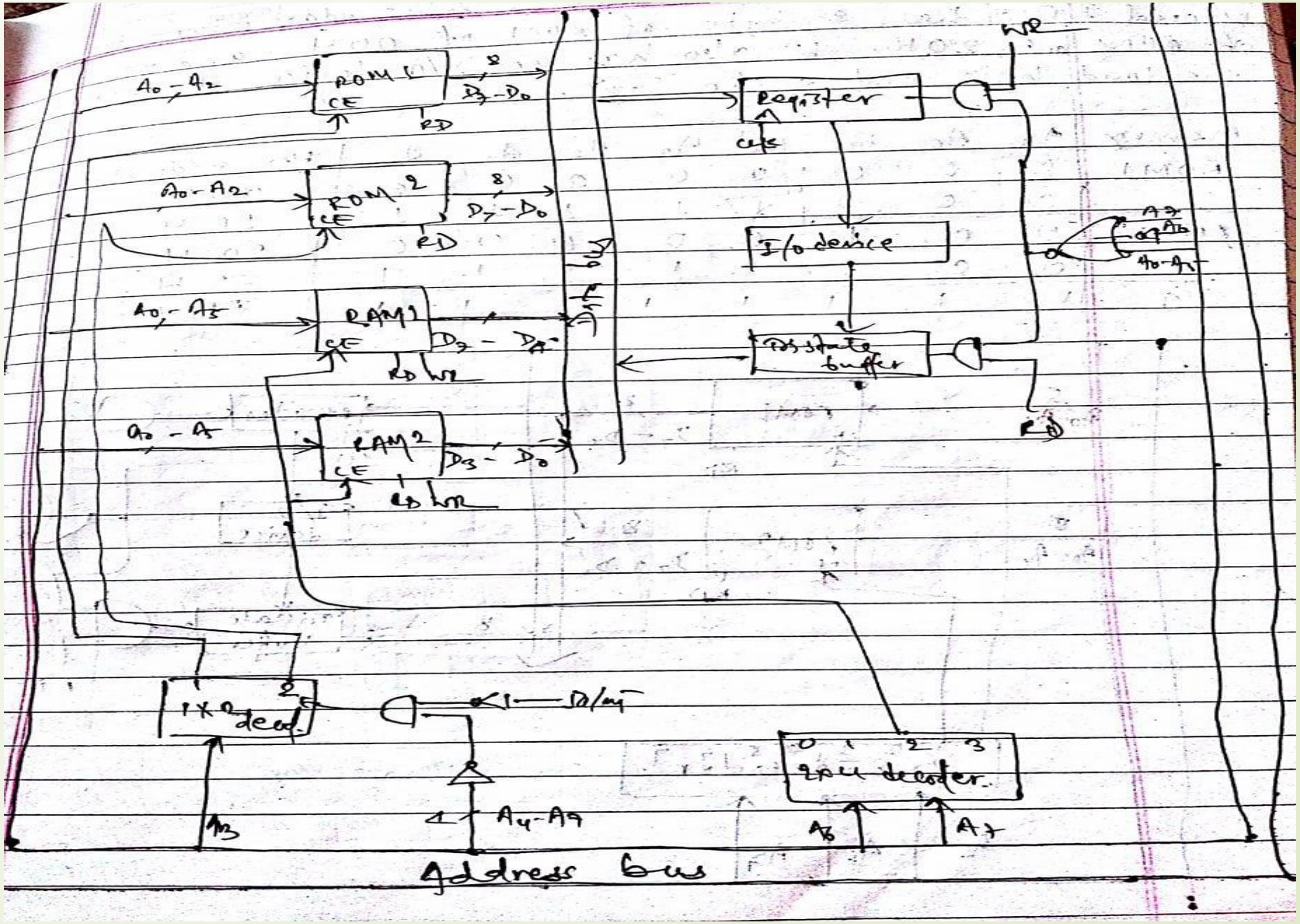

64 x 4 EEPROM
CE
OE
RD
3-state buffers
Input device
READY
32x8 RAM
R/W
Register
LD
clk
Output Device
3-8 Decoder
IO/M
READ
Data Bus
Address Bus

A computer system with an 8-bit address and an 8-bit data bus using isolated I/O. It has 16 x 8 ROM starting at address 00H constructed using 8 x8 chips; 64 x 8 of RAM starting at address 80H constructed using 64 x 4 chips. There is an I/O device at 40H. Show the design for the system.



Memory	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address
ROM1	0	0	0	0	0	0	0	0	00 H
	0	0	0	0	0	1	1	1	07 H
ROM2	0	0	0	0	1	0	0	0	08 H
	0	0	0	0	1	1	1	1	0F H
RAM	1	0	0	0	0	0	0	0	80 H
	1	0	1	1	1	1	1	1	BF H

Contd..


ROM 1
CE
RD
$A_0 - A_2$
$D_7 - D_0$
ROM 2
RAM 1
RAM 2
Register
I/o device
Tri-state buffer
WR
RD
1x2 decd.
2x4 decoder
$A_4 - A_9$
A_3
A_6
A_7
Address bus
Data bus