

Q.N.1.

A. Ans.

Analog Signal

- They are continuous signals.
- These signals have infinite range of values.
- More exact values but difficult to work with.

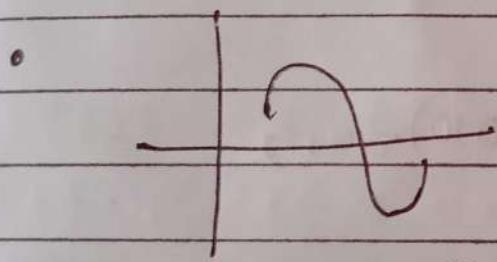


fig : Analog signal.

Digital Signal.

- They are discrete signals.
- Finite range of values.
(i.e. 0 and 1).
- Not as exact as analog, but easier to work with.

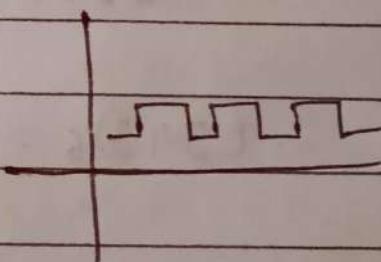


fig : Digital signal

- Accuracy and precision is less compared to digital signal.

- They are more sensitive to noise and contains lots of noise in them.

- Accuracy and precision is greater and reliable.

- They are less sensitive to noise.

B. Ans.

i. Here,

$$\begin{aligned}(543)_6 &= 5 \times 6^2 + 4 \times 6^1 + 3 \times 6^0 \\&= 5 \times 36 + 24 + 3 \\&= 180 + 27 \\&= 207_{10}\end{aligned}$$

Now converting 207 to Excess-3 code.

$$\begin{array}{r} 2 \quad 0 \quad 7 \\ 0010 \quad 0000 \quad 0111 \\ + 0011 \quad 0011 \quad 0011 \\ \hline 0101 \quad 0011 \quad 1010 \end{array}$$

$$\therefore (543)_6 = (010100111010)_{\text{Excess-3}}$$

ii. $(708)_{10} = (\dots)_{842_1}$

$$\therefore (708)_{10} = (0111 \quad 0000 \quad 1000)_{842_1}$$

C. Ans.

i. $(1011)_2 - (10100)_2$

Taking 2's complement of $(10100)_2$

$$\begin{aligned}&= 01011 + 1 \\&= 01100\end{aligned}$$

Now, adding 2's complement of subtrahend to minued.

$$\begin{array}{r} \therefore 0 \ 1 \ 0 \ 1 \ 1 \\ + 0 \ 1 \ 1 \ 0 \ 0 \\ \hline 1 \ 0 \ 1 \ 1 \ 1 \end{array}$$

since, there is no carry in the result. so we get negative result.

$$\begin{aligned} \text{Again the 2's complement of } 10111 \text{ is, } & 01000 + 1 \\ & = 1001. \end{aligned}$$

$$\therefore (1011)_2 - (10100)_2 = -(1001)_2.$$

ii. $(952)_{10} - (873)_{10}$

$$\begin{aligned} \text{Taking 2's complement of } (873)_{10} &= (1101101001)_2. \\ &+ 1 \\ &= (1101101010). \end{aligned}$$

Now, Adding 2's complement of subtrahend to minued.

~~$$\begin{array}{r} \therefore 1 \ 1 \ 1 \ 0 \ 1 \ 1 \ 1 \ 0 \ 0 \ 0 \\ + 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 1 \ 0 \ 1 \ 0 \\ \hline 1 \ 1 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \ 1 \ 0 \end{array}$$~~

ii. $(952)_{10} - (873)_{10}$.

Ans. Converting into binary we get,
 $(952)_{10} = (1110111000)_2$. &
 $(873)_{10} = (1101101001)_2$.

i's complement of minuend = $(1101101001)_2$
= $(0010010110)_2 + 1$
= 0010010111

Now, Adding i's complement of subtrahend to minuend.

$$\begin{array}{r} 1110111000 \\ + 0010010111 \\ \hline (1)0001001111 \end{array}$$

↓ discarded.

$$\therefore (952)_{10} - (873)_{10} = (0001001111)_2 = (79)_{10}.$$

iii. $(368)_{BCD} - (256)_{BCD}$.

Ans. Converting into binary we get,

$$368 = 10111000_2 \text{ and } 256 = 100000000_2$$

i's complement of subtrahend = $(100000000)_2$
= $(01111111)_2 + 1$
= 100000000

Now, Adding i's complement of subtrahend to minuend.

$$\begin{array}{r} 010111000 \\ + 100000000 \\ \hline 110111000 \end{array}$$

Q.N.2.

A. Ans.

$$\begin{aligned} & 1. \overline{AB} + BC + \overline{A}B\overline{C} \\ &= \overline{AB} + BC \cdot (A + \overline{A}) + \overline{ABC} \\ &= \overline{AB} + ABC + \overline{ABC} + \overline{ABC} \\ &\approx (\cancel{+}), \end{aligned}$$

ANS. $\overline{A}\overline{B} + BC + \overline{AB}\overline{C}$

$$\begin{aligned} &= \overline{A}\overline{B} + \overline{A}B\overline{C} + BC \\ &= \overline{A}(\overline{B} + B\overline{C}) + BC \end{aligned}$$

Wrong question.

B. Ans.

$$\begin{aligned} L.H.S. & X\overline{Y} + Y\overline{Z} + Z\overline{X} \\ &= X\cancel{\overline{Y}}(X + \overline{X}) + Y\cancel{\overline{Z}}(Y + \overline{Y}) + Z\cancel{\overline{X}}(Z + \overline{Z}) \\ &= X\cancel{\overline{Y}} + 0 + Y\cancel{\overline{Z}} + 0 + Z\cancel{\overline{X}} + 0 \end{aligned}$$

•

Unless there is some special relation betⁿ X, Y, Z and \overline{X} , \overline{Y} and \overline{Z} it won't be proved by algebraic method.

We can prove it by assuming.

As, $X = 1, Y = 1$ and $Z = 1$. Then $\overline{X} = 0, \overline{Y} = 0$ & $\overline{Z} = 0$.

Then, L.H.S.

$$\begin{aligned} & X\overline{Y} + Y\overline{Z} + Z\overline{X} \\ &= 1 \cdot 0 + 1 \cdot 0 + 1 \cdot 0 \\ &= 0 \end{aligned}$$

R.H.S.

$$\begin{aligned} & \overline{XY} + \overline{YZ} + \overline{ZX} \\ &= 0 \cdot 1 + 0 \cdot 1 + 0 \cdot 1 \\ &= 0 \quad \therefore L.H.S. = R.H.S. \end{aligned}$$

B. Ans.

Here, $F = \overline{BCD} + \overline{ACD} + \overline{ABC} + \overline{ABCD}$
 $d = \overline{ABC}\overline{D} + ACD + A\overline{BD}$.

Converting the given expression in standard form

$$\begin{aligned} \text{so, } F &= \overline{BCD}(A+\overline{A}) + \overline{ACD}(B+\overline{B}) + \overline{ABC}(D+\overline{D}) \\ &\quad + \overline{ABC}\overline{D} \\ &= A\overline{BC}\overline{D} + \overline{A}\overline{B}C\overline{D} + \overline{ABC}\overline{D} + \overline{ABC}\overline{D} + \\ &\quad \overline{ABC}\overline{D} + \overline{ABC}\overline{D} + \overline{ABC}\overline{D} \\ &= {}^6\overline{ABC}\overline{D} + {}^7\overline{ABC}\overline{D} + {}^8\overline{ABC}\overline{D} + {}^9\overline{ABC}\overline{D} + \\ &\quad {}^10\overline{ABC}\overline{D} + \overline{ABC}\overline{D} \\ &= (0, 2, 3, 6, 7, 10) \end{aligned}$$

Similarly for d,

$$\begin{aligned} d &= \overline{ABC}\overline{D} + ACD(B+\overline{B}) + A\overline{B}\overline{D}(C+\overline{C}) \\ &= {}^5\overline{ABC}\overline{D} + {}^{15}ACD + {}^{11}A\overline{B}\overline{D} + {}^{10}\overline{ABC}\overline{D} + {}^8\overline{ABC}\overline{D} \\ &= (5, 8, 10, 11, 15). \end{aligned}$$

For SOP,

		\overline{BCD}					
		00	01	11	10		
AB	CD	1	0	1	1	A.C	
		0	0	1	1		
00	0	0	x	0			
01	x	0	x	1			
10					$A\overline{B}C$		

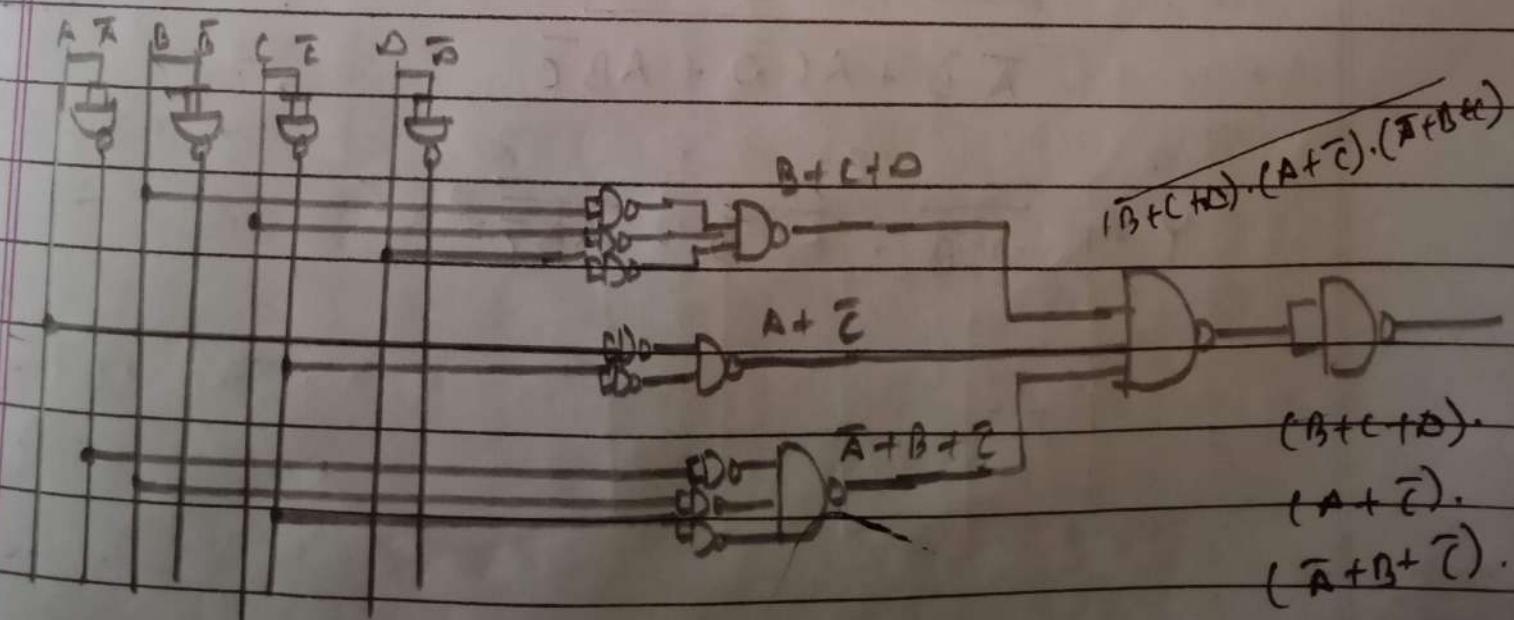
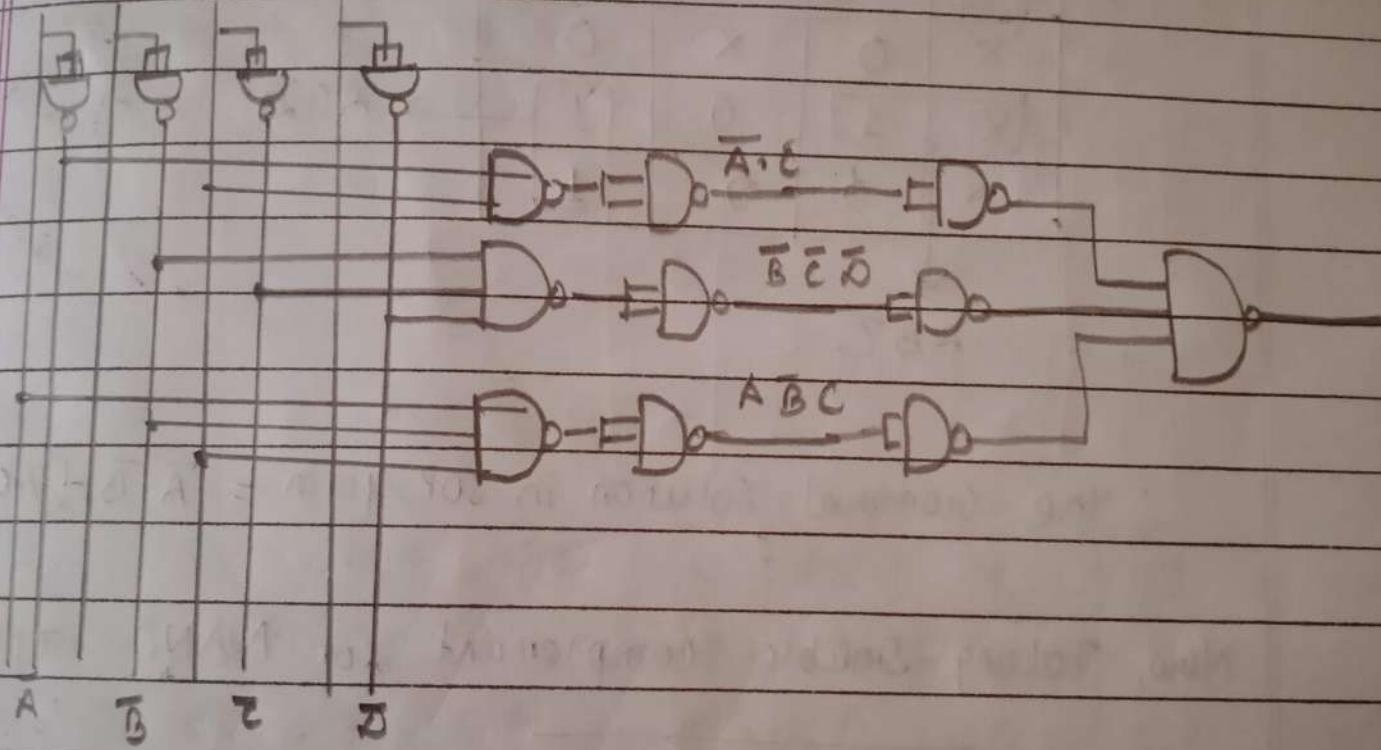
\therefore General Solution is, $= \overline{AC} + \overline{BC}\overline{D} + A\overline{B}C$

For PDS.

POS.		$B + C + D$				
AB	CD	BD	DI	II	IO	
BD	0	1	0	0		$A + \bar{C}$
DI	1	1	0	0		
II	1	1	X	1		
IO	X	1	X	0		\bar{A}

∴ General solution is, = $(B+C+\alpha) \cdot (A+\bar{C}) \cdot (\bar{A}+B+\bar{C})$

A B C D



C. Ans.

Given is of SOP form. and is of four variables.

$$\text{i.e. } F(A, B, C, D) = \Sigma(0, 1, 2, 3, 10, 13, 14).$$

$$d(A, B, C, D) = \Sigma(4, 7, 12).$$

K. Map.

AB	CD	00	01	11	10	
00		1	1	1	1	$\bar{A} \bar{B}$
01	x	0	x	0		
11	x	1	0	1		$A \bar{C} \bar{D}$
10	0	0	0	1		

↓

ABC .

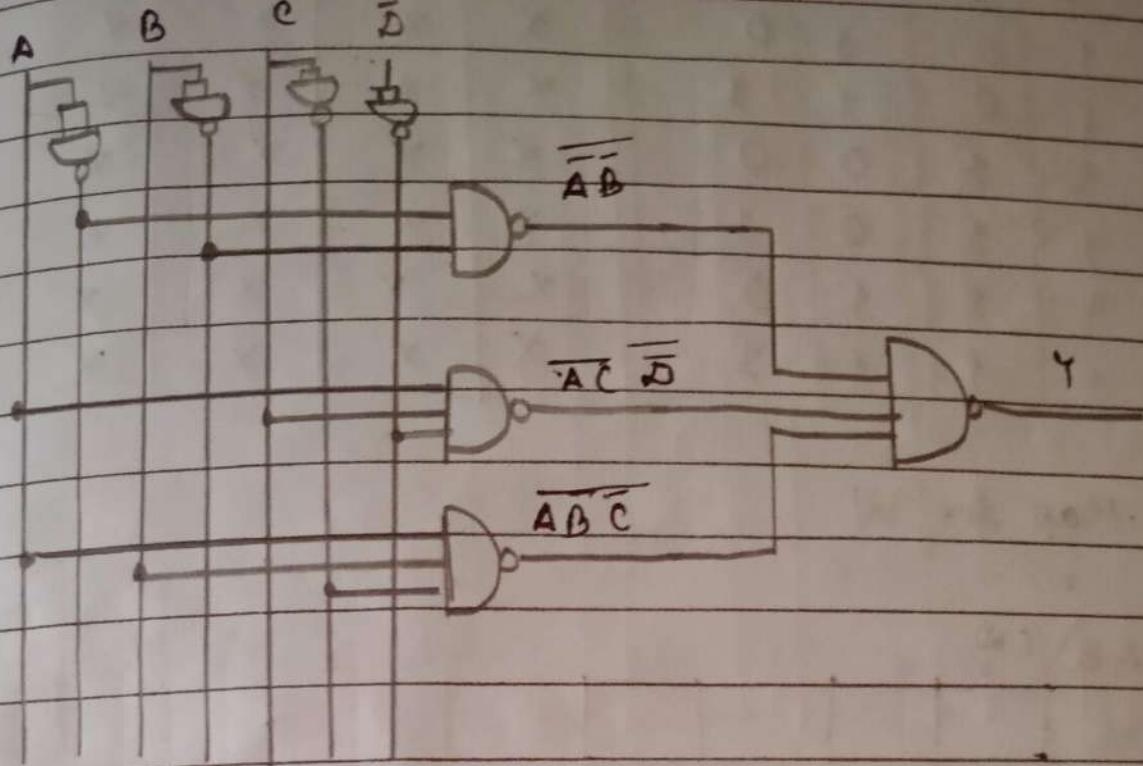
∴ The General solution in SOP form = $\bar{A} \bar{B} + A \bar{C} \bar{D} + ABC$.

Now, Taking Double complement for NAND implementation.

$$\overline{\bar{A} \bar{B} + A \bar{C} \bar{D} + ABC}$$

$$Y = \overline{\overline{A} \overline{B}} \cdot \overline{A \overline{C} \overline{D}} \cdot \overline{ABC}$$

Realization using NAND gate:



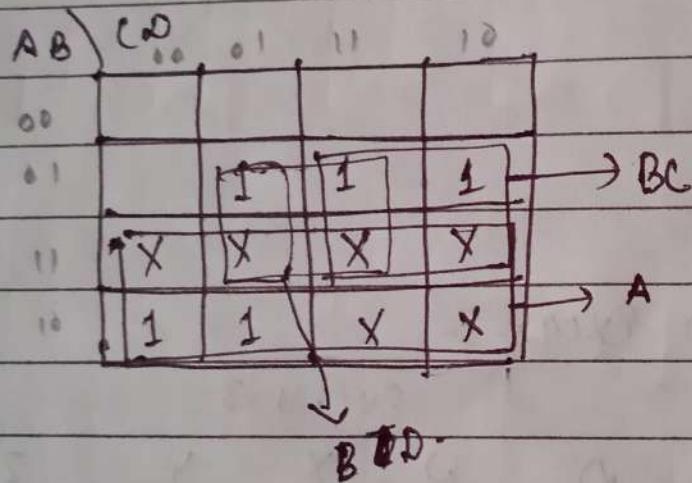
Q.N. 3.

A. Ans. 8-4-2-1 to Excess-3.

BCD (8421)				Excess 3				
A	B	C	D	W	X	Y	Z	
0	0	0	0	0	0	1	1	
0	0	0	1	0	1	0	0	
0	0	1	0	0	1	0	1	
0	0	1	1	0	1	1	0	
0	1	0	0	0	1	1	1	
0	1	0	1	1	0	0	0	
0	1	1	0	1	0	0	1	
0	1	1	1	1	0	1	0	
1	0	0	0	1	0	1	1	

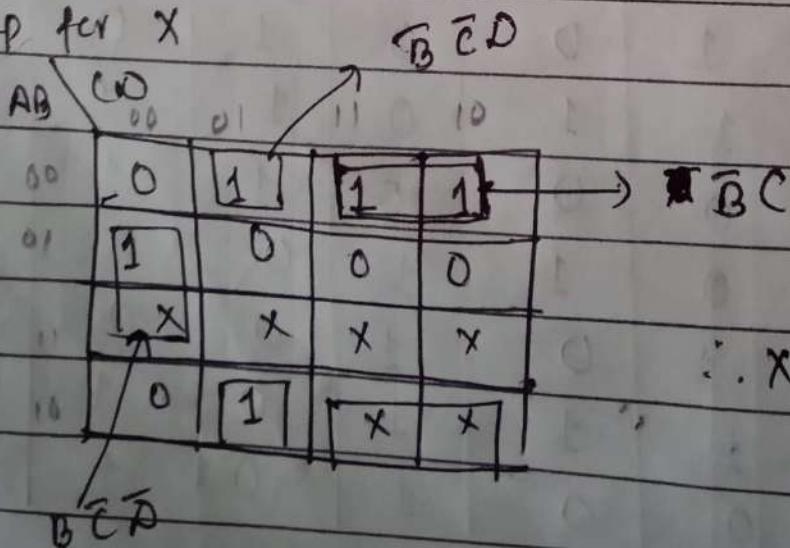
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

K-Map for W.



$$\therefore W = A + BC + B'D$$

K-Map for X



$$\therefore X = \overline{B}C + B\overline{C}\overline{D} + \overline{B}\overline{C}D$$

K.Map for Y.

AB \ CD	00	01	11	10
00	1	0	1	0
01	1	0	1	0
11	x	x	x	x
10	1	0	x	x

$\downarrow \bar{C} \bar{D}$. $\downarrow CD$

$$\therefore Y = CD + \bar{C} \bar{D}.$$

K.Map for Z.

AB \ CD	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	x	x	x	x
10	1	0	x	x

$\downarrow \bar{C} \bar{D}$. $\downarrow CD$

$$\therefore Z = \bar{C} \bar{D} + C \bar{D}.$$

Realization:

A B C D



C

D



\bar{BC}

D_{BD}

$$W = A + \bar{B}C + \bar{B}D$$

\bar{BC}

$\bar{B}\bar{C}\bar{D}$

$\bar{B}\bar{C}D$

X

\bar{CD}

$\bar{C}\bar{D}$

$$Y = CD + \bar{C}\bar{D}$$

$\bar{C}\bar{D}$

$\bar{C}\bar{D}$

$$Z = \bar{C}\bar{D}$$

B. Ans.

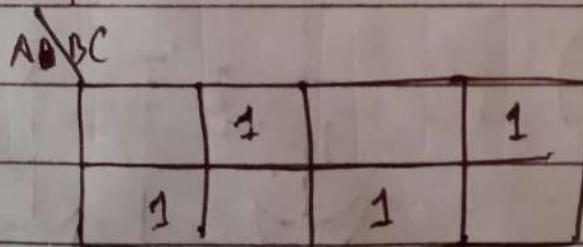
The fourth table of full subtractor is :

Inputs			Outputs	
A	B	Bin (c)	Difference (D_i)	Borrow (B_i)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1.	1	1.

Here. $= \text{Em}(1, 2, 4, 7)$

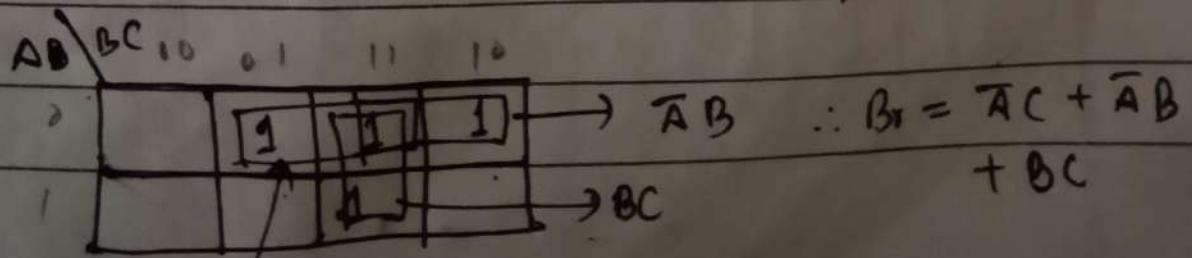
We have $D_1 = \overline{A}BC + \overline{ABC} + A\overline{B}\overline{C} + ABC$

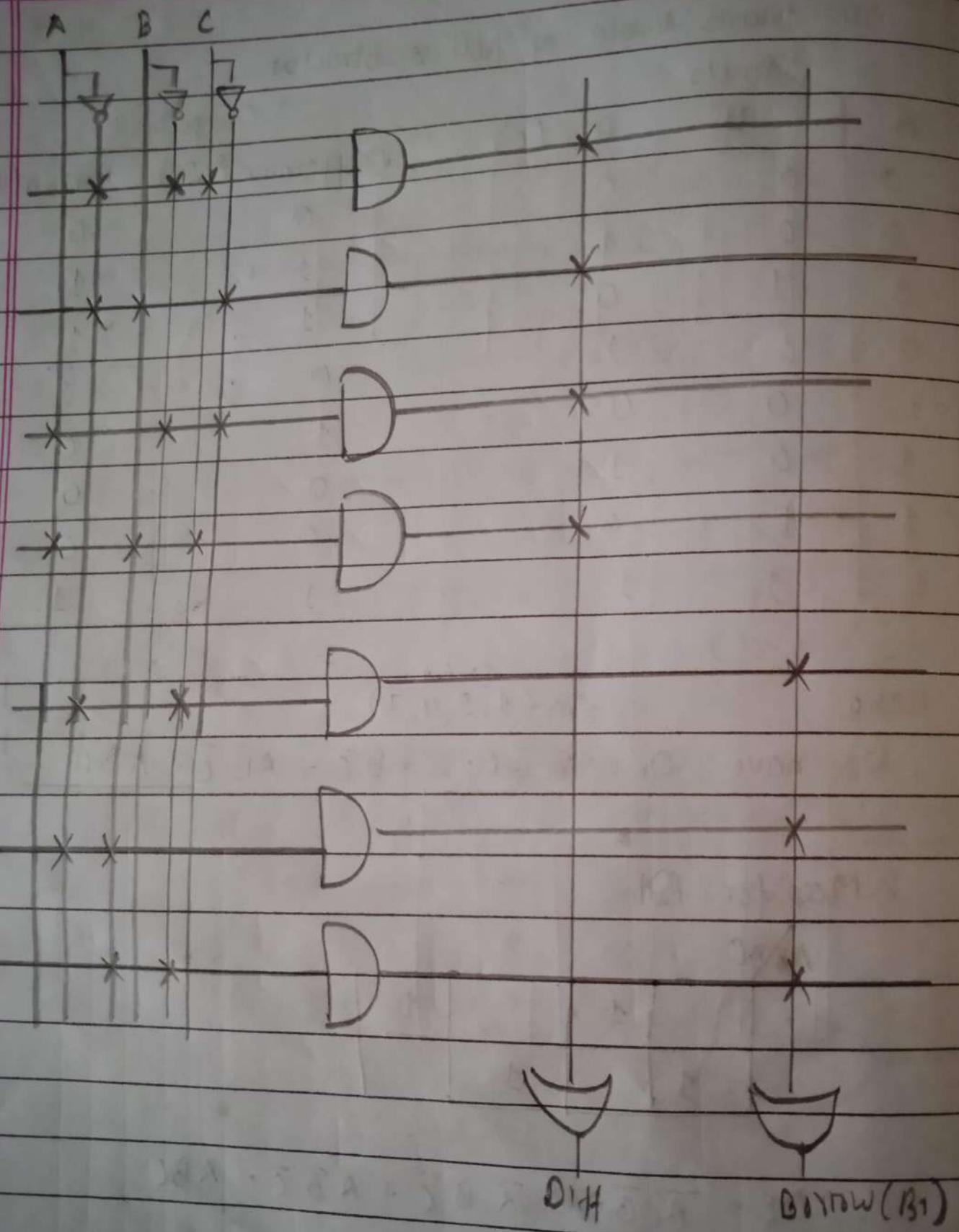
R. Map for RDi.



$$\therefore D_i = \overline{A} \overline{B} C + \overline{A} B \overline{C} + A \overline{B} \overline{C} + ABC$$

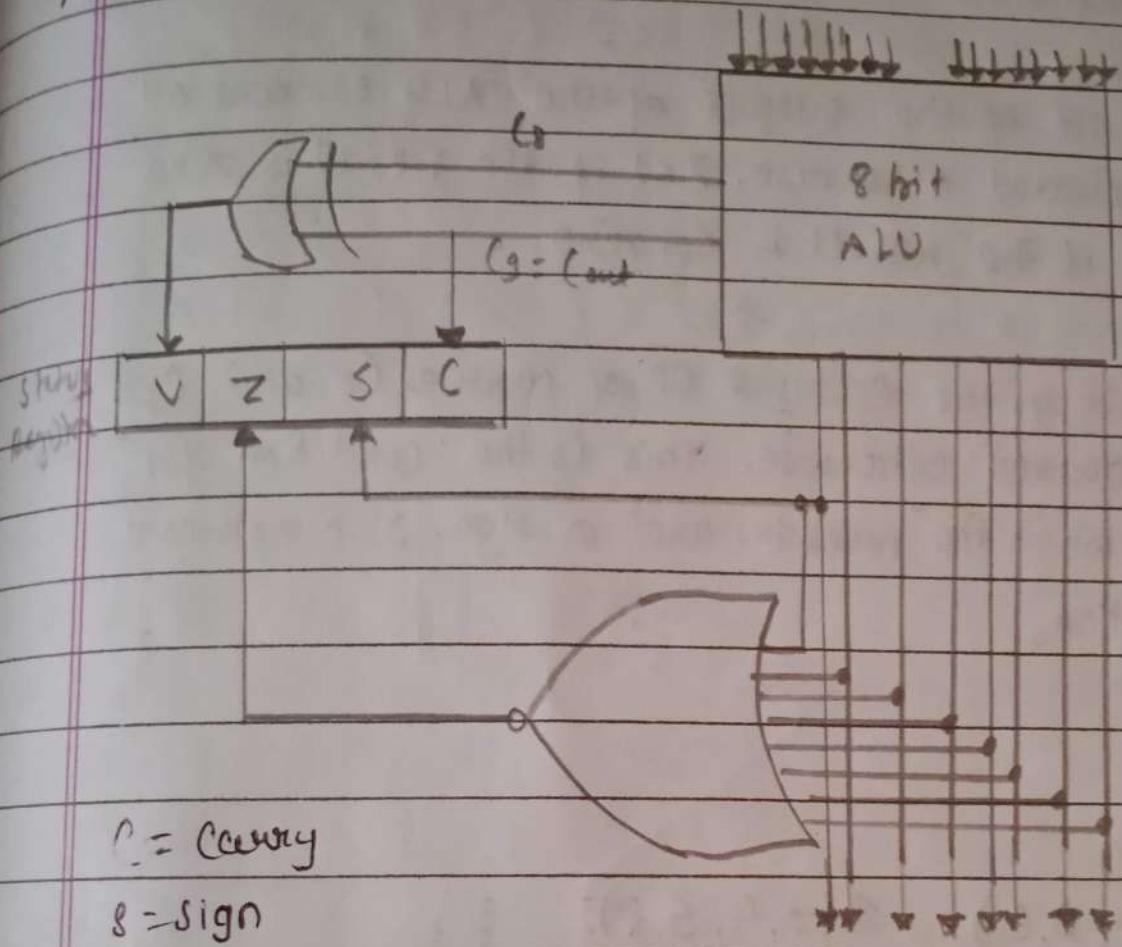
k. Map for, B_1 . We have, $B_1 = \text{EM}(1, 2, 3, 7)$.





Q.N.4.

A. Ans.



The four status bits or flag bits are symbolized by C, S, Z and V. The bit are set or cleared as a result of an operation performed in the ALU.

Operation steps:

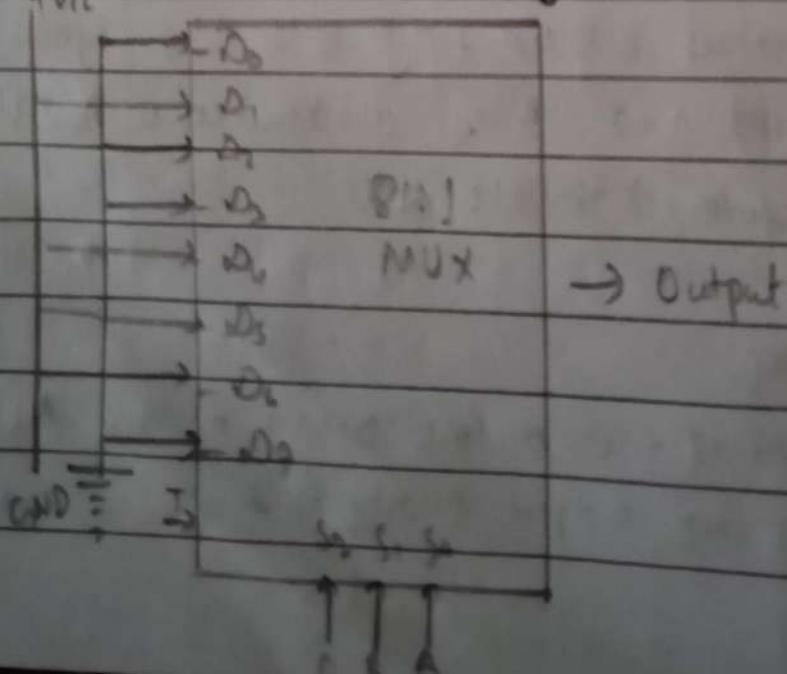
1. Bit C is set if the output carry of the ALU is 1. It is cleared if the output carry is 0.

2. Bit S is set if the highest-order bit of the result in the output of the ALU (the sign bit) is 1. It is cleared if the highest order bit is 0.
3. Bit Z is set if the output of the ALU contains all 0's and cleared otherwise, Z=1 if the result is zero and Z=0 if the result is nonzero.
4. Bit V is set if the exclusive OR of carries C₈ and C₉ is 1, and cleared otherwise. This is the condition for overflow when the numbers are in sign-2's complement representation.

B. Ans.

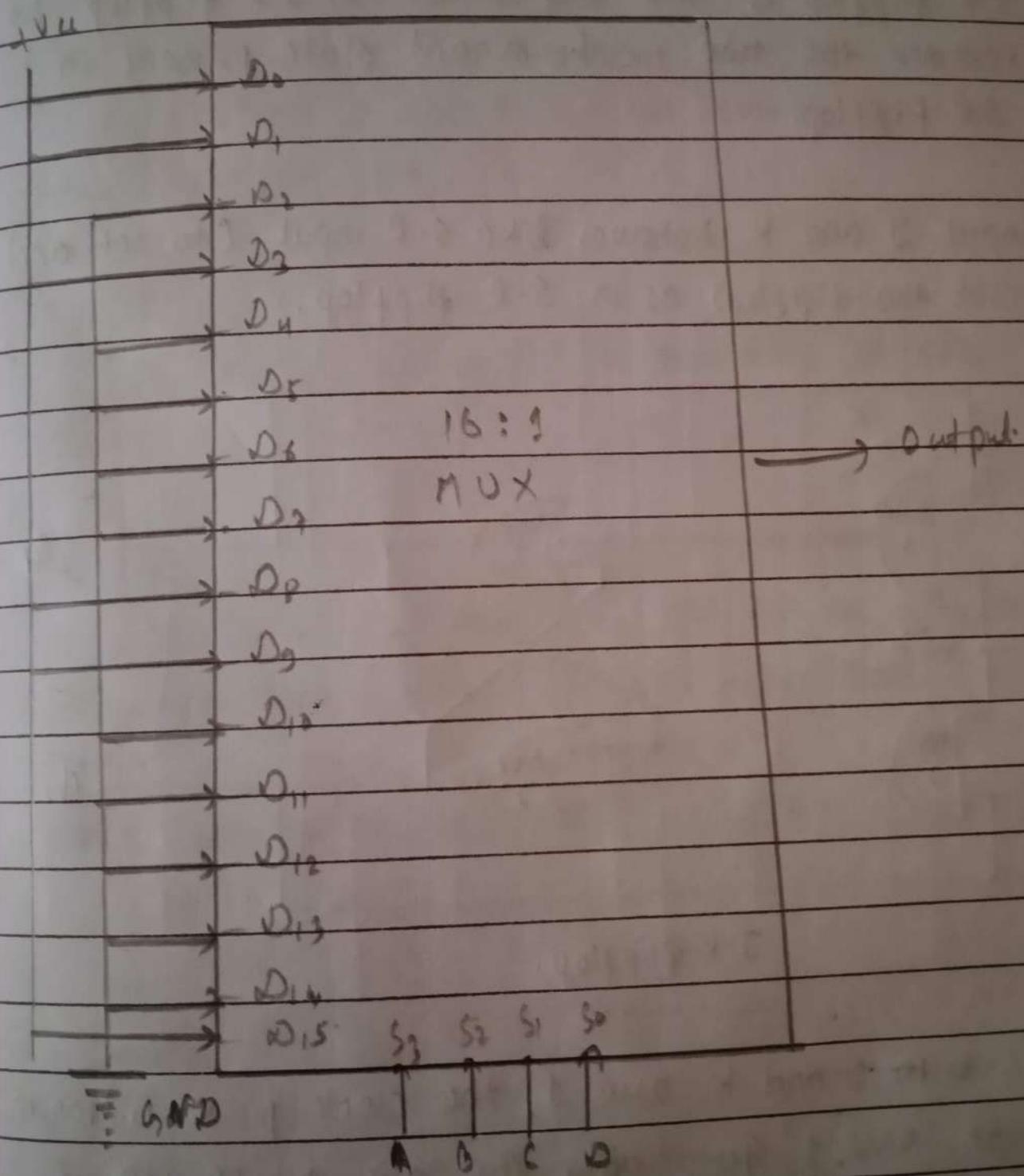
$$i. F(A, B, C) = \Sigma(1, 4, 5, 6).$$

Here the function has three variables. So, It can be implemented by using 8:1 MUX.



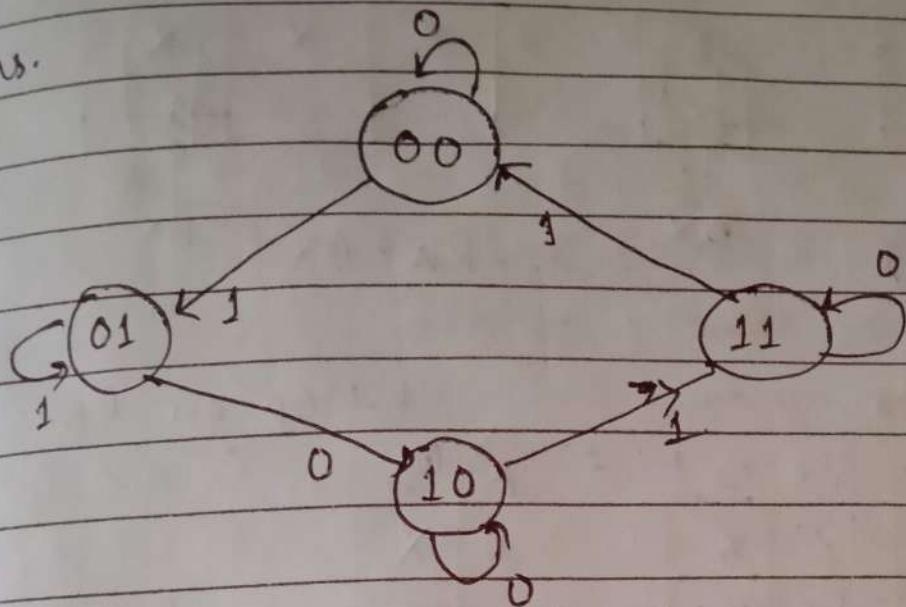
$$\text{ii. } F(A, B, C, D) = \Sigma(0, 1, 3, 8, 9, 15)$$

Here, the function has four variables. So, It can be implemented by using 16:1 MUX.



Q.N.5.

A. Ans.



Plotting the given information of state diagram into state table.

Present state (A'B')	Input (X)	Nextstate (A'B')	SR Input		Output (Y)
			S _A	R _B	
00	0	00	0X	0X	
00	1	01	0X	10	
01	0	10	10	X0	
01	1	01	0X	X0	
10	0	10	X0	0X	
10	1	11	X0	10	
11	0	11	X0	X0	
11	1	00	X01	01	

Excitation Table of S-R flipflop.

Q _t	Q _{t+1}	S	R
0	0	0	1
1	0	1	0

K-Map for S_A

		Bx		00		01		11		10	
		A	\bar{A}	00	01	11	10	00	01	11	10
		0		X	X		1		X	X	X
		1				X					

$$\therefore S_A = B\bar{X}$$

 $B\bar{X}$

$$\therefore R_A = Bx$$

 Bx

K-Map for S_B

		Bx		00		01		11		10	
		A	\bar{A}	00	01	11	10	00	01	11	10
		0		1	X	X					
		1		1	X						

$$\therefore S_B = \overline{B}X$$

 $\overline{B}X$

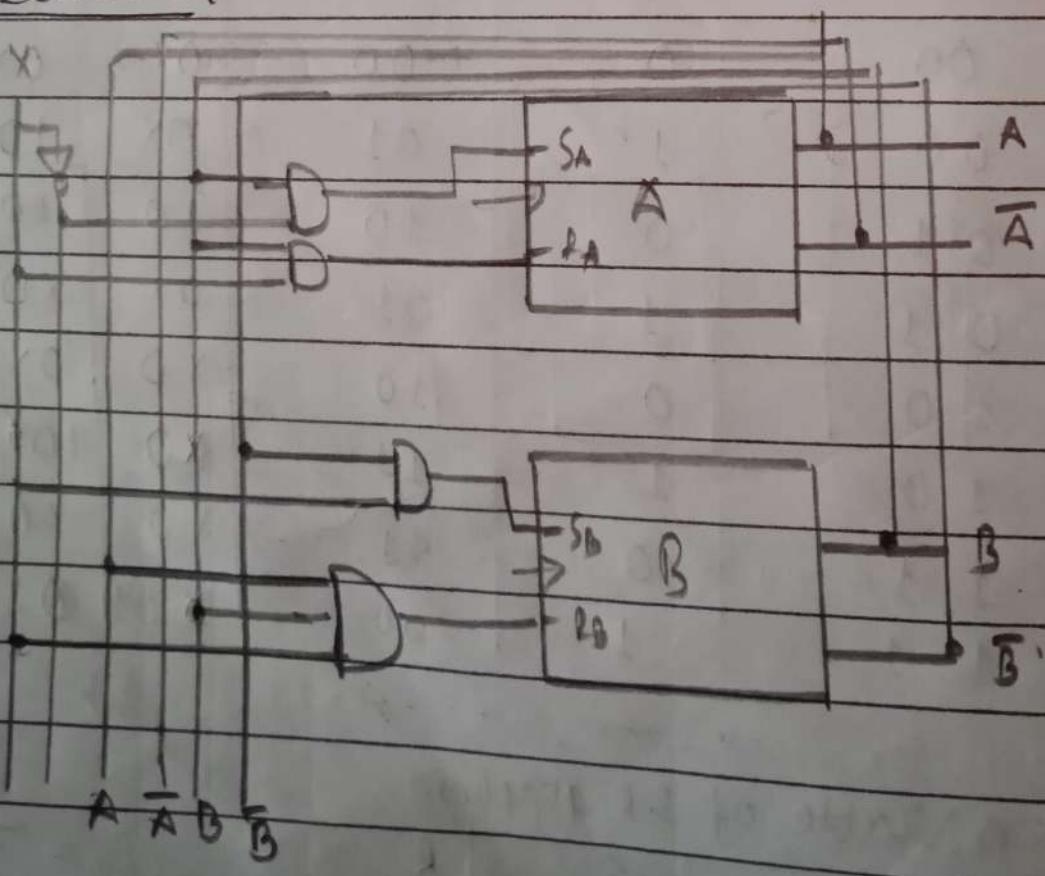
K-Map for R_B .

		Bx		00		01		11		10	
		A	\bar{A}	00	01	11	10	00	01	11	10
		0		X							
		1		X							

$$\therefore R_B = ABX$$

 ABX

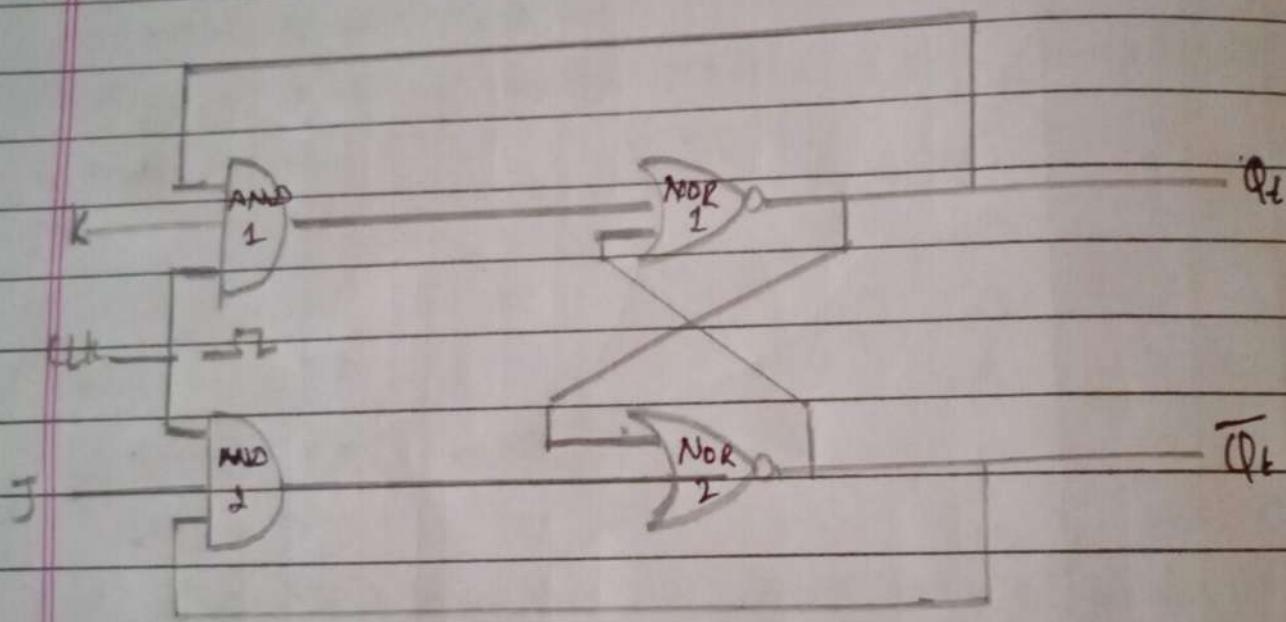
Realization:



5. B. Ans.

J-K flip flop:

- J-K flip flop is the refinement of S-R flip flop to remove the two indeterminant state present in S-R flip flop.
- Input J and K behaves like S-R input (to set and reset the flip flop) as in S-R flip flop.



J-K flip flop.

- When both J and K are 1, the clock pulse is transmitted through 'AND 1' gate only, the one whose input is connected to the flip flop output, which is presently equal to 1. Thus if $Q_t = 1$ upper AND gate becomes enabled under the application of clock pulse.

Case I:

If clock pulse (C_p) = 1, $J=0$, and $K=0$ then o/p of flip flop remains in its previous state.

Case II:

If $C_p = 1$, $J=0$ and $K=1$, then o/p of flip flop changes to clear state.

Case III:

If $C_p = 1$, $J=1$ and $K=0$ then the set state is reached.

Case IV:

If $C_p = 1$, $J=1$ and $K=1$, the o/p of flip flop will be complement of the present value / state Q_t .

The characteristic table of J-K flip flop is shown below:

Input			Output
Q_t	J	K	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

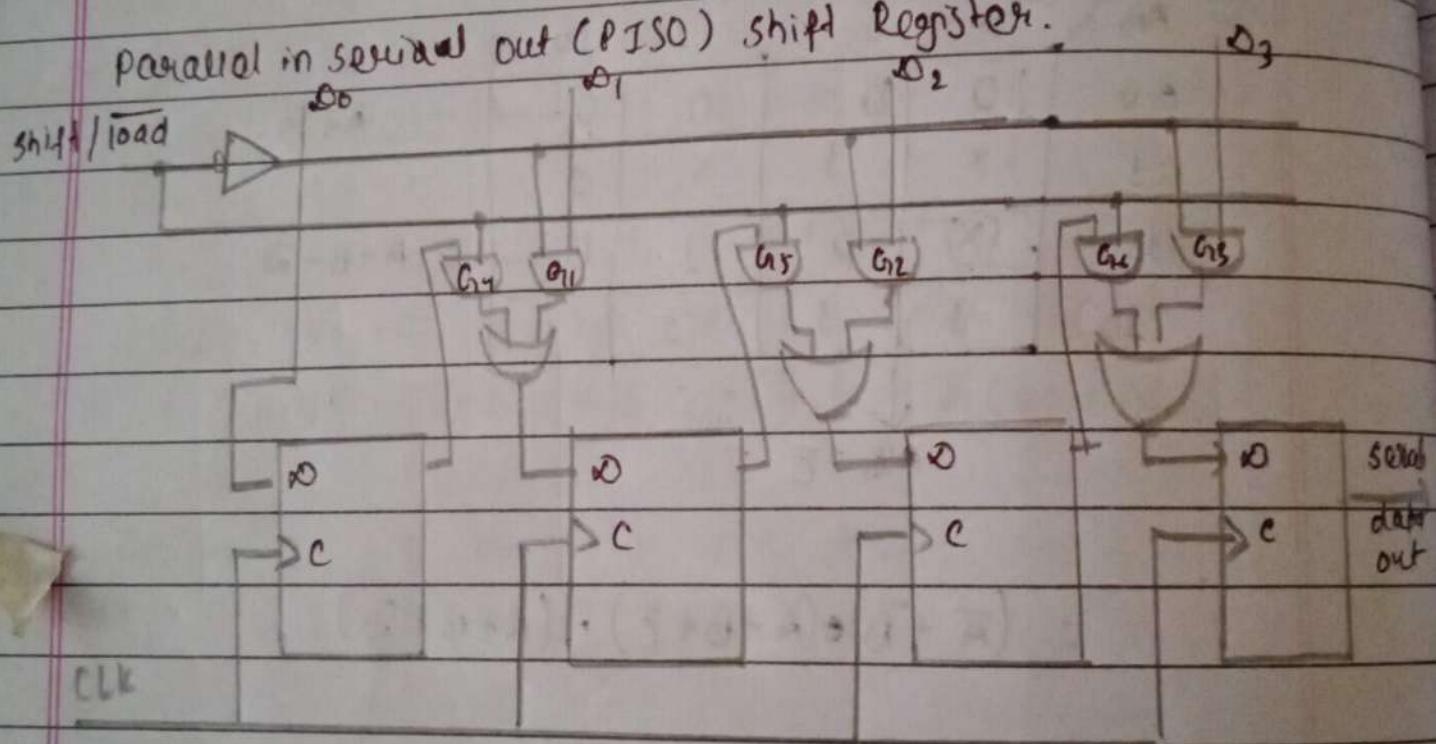
Q.N.6.

A. AN.

Shift Register:

Shift registers are a type of logic circuits closely related to counters. They are basically used for storage and transfer of digital data.

parallel in serial out (PISO) shift register.



Load Mode:

When the shift/load line is low, the AND gates G₁, G₂ and G₃ become active. They will pass D₀, D₁, and D₂ bits to the corresponding flip flops.

On the low going edge of clock, the binary inputs D₀, D₁, D₂ and D₃ will get loaded into corresponding flip flop. Thus, parallel loading takes place.

Shift Mode:

- When the shift / load mode is high, the AND gates G₁, G₂ and G₃ become inactive. Hence parallel loading of data becomes impossible.
- But AND gates G₄, G₅ and G₆ become active. Therefore the shifting of data from left to right bit by bit on application of clock pulses.
- Thus the parallel in serial out operation takes place.

B. AN -

No. of required flipflops = 3, for T-flipflop.

Excitation table of T-flipflop.

Q_t	Q_{t+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Since, No. of states = $2^3 = 8$, Max count = $8 - 1 = 7$.

PRESENT STATE (P.S)	NEXT STATE (N.S)	T _A	T _B	T _C
------------------------	---------------------	----------------	----------------	----------------

A	B	C	A'	B'	C'		
0	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1
0	1	0	0	1	1	0	0
0	1	1	1	0	0	1	1
1	0	0	1	0	1	0	0
1	0	1	1	1	0	0	1
1	1	0	1	1	1	0	0
1	1	1	0	0	0	1	1

From table, $T_C = 1$.

K-map for T_A .

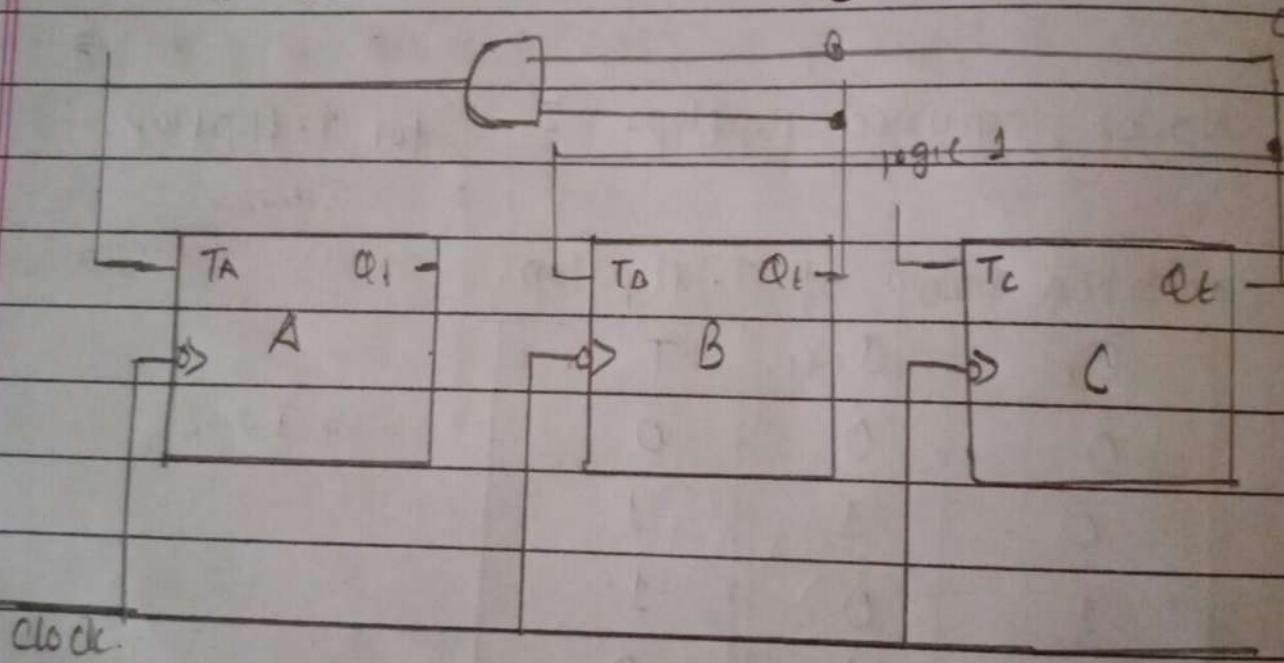
A \ BC	00	01	11	10
0	1			
1		1		

$$\therefore T_A = BC$$

K-map for T_B .

A \ BC	00	01	11	10
0		1	1	
1		1	1	

$$T_B = C$$



Q.N.7.

A. Computational Logic Design Procedure :

The design procedure for combinational logic ckt starts with the problem specification and comprises the following steps:

1. Determine required number of inputs and outputs from the specification.
2. Define the truth table for each of the outputs based on their relationships to the input.
3. Similarly the Boolean expression for each output. Using K-map for Boolean Algebra.
4. Draw a logic diagram that represents the simplified Boolean expression. Verify the design by analysing or simulating the circuit.

B. Johnson Counter :

- Johnson counter is a reverse ring counter or modified ring counter in which the output from the last flip flop is inverted and fed back as an input to the first.
- Also known as Inverse Feedback counter or Twisted Ring counter.
- The Mod of the Johnson counter is ' 2^n ', n is the bit size of the counter.

Advantages:

- More output as compared to ring counter.
- It has the same number of flip flop but it can count twice the number of states the ring counter can count.
- It only needs half the number of flip flops compared to the standard ring counter for the same MOD.

Disadvantages:

- Only 8 of the 15 states are being used.
- It doesn't count in binary sequence.

Q.N.1.

A. Ans.

A digital system is a system which deals with discrete signal. The input and output of this system is two binary value which is 0 and 1. Examples of digital systems are mobile phones, radio, and many more.

I prefer Digital system against analog because of following reasons:

- Digital signal doesn't carry noise as compared to analog system.
- Digital system has ability to transfer more data as compared to analog.
- Digital system has greater accuracy than that of analog system.
- Digital system turns out to be best for long distance data transmission, as there won't be unwanted disturbance.

B. Ans.

$$i. (111001)_2 - (11011)_2$$

Ans. (T-1) means subtraction using 1's complement
So, 1's complement of 11011 = 00100.

Adding minuted with 1's complement

$$\begin{array}{r} 111001 \\ + \cancel{00100} \\ \hline 11101 \end{array}$$

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since we get carry^{out} as 1 so adding it to
LSB.

$$\begin{array}{r} 1 \ 1 \ 1 \ 0 \ 1 \\ + \quad \quad 1 \\ \hline 1 \ 1 \ 1 \ 1 \ 0 \end{array}$$

$$\therefore (111001)_2 - (11011)_2 = (11110)_2.$$

ii. $(2321)_{10} - (8301)_{10}.$

so, $(7-1)$'s complement is $(10-1) = 9$'s complement
 9 's complement of subtrahend is,

$$\begin{array}{r} 9 \ 9 \ 9 \ 9 \\ - 8 \ 3 \ 0 \ 1 \\ \hline 1 \ 6 \ 9 \ 8 \end{array}$$

Now,

Adding with minuted.

$$\begin{array}{r} 2 \ 3 \ 1 \ 2 \ 1 \\ + 1 \ 6 \ 9 \ 8 \\ \hline 4 \ 0 \ 1 \ 9 \end{array}$$

As there is no carry, result is -ve and in 9 's complement form. So, answer in decimal form will be
~~5980~~ 5980

$$\therefore (2321)_{10} - (8301)_{10} = -5980$$

C. Ans.

Date / /
Page No.

Weighted code are such code in which each digit position has a weight or value. Whereas ^{In} Non-weighted code or reflected code there is no positional weight that means the positions of digits don't determine their value.

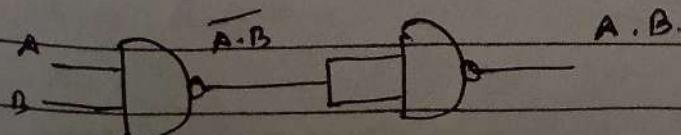
Gray code is called reflected code Because the position of digit in the gray code doesn't determine the weight or value of the number.

Q.N.2.

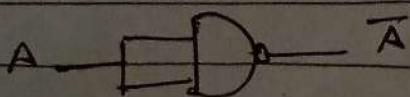
A. Ans. NAND & NOR gates in logic circuits are known as Universal gates. This is so because through them we can construct our basic logic gates.

NAND gates as Universal gates.

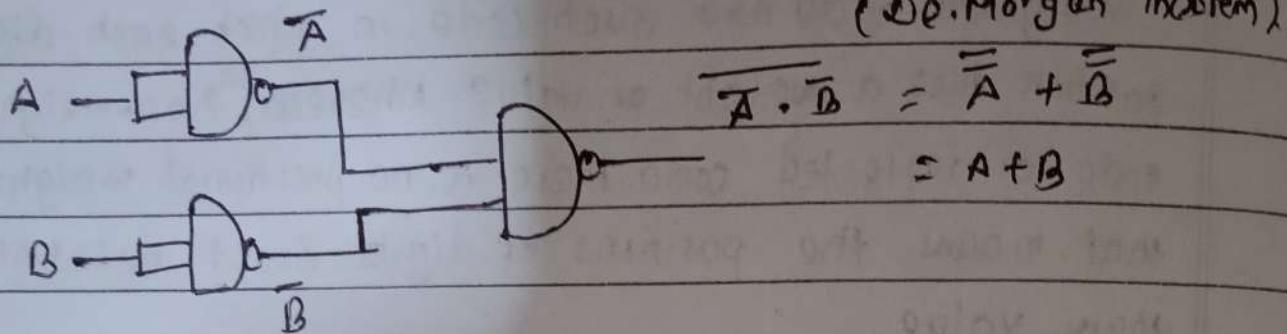
- AND Gate.



- NOT Gate

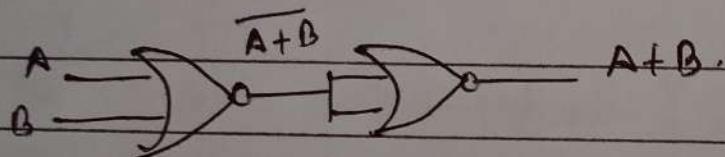


- OR Gate



NOR Gates as universal gates.

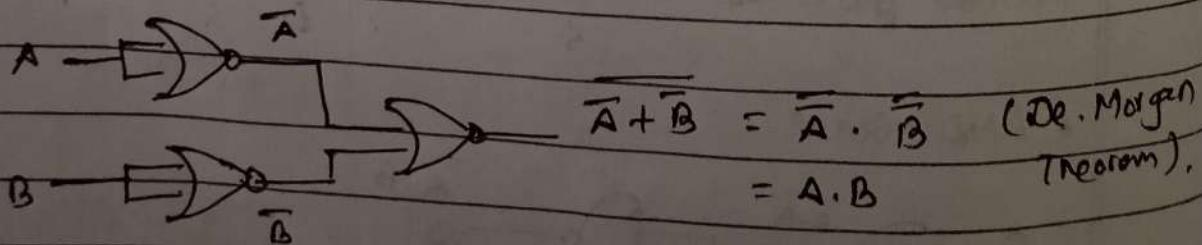
- OR Gate.



- NOT Gate.



- AND Gate.



In this way, from NAND and NOR gates we can construct basic gates. So, NAND and NOR gates are called universal gates.

B Ans.

Given logical Expression,

$$F(A, B, C, D) = \bar{A}B + BD + \bar{A}\bar{D} + \bar{B}\bar{D}$$

Converting the given expression into standard form.

$$\begin{aligned} F(A, B, C, D) &= \bar{A}B(C+\bar{C})(D+\bar{D}) + BD(A+\bar{A})(C+\bar{C}) \\ &\quad + \bar{A}\bar{D}(B+\bar{B})(C+\bar{C}) + \bar{B}\bar{D}(A+\bar{A})(C+\bar{C}) \end{aligned}$$

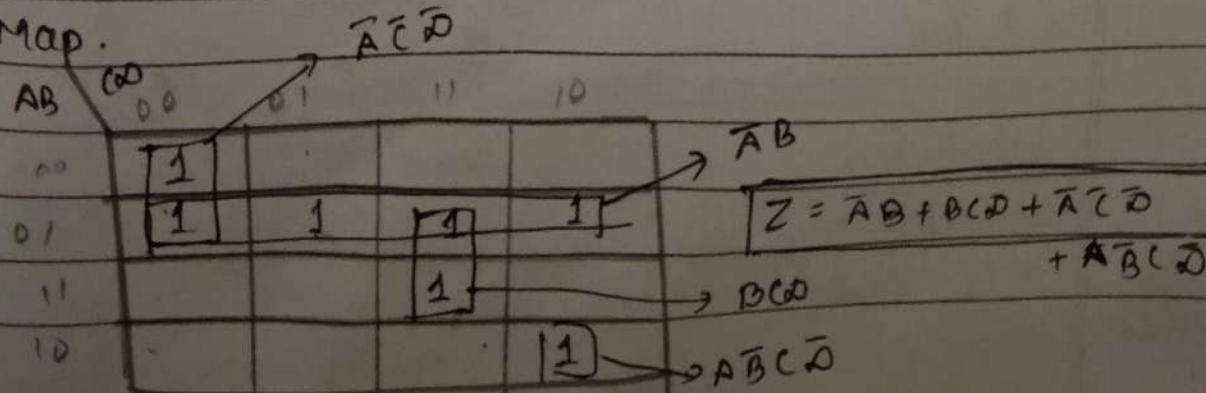
$$\begin{aligned} &= (\bar{A}BC + \bar{A}B\bar{C})(D+\bar{D}) + (ABD + \bar{A}B\bar{D}) \\ &\quad (C+\bar{C}) + (\bar{A}B\bar{D} + \bar{A}\bar{B}\bar{D})(C+\bar{C}) + \\ &\quad (A\bar{B}\bar{D} + \bar{A}\bar{B}\bar{D})(C+\bar{C}) \end{aligned}$$

$$\begin{aligned} &= (\bar{A}BCD + \bar{A}B\bar{C}\bar{D}) + (ABC\bar{D} + \bar{A}B\bar{C}D) \\ &\quad + (\bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D}) + (A\bar{B}\bar{C}\bar{D} + \\ &\quad \bar{A}\bar{B}\bar{C}D) \end{aligned}$$

$$\begin{aligned} &= \overline{\underset{2}{A}} \overline{\underset{4}{B}} \overline{\underset{15}{C}} \overline{\underset{5}{D}} + \overline{\underset{4}{A}} \overline{\underset{11}{B}} \overline{\underset{10}{C}} \overline{\underset{5}{D}} + \\ &\quad \overline{\underset{6}{A}} \overline{\underset{0}{B}} \overline{\underset{10}{C}} \overline{\underset{5}{D}} + \overline{\underset{11}{A}} \overline{\underset{0}{B}} \overline{\underset{10}{C}} \overline{\underset{15}{D}}. \end{aligned}$$

$$= \Sigma m(0, 4, 5, 6, 7, 10, 15)$$

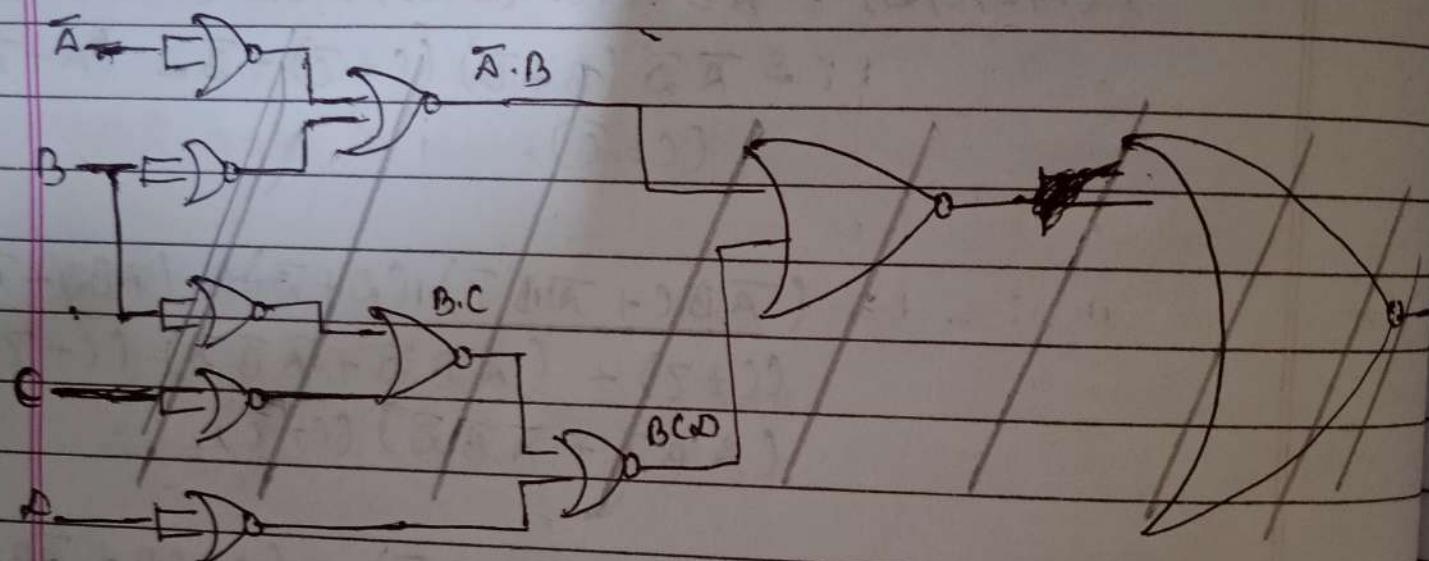
K.Map.



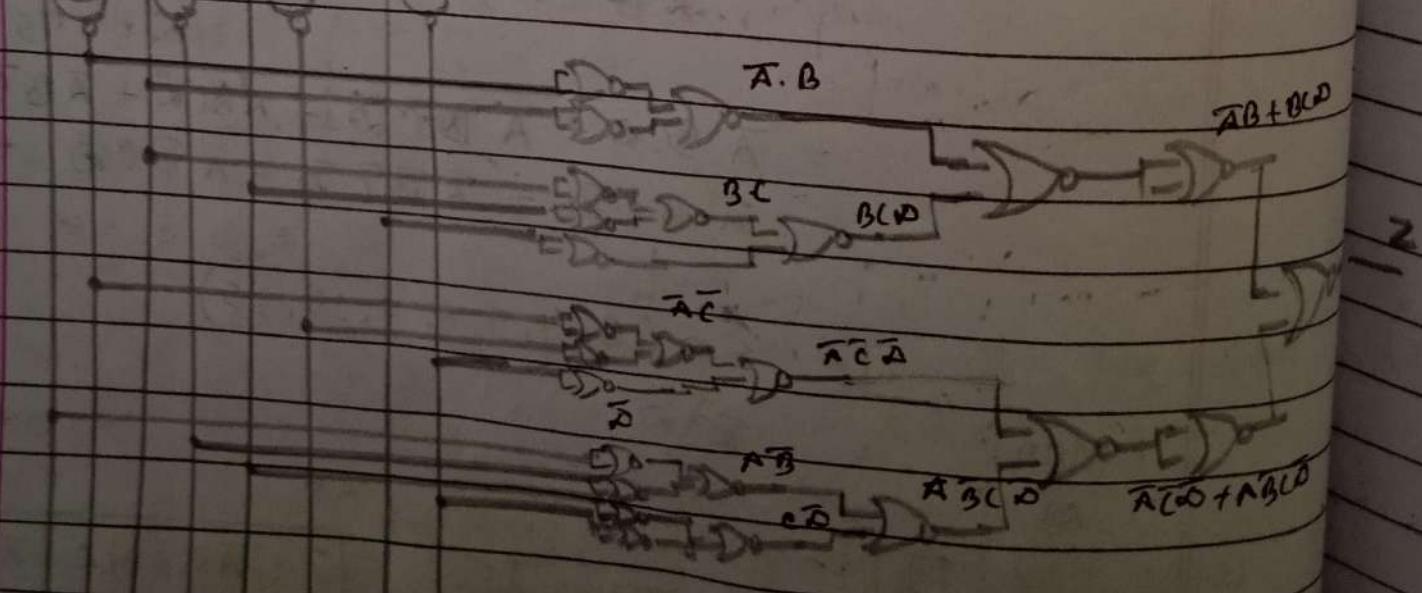
From K-Map we got,

$$Z = \overline{A}B + BC\bar{D} + \overline{A}\overline{C}\bar{D} + A\overline{B}C\bar{D}$$

Realizing using NOR gate (2 input) only.



A B C Z



Q.N.3.

A. Ans.

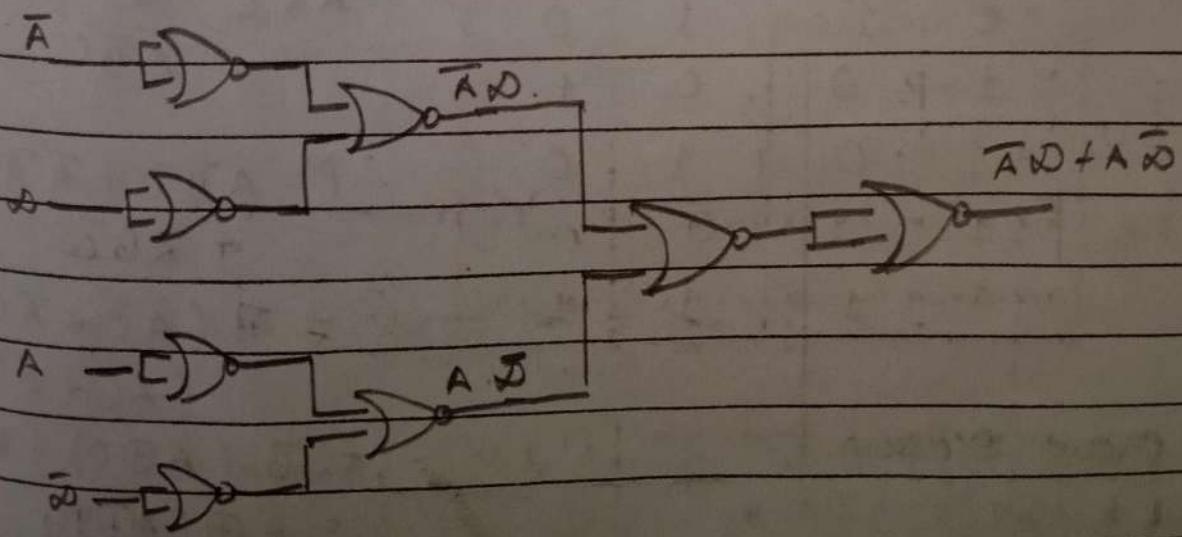
$$\text{Given, } f(A, B, C, D) = \Sigma m(1, 5, 8, 12)$$

$$d(A, B, C, D) = \Sigma m(3, 7, 10, 11, 14, 15).$$

AB	CD	01	11	10	00	
00		1	X			\overline{AD}
01		1	X			
11	1		X	X		$A\overline{D}$
10	1		X	X		

$$\therefore Z = \overline{AD} + A\overline{D}.$$

Realization using NOR gate.



B. Ans.

Parity bits are the extra bits that are added on the message to check its validity at the receiving point.

3 bit parity generator.

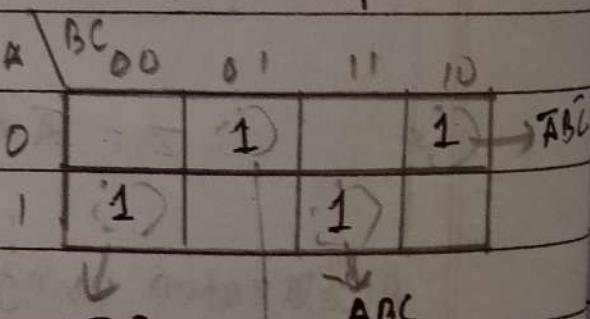
Let three inputs be represented by A, B and C and output by P.

So we have:

Truth table

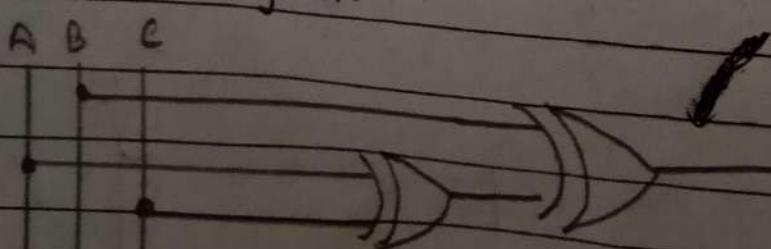
A	B	C	P(even)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

K-Map.



$$\begin{aligned} \therefore P &= A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC \\ &\quad + \bar{A}B\bar{C} \\ &= \bar{B}(A\bar{C} + \bar{A}C) + B(C + \bar{A}\bar{C}) \end{aligned}$$

Circuit Diagram.



$$\begin{aligned} &= \bar{B} \cdot (A \oplus C) + B(A \oplus C) \\ &= B \oplus (A \oplus C). \end{aligned}$$

4 bit parity generator.

Let four inputs be represented by A, B, C, D and output by P.

so we have:

Truth table.

A	B	C	D	P (even)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

K. Map.

AB	CD			
	00	01	11	10
00		(1)		(1)
01	(1)		1	
11		(1)		(1)
10	(1)		1	

$$\therefore P = \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}C\overline{D} + \overline{ABC}\overline{D} + \overline{ABC}D + AB\overline{C}D + ABC\overline{D}$$

$$= \overline{A}\overline{B}(\overline{C}D + C\overline{D}) + \overline{AB}(\overline{C}D + C\overline{D}) + AB(CD + C\overline{D}) + A\overline{B}(\overline{C}D + CD)$$

$$= \overline{A}\overline{B}(C \oplus D) + \overline{AB}(C \oplus D) + AB(C \oplus D) + A\overline{B}(\overline{C} \oplus D)$$

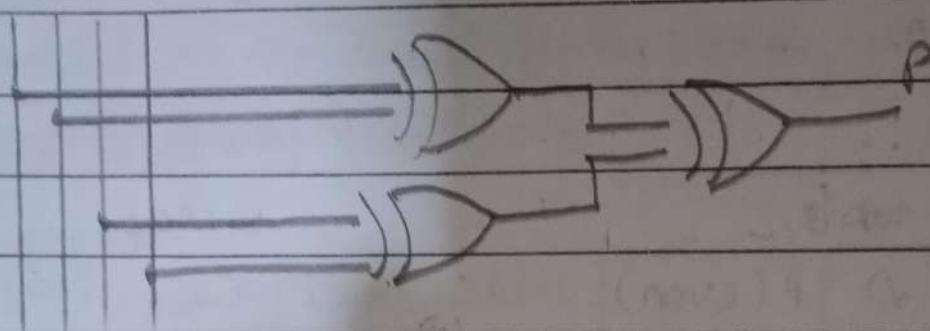
$$= (C \oplus D)(\overline{A}\overline{B} + AB) + (\overline{C} \oplus D)(\overline{AB} + A\overline{B})$$

$$= (C \oplus D)(A \oplus B) + (\overline{C} \oplus D)(\overline{A} \oplus B)$$

$$= (A \oplus B) \oplus (C \oplus D)$$

Circuit Diagram:

A B C D



Q. N. 4.

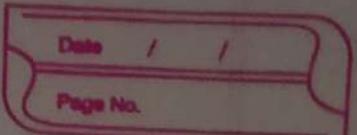
A. Ans. Let the 3 bit inputs be represented by, A, B, and C.

Inputs.			Outputs							Decimal.
A	B	C	x_5	x_4	x_3	x_2	x_1	x_0		
0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1	1
0	1	0	0	0	0	1	0	0	4	4
0	1	1	0	0	1	0	0	1	9	9
1	0	0	0	1	0	0	0	0	16	16
1	0	1	0	1	1	0	0	1	25	25
1	1	0	1	0	0	1	0	0	36	36
1	1	1	1	1	0	0	0	1	49	49

Truth table for the circuit.

Let's draw the k-map for simplification of circuit for all outputs (x_0, x_1, x_2, x_3, x_4 and x_5).

FOR IC0011 . K-map (new)
OR programmable



K-Map for X_5 .

(No Need to
make MAP + BY PLD as ROM)

A \ BC	00	01	11	10	
0					
1			1	1	→ AB

$$\therefore X_5 = AB$$

K-Map for X_4

A \ BC	00	01	11	10	
0					
1	1	1	1		

$$\therefore X_4 = A\bar{B} + AC$$

K-Map for X_3 .

A \ BC	00	01	11	10	
0	.		1		
1		1			

$$\therefore X_3 = A\bar{B}C + \bar{A}BC$$

$$= C((A\bar{B} + \bar{A}B))$$

$$= C(A \oplus B)$$

K-Map for X_2 .

A \ BC	00	01	11	10	
0				1	→ BC
1				1	

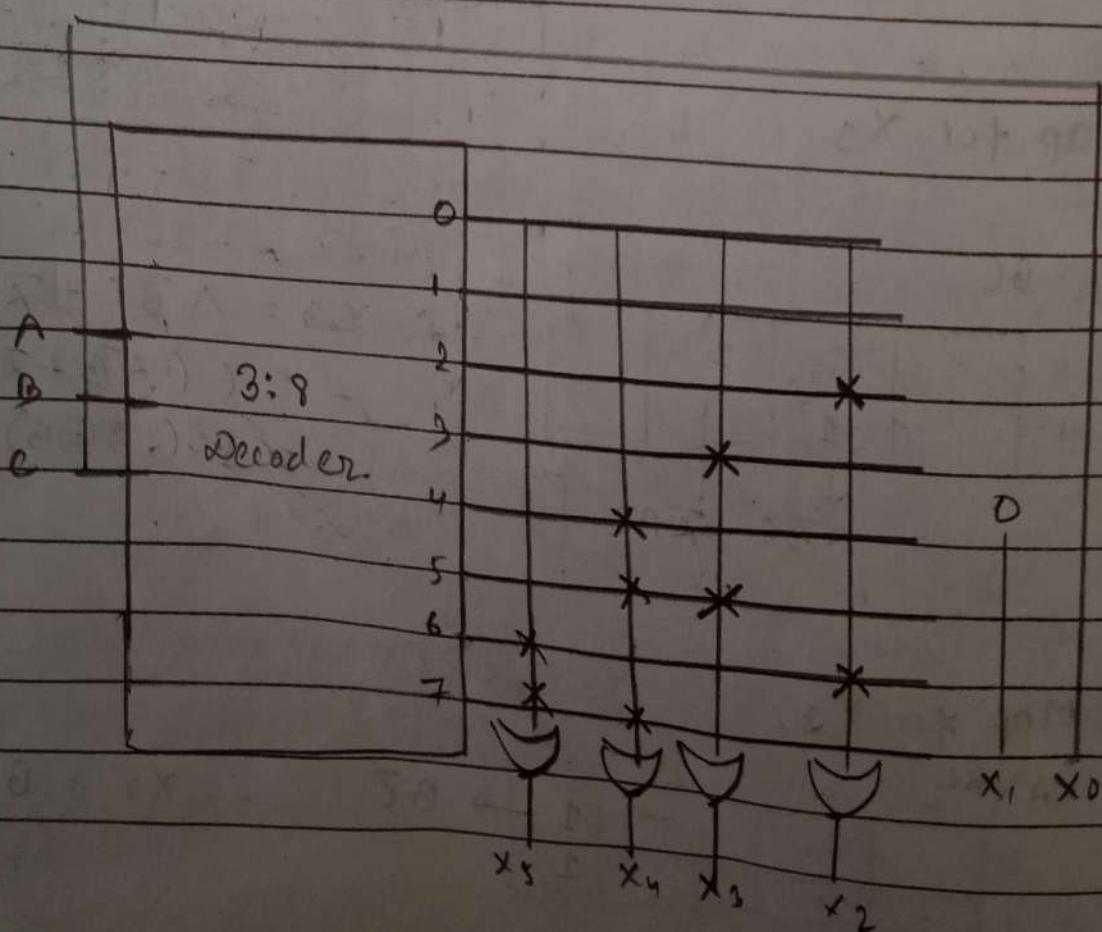
$$\therefore X_2 = B\bar{C}$$

K-Map for x_1

A	BC	00	01	11	10	
D						$x_1 = 0$
I						

K-Map for x_0

A	BC	00	01	11	10	
0		1	1			$\therefore x_0 = C$
1		1	1			



B. Ans.

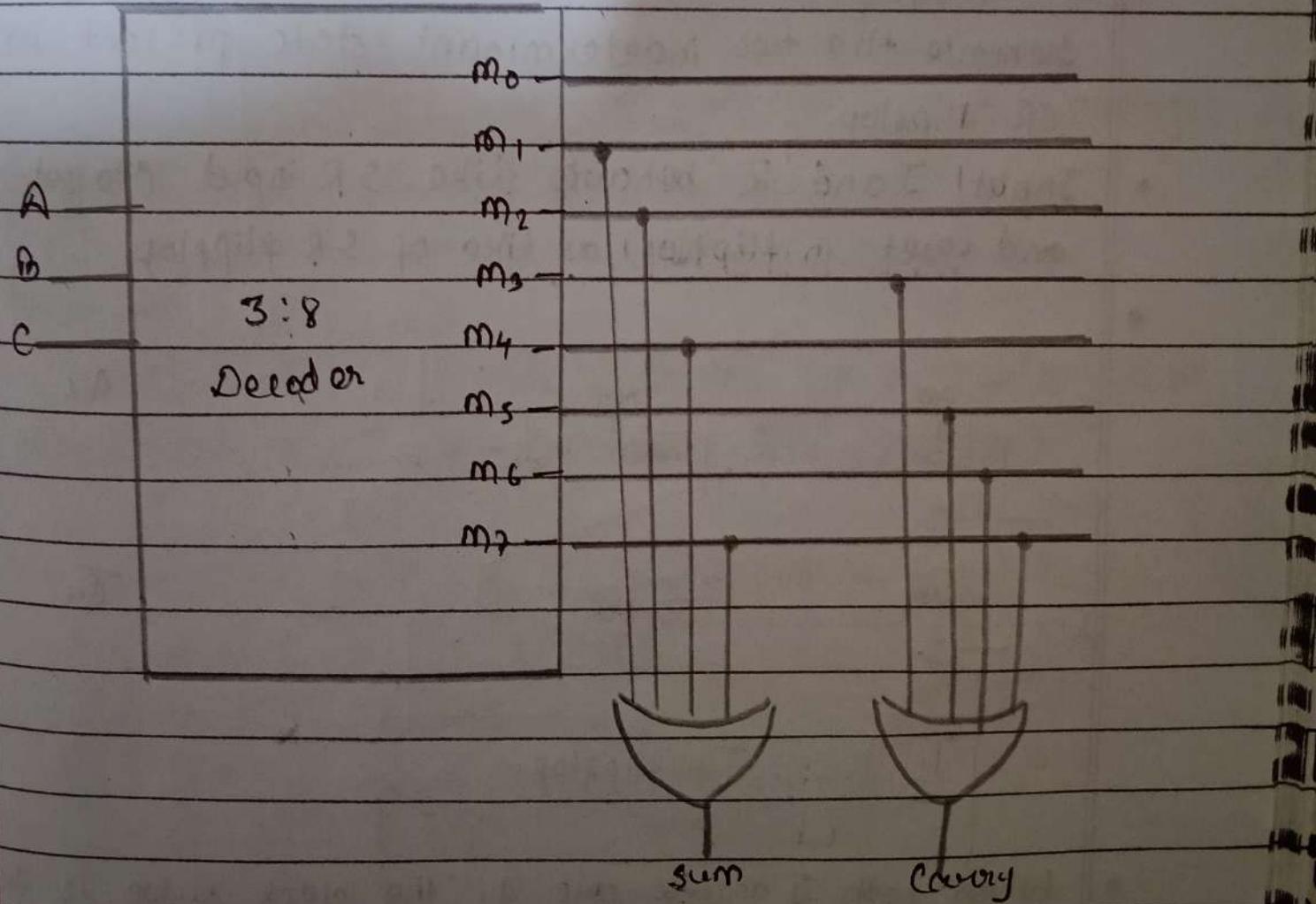
for full adder, no. of inputs = 3, (A, B, C, D)

Decoder size = 3:8

No. of outputs = 2 (sum, carry).

$$\text{sum} = \Sigma m(1, 2, 4, 7)$$

$$\text{carry} = \Sigma m(3, 5, 6, 7).$$

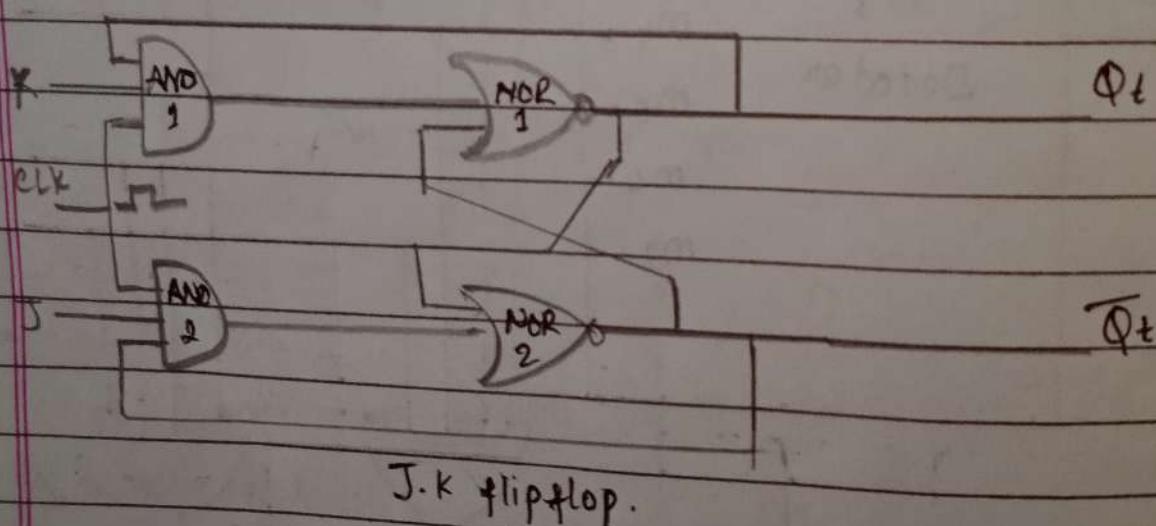


Q.N.5.

A. Ans. The significance of a flip-flop is that we can store 1 bit of information in it which helps in identifying two states either Q or \bar{Q} .

J-K flipflop.

- J-K flipflop is the refinement of S-R flipflop to remove the two indeterminant state present in SR flipflop.
- Input J and K behaves like S-R input (to set and reset in flipflop) as like of S-R flipflop.



J-K flipflop.

- When both J and K are 1, the clock pulse is transmitted through 'AND 1' gate only. Thus if $Q_t = 1$ upper AND gate becomes enabled under the application of clock pulse.

Case I :

If clock pulse (C_p) = 1, $J=0, K=0$, the o/p of flipflop remains in its previous state.

Case II :

If $C_p=1, J=0$ and $K=1$, the o/p of flipflop changes to clear state.

Case III :

If $C_p=1, J=1$ and $K=1$, the o/p of flipflop changes to reset state.

Case IV :

If $C_p=1, J=1$ and $K=0$, the o/p of flipflop will be complement of the present value Q_t .

The characteristic table of JK flipflop is shown below:

Q_t	Input J	K	Output Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Ans.
Plotting state diagram information into state table.

Present State (AB)	Input (X)	Next State (A'B')	T input TA TB	Output (Y)
00	0	00	0 0	0 0
00	1	01	0 1	1
01	0	10	1 1	1
01	1	01	0 0	0
10	0	10	0 0	0
10	1	11	0 1	1
11	0	11	0 0	0
11	1	00	1 1	1

Excitation table of T flipflop.

Q _t	Q _{t+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Solving using K.MAP.

For T_A.

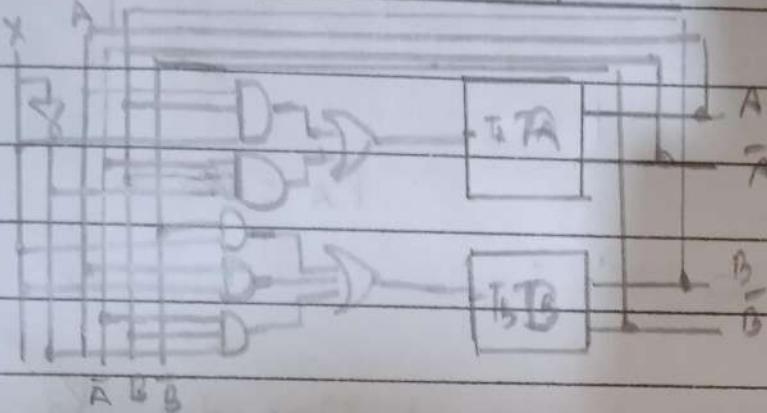
$$\begin{array}{c}
 \text{A} \backslash \text{B} \\
 \text{0} \quad \text{0} \quad \text{1} \quad \text{1} \\
 \text{0} \quad \text{1} \quad \text{1} \quad \text{0} \\
 \text{1} \quad \text{0} \quad \text{0} \quad \text{1} \\
 \text{1} \quad \text{1} \quad \text{1} \quad \text{0}
 \end{array}
 \xrightarrow{\text{K.MAP}}
 \begin{array}{c}
 \text{1} \\
 \text{1} \\
 \text{1} \\
 \text{0}
 \end{array}
 \Rightarrow \overline{A} \overline{B} X \quad \therefore T_A = A \overline{B} X + \overline{A} \overline{B} X$$

For To.

TB.		BX		AX	
A	BX	00	01	11	10
0		1			1
1		1	1		

$\therefore TB_0$

$$\therefore T_B = \overline{B}X + AX + \overline{A}\overline{B}\overline{X}.$$



Q.N.G.

A. Ans.

No. of required flipflops = 3., (J-K flipflops).

Excitation table of JK - flipflop

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

K-Map for J_A .

A	BC	00	01	11	10
0			1		
1		X	X	X	X
	BC				

$$\therefore J_A = BC$$

K-Map for K_A

A	BC	00	01	11	10
0		X	X	X	X
1		X	X	X	1
	BC				

$$\therefore K_A = \overline{B} \cdot \overline{C}$$

K-Map for J_B .

A	BC	00	01	11	10
0		1	X	X	
1		X	X	X	
	C				

$$\therefore J_B = C$$

K-Map for K_B

A	BC	00	01	11	10
0		X	X	1	0
1		X	X	X	X
	C				

$$\therefore K_B = C$$

K-Map for J_C

A	BC	00	01	11	10
0		1	X	X	1
1		X	X	X	X
	A				

$$\therefore J_C = \overline{A}$$

K-Map for K_C

A	BC	00	01	11	10
0		X	1	1	X
1		X	X	X	X
	C				

$$\therefore K_C = 1$$

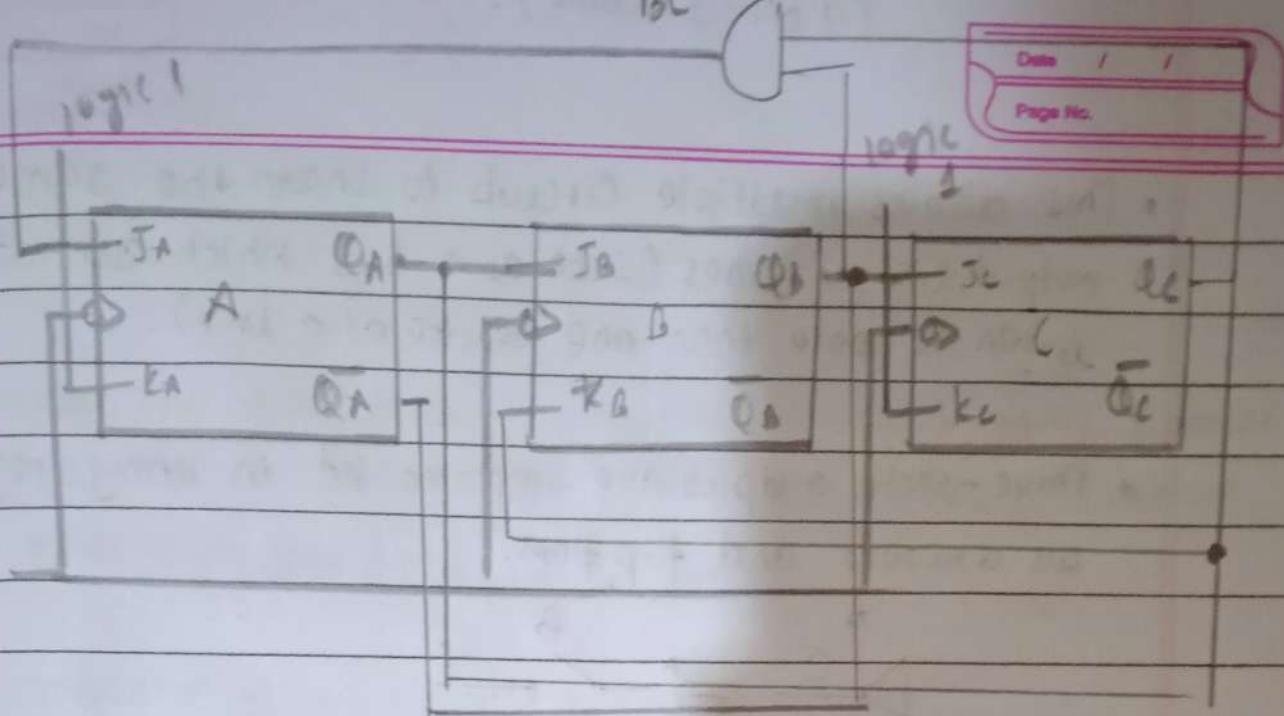


fig: Arrangement for MOD 5 Synchronous counter using J-K flip-flop.

Q.N.7.

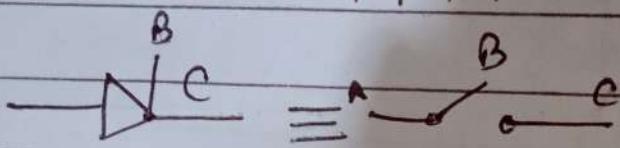
B. Tristate Logic:

- Tristate logic or 3 state logic allows an output port to assume a high impedance state, effectively removing the output from the circuit, in addition to the 0 and 1 logic levels.

(4 bit = 1 Nibble).

Date	/	/
Page No.		

- This allows multiple circuits to share the same output line or lines (such as a bus which cannot listen to more than one device at a time).
- Three-state outputs are implemented in many register, bus drivers, and flip flops.



C. 4-Bit Nibble Adder:

(4 Bit parallel Adder using full Adder).

