

By making TxRDY line high, the 8251 informs CPU that the transmitter is ready to accept data. When data are received from the CPU, TxRDY becomes low. The 8251 converts parallel data received from the CPU to serial format. Before transmitting the serial data, it makes correspondence with the modem. A modem is a device which converts the digital signal to audio frequency tones. This is needed because our telephone lines are conventional having band width only about 300 to 3000 Hz. Therefore, digital signals cannot be transmitted over these lines directly. To overcome this difficulty, digital signals are converted to audio frequency tones. Telephone lines being less costly may be used for serial data transmission. Modem and other equipment used to send data over long distances are known as data communication equipment (DCE). The terminals and computers which are used to send or receive serial data are called data terminal equipment (DTE).

The 8251 makes DTR low to inform modem that it is ready to send data. By making DSR low, the modem responds to 8251 indicating that it is also ready for onward data transmission. When modem and 8251 both are ready for data transmission, the 8251 makes RTS low to request modem for initiation of data transmission. The modem acknowledges this request by making CTS low. When CTS goes low, it enables transmission logic of 8251 to send serial data on TxD line. If data transmission has to be stopped due to any reason, CTS signal is made high.

8.9 PROGRAMMABLE COUNTER/INTERVAL TIMER

The important functions of a programmable timer/counter are generation of accurate time delay, event counting, rate generation, complex wave form generation, complex motor control, etc. under software control. Intel has developed 8254 and 8253 programmable counter/interval timer for such purposes.

8.9.1 Intel 8254

Intel 8254 is a programmable counter/interval timer. It is designed to generate accurate time delay, to generate square waves to control motor etc. It is a 24 pin IC and operates at 5 volt DC. Its operating frequency is in the range DC to 10 MHz, uses HMOS technology, contains 3 independent 16-bit counters and operates in the following six modes:

- Mode 0 : Interrupt on terminal count
- Mode 1 : Hardware retriggerable one-shot
- Mode 2 : Rate generator
- Mode 3 : Square wave generator
- Mode 4 : Software triggered strobe
- Mode 5 : Hardware triggered strobe.

Figure 8.31 shows the schematic diagram of Intel 8254. Its important signals are:

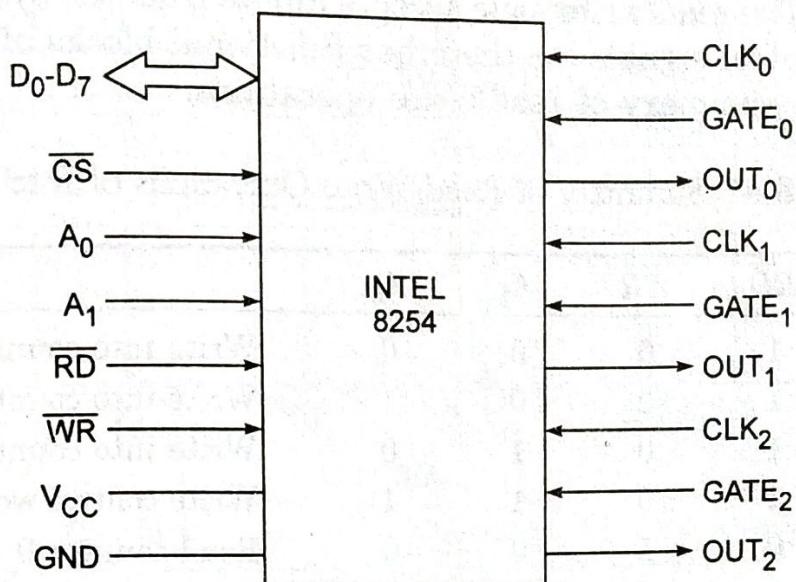


Fig. 8.31 Schematic Diagram of Intel 8254

RD (Read) When this signal goes low the CPU reads information from 8254.

WR (Write) When it goes low CPU writes into 8254.

CS (Chip select) When it is made low the 8254 is enabled.

D₀ - D₇ Bidirectional 3-state Data Bus lines connected to system data bus.

A₀ - A₁ (Address pins) These are used to select one of the 3 counters or the control word register for read or write operation. Counters or control word register are selected as shown in Table 8.3.

Table 8.3 Addressing of Counters of 8254

		Selects
A ₁	A ₀	
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word register

✓ CLK₀, CLK₁ and CLK₂ are clock terminals for counter 0, counter 1 and counter 2 respectively.

✓ GATE₀, GATE₁ and GATE₂ are gate terminals of counter 0, counter 1 and counter 2 respectively.

✓ OUT₀, OUT₁ and OUT₂ are output terminals of counter 0, counter 1 and counter 2 respectively.

Figure 8.32 shows the functional block diagram of Intel 8254. The 8254 contains data bus buffer, read/write logic, a control word register and three 16-bit counters. The data bus buffer is a 3-state, bidirectional, 8-bit buffer. The read/write logic accepts inputs from the system bus and generates control signals for the other functional blocks of 8254. Table 8.4 gives the summary of read/write operations.

Table 8.4 Summary of Read/Write Operations of Intel 8254

\overline{CS}	\overline{RD}	\overline{WR}	A_1	A_0	
0	1	0	0	0	Write into counter 0
0	1	0	0	1	Write into counter 1
0	1	0	1	0	Write into counter 2
0	1	0	1	1	Write control word
0	0	1	0	0	Read counter 0
0	0	1	0	1	Read counter 1
0	0	1	1	0	Read counter 2
0	0	1	1	1	No operation (3-state)
1	X	X	X	X	No operation (3-state)
0	1	1	X	X	No operation (3-state)

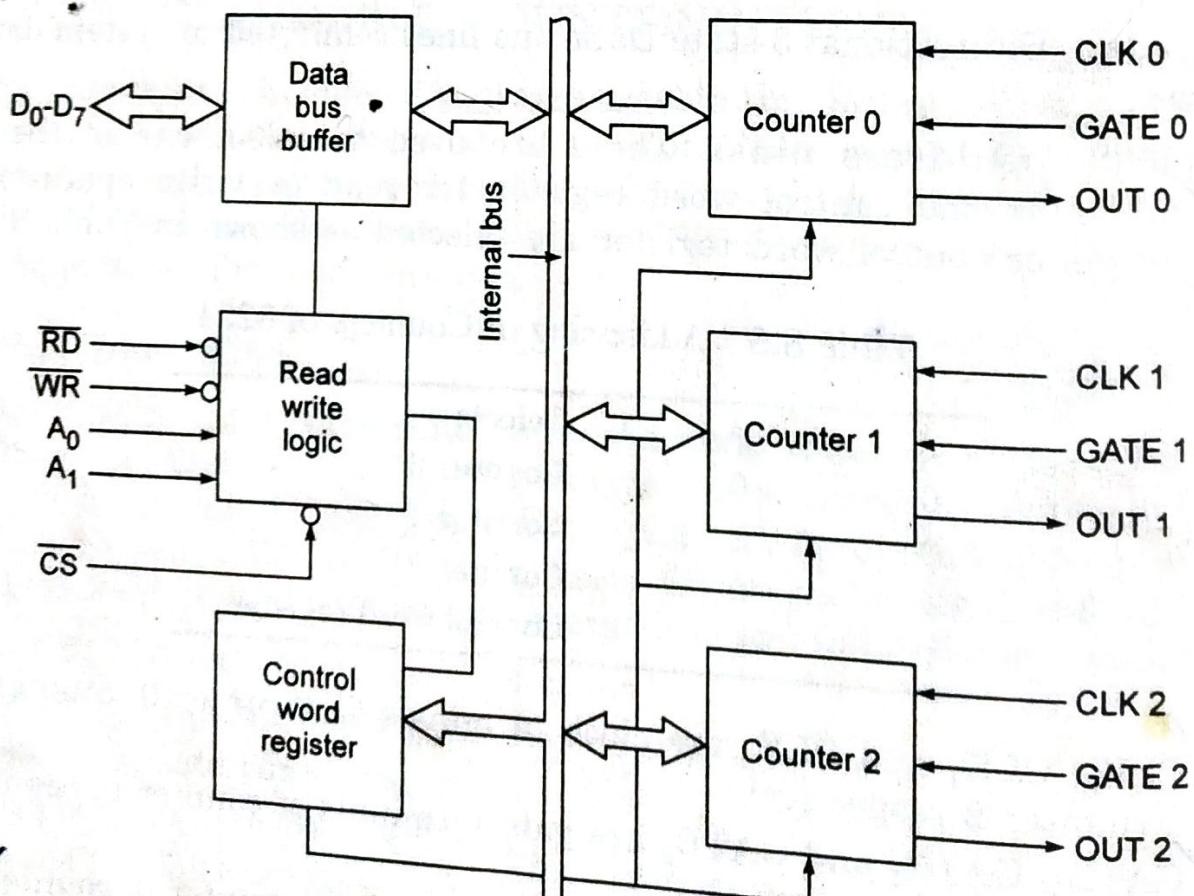


Fig. 8.32 Functional Block Diagram of Intel 8254

Control Word Register A control word is determined to select and program a counter of 8254. The control word is written into the control word register of 8254. The control word register is selected when $A_1, A_0 = 11$. The control word also specifies which counter is being programmed. The initial count is written into the counter register, not the control register. A_1, A_0 select the counter to be written into.

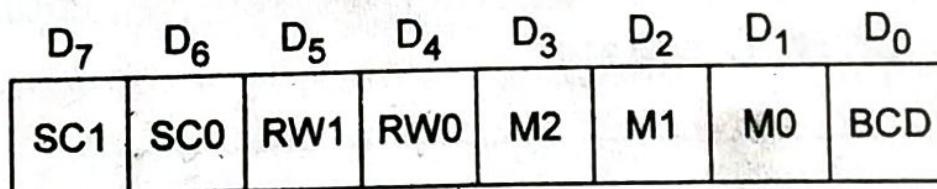


Fig. 8.34 Control Word Format for Intel 8254

The Fig. 8.34 shows the control word format for Intel 8254. The bits D₆ and D₇ of the control word select one of the three counters as shown in Table 8.5.

Table 8.5 Selection of Counters

SC ₁	SC ₀	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Read back command

D_4 and D_5 are used for loading/reading the count into/from the counter register as shown in Table 8.6.

Table 8.6 Read/Write Operation

RW_1	RW_0	
0	0	Counter latch command
0	1	Read/write least significant byte only
1	0	Read/write most significant byte only
1	1	Read/write least significant byte first then most significant byte.

The bits D_1 , D_2 and D_3 are used to select one of the six operating modes of 8254 as shown in Table 8.7.

Table 8.7 Mode Selection

M_2	M_1	M_0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

Bit No. D_0 is used to specify whether the selected counter will act as a binary counter or BCD counter.

D_0
0 Binary counter, 16-bit
1 BCD counter, 4 decades

Counter Latch Command Like a control word, this command is also written to the control word register. Its format is shown in Fig. 8.35. The bit No. 7 and 6 specifies counter to be latched. The bit No. 4 and 5 are 00. They designate counter latch command. These bits distinguish the counter latch command from the control word. Bit No. 0 to bit No. 3 are don't care bits.

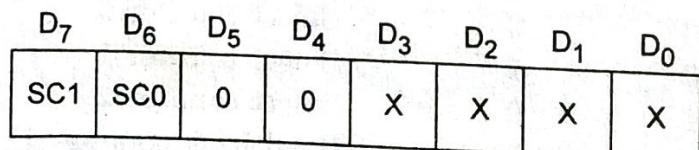


Fig. 8.35 Counter Latching Command Format

The selected counter's output latch latches the count when the counter latch command is received. This count is held in the latch until it is read by the CPU (or until the counter is reprogrammed). This permits reading the contents of a counter without affecting the counting in progress. Multiple counter latch commands can be used to latch more than one counter. Each latched counters output latch holds its count until it is read. Counter latch command's do not affect the programmed mode of operation of the counter.

Read-back Command The read-back command permits the programmer to check the count value, programmed mode and current state of output of the selected counter. This command is also written to the control word register. Figure 8.36 shows format of read-back command. Bit No. 7 and 6 are 11 to identify this command as a read-back command. Bit No. 5 is put zero to latch the count of selected counter, bit No. 4 is put zero to latch status of the selected counter, bit No. 3 is put 1 to select counter 2, bit No. 2 is put 1 to select counter No. 1, bit No. 1 is put 1, to select counter 0 and bit No. 0 is reserved for future expansion. It is put to 0. The advantage of this control word is that the programmer can latch one, two or three counters putting 1 in the appropriate bits in the read-back command format.

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	Count	Status	CNT2	CNT1	CNT0	0

Fig. 8.36 Read-Back Command Format

Mode 0: Interrupt on Terminal Count This mode of operation is used for generation of accurate time delay under software control. The control word for mode 0 operation is loaded into the control word register. The control word selects a particular counter and defines its mode of operation etc. Then the count is loaded into the register of selected counter. After the control word is written, the output of the counter goes low and remains low until counter decrements its count to 0. GATE is kept high to enable the counting. After a count is loaded into the count register, the counting will start if GATE is high. The counting starts from the following edge of next clock cycle as shown in Fig. 8.37. The output of the counter is initially low and remains low while counting is going on. When counter decrements its count to 0, the output will go high and will remain high until a new count or a new Mode 0 control word is written into the counter. When a new count is loaded or the counter is reloaded, the output becomes low and counter starts counting again.

If GATE goes low while counting is going on, counting stops. When GATE returns to high, counting is resumed from the count value at which counting had discontinued. The count value can also be changed

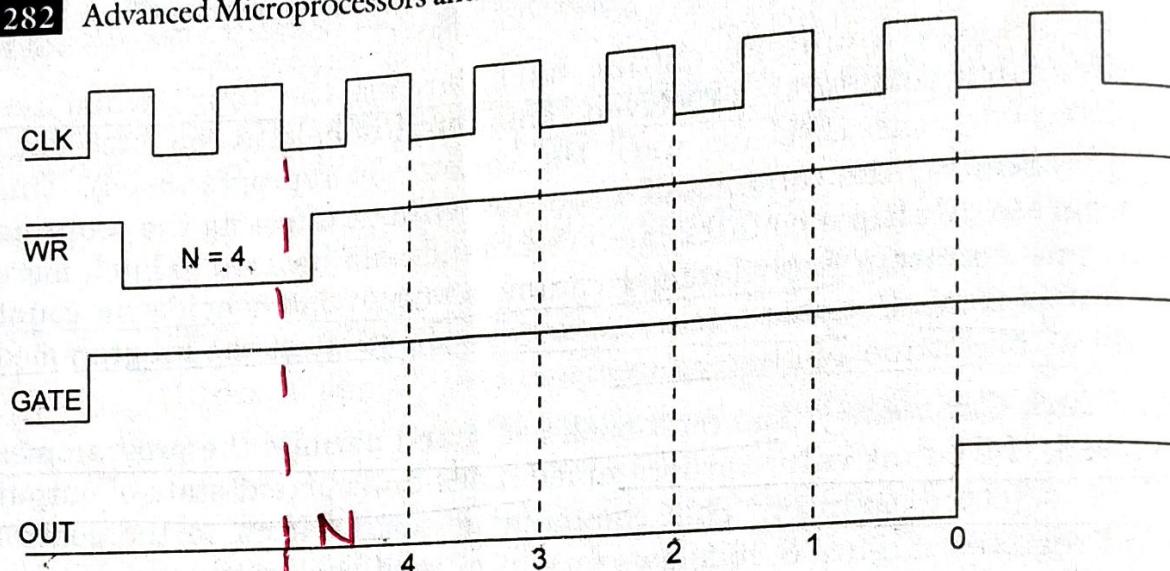


Fig. 8.37 MODE 0, Interrupt on Terminal Count

while count is going. After the loading of new count, counting restarts from the new value of the count. The counting starts after the loading of new value of count if the count is of only one byte. If the new count is of two bytes, the counter stops after loading of the first byte of the new count. The counter starts its counting operation after the 2nd byte of the new count is loaded.

The output of the counter can be used to strobe a device which has to start its operation after certain accurate time delay. The output can also be used to interrupt the microprocessor. The delay time can be calculated from the number of counts and the time for one clock cycle of the clock applied to the counter. If the count is N and time for one clock cycle is t , the delay is equal to $(N + 1)t$. One extra clock cycle is required because the counting starts from the next falling edge of the clock after loading the counter.

Mode I: Hardware Retriggerable One-shot or Programmable One-shot In this mode of operation, a low to high pulse signal is applied to the GATE. This signal acts as a trigger. After mode set operation the counter is loaded with the count value of N . Initially, the output remains high. It goes low on the clock pulse following a trigger. Counting starts as shown in the Fig. 8.38. The output remains low until the counter reaches 0. The width of the output pulse is equal to N clock cycles. This width is programmable, and hence this mode of operation is called programmable one-shot.

If the trigger pulse is applied to the GATE again, the counter is reloaded by the count N . The counter decrements count once again and the output goes low for N clock cycles once again. Thus one-shot mode is retriggerable. If a new count is written to the counter while output is still low (i.e. during a one-shot pulse), the current one-shot is not affected unless the counter is retriggered. After retrigerring, the one-shot is again generated with new count value.

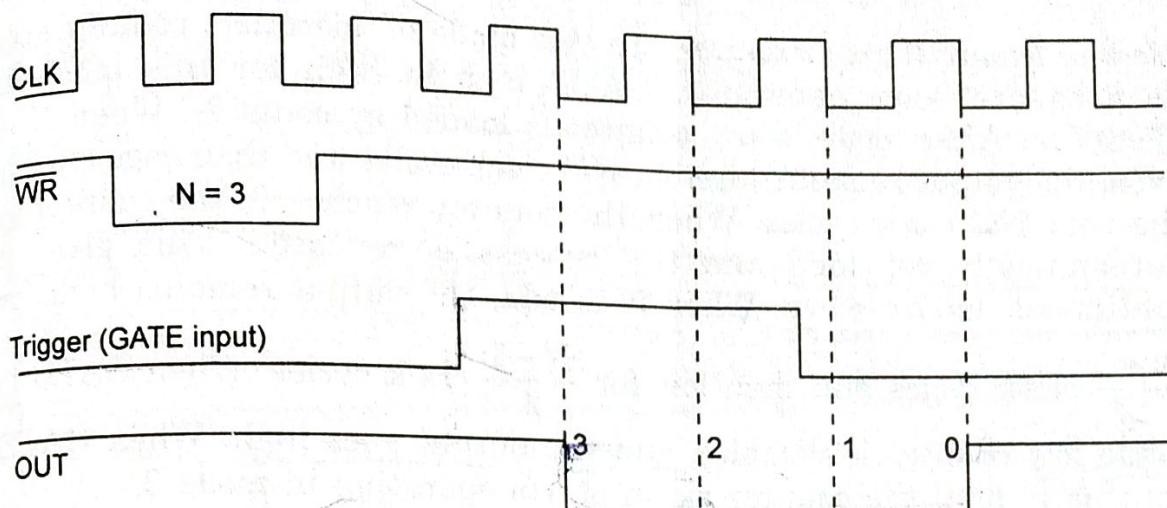


Fig. 8.38 MODE 1, Programmable One-Shot

If the GATE is retriggered while counting is still going on (i.e. during a one-shot pulse), the counter is reloaded again and it decrements count again. The output will continue to remain low for N clock cycles after the occurrence of the second low to high transition signal applied to the GATE.

Mode 2: Rate Generator In this mode of operation counter acts as a divide by N counter. After mode is set, the counter is loaded with the count N . For mode 2 operation, GATE is to be kept high. After the counter is loaded the counting starts at the negative edge of the next clock cycle as shown in Fig. 8.39. The output remains high for $(N-1)$ clock cycles and then goes low for one clock-cycle. This process is repeated till the GATE is high. If GATE is made low, the counter is disabled and the output becomes high. When GATE returns to high the counter resumes its operation and starts counting from initial count.

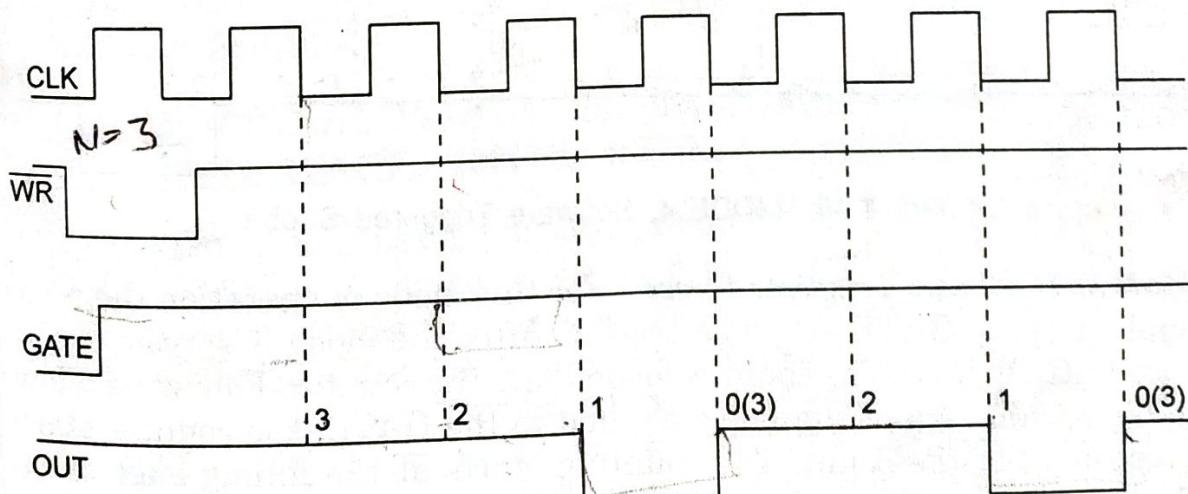


Fig. 8.39 MODE 2, Rate Generator

If a new count is written between the output pulses, the current sequence of counting is not affected. But subsequent sequence of counting uses new value of the count.

Mode 3: Square Wave Generator In this mode of operation, counter acts as a square wave generator. GATE is held high for this mode of operation. After mode is set, counter is loaded by count N. When N is even, the output remains high for $N/2$ clock cycles and then goes low for the next $N/2$ clock cycles. When the counter reaches 0, the counter is automatically reloaded and the process is repeated. This gives a continuous square wave. When N is odd, the output remains high for $\frac{N+1}{2}$ clock cycles and then low for $\frac{N-1}{2}$ clock cycles. When GATE is made low counter is disabled and the output goes high. When GATE returns to high the counter again starts operating in mode 3.

✓ **Mode 4: Software Triggered Strobe** For this mode of operation GATE is held high. After mode is set the output becomes initially high. Counter starts counting at the falling edge of the next clock pulse. When counter reaches zero the output goes low for one clock period and then goes high again as shown in Fig. 8.40. The output may be used as a strobe. As the generation of the strobe signal is triggered by writing a count into the counter, this mode of operation is called software triggered strobe. If a new count is written during counting, it will be loaded on the next clock pulse and the counting will continue from the new count again.

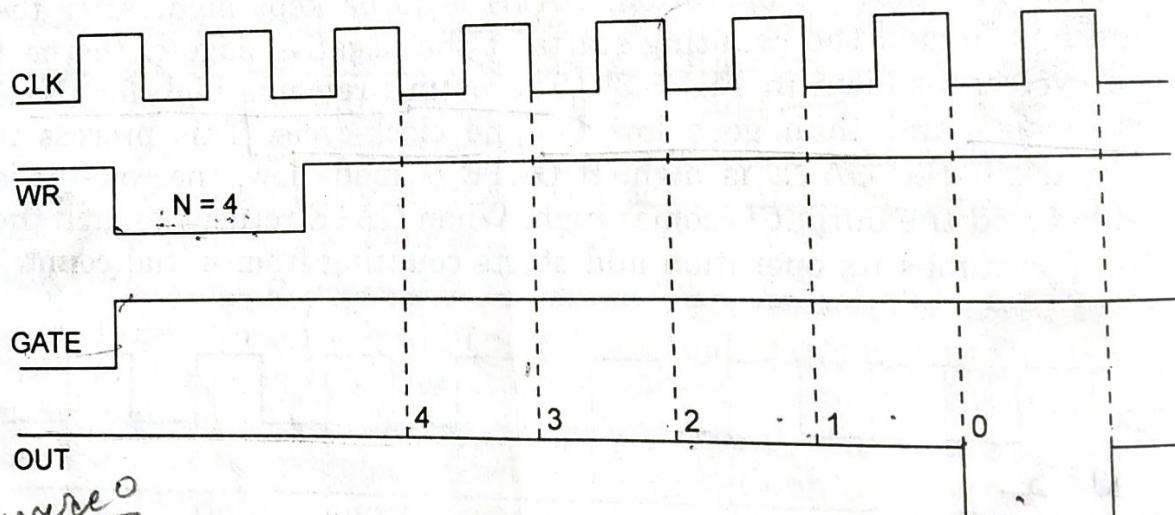


Fig. 8.40 MODE 4, Software Triggered Strobe

Mode 5: Hardware Triggered Strobe For this mode of operation the pulse applied to the GATE acts as a trigger. After the mode is set the output goes initially high. The count is loaded into the counter. Following a low-to-high transition of the pulse applied to the GATE, the counter starts decrementing the count. The counting starts at the falling edge of the clock pulse after the application of a trigger pulse to the GATE, as shown in Fig. 8.41. When counter reaches zero the output goes low for one clock period and then becomes high again. As the triggering pulse comes from the hardware circuitry this mode of operation is called hardware triggered strobe.

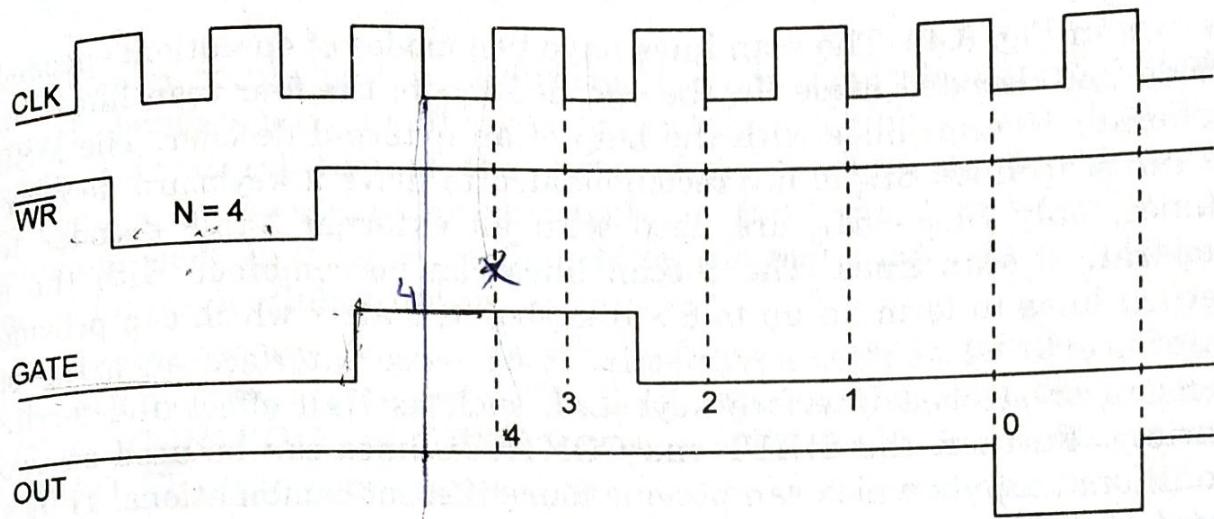


Fig. 8.41 MODE 5, Hardware Triggered Strobe

This mode of operation is retriggerable. If the trigger pulse is applied to the GATE again, the counter is reloaded by the count N and the counter starts decrementing the count again. When the counter reaches zero, the output goes low for one clock period and becomes high again.

If a new count is loaded during counting, the current counting sequence is not affected. If a trigger occurs after a new count is loaded but before the current count reaches zero, the counter will be loaded with the new count and counting will continue from there.

8.9.2 Intel 8253

$8254 \rightarrow 8MHz$

Intel 8253 is a programmable counter/interval timer. It is pin to pin compatible with Intel 8254. Its input clock frequency is comparatively less than that of Intel 8254. The range of its clock frequency is DC to 2.6 MHz. It also operates in six modes as explained in case of Intel 8254. It has three 16-bit programmable counters.

Intel 8254 has a read-back feature whereas Intel 8253 does not have read-back feature.