

Chapter 4: Bus Structure & Memory Device

Bus configuration of a microprocessor (Refer to chs)

- ↳ Address bus
- ↳ Data bus
- ↳ Control bus

Synchronous bus Vs Asynchronous bus

Memory Classification

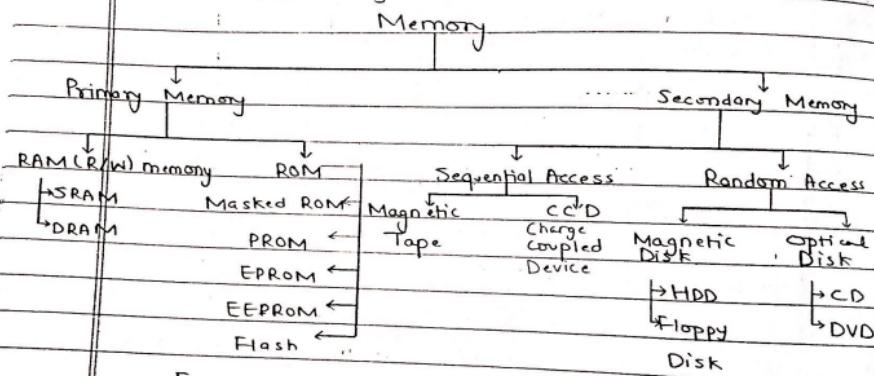


Fig: classification of memory.

Synchronous

- A memory is a collection of storage cells that is used to store data and information.
- A memory is a storage device.
- Flipflop is the memory unit that stores 1 bit of information.

1. Structure of a memory

- The internal structure of a 8x8 memory is shown.
- Every memory unit has similar type of structure.

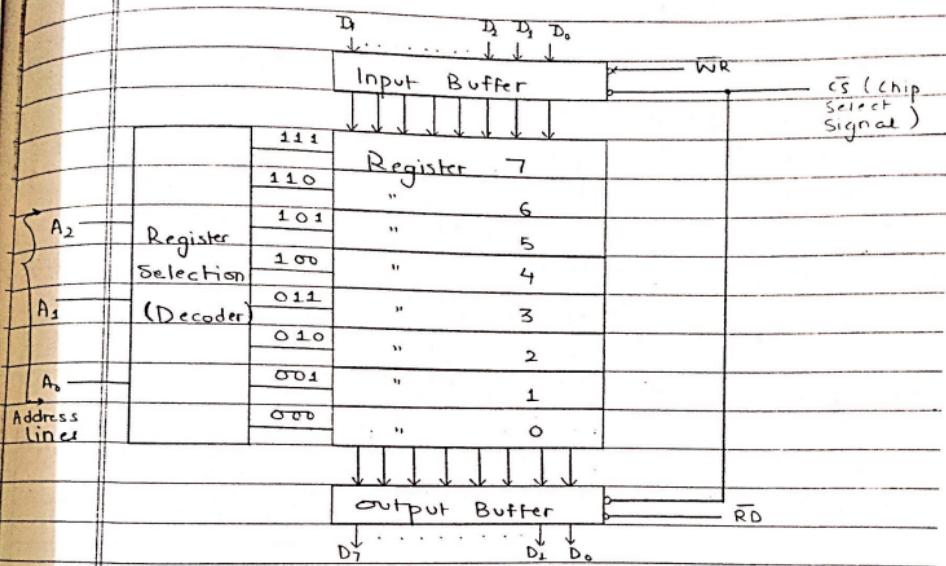


Fig: Internal structure of a 8x8 memory.

Internally, a memory consists of :

↳ address decoder

↳ Input buffer

↳ output buffer

↳ registers

along with data lines, address lines & control signals.

→ The memory capacity of any memory can be written as : $C = M \times N$

$$= 2^k \times N$$

Where, M → no. of memory locations

K → address bus width

N → Data bus width

For eg: 8x8 memory consists of
address bits = 3
Data bits = 8

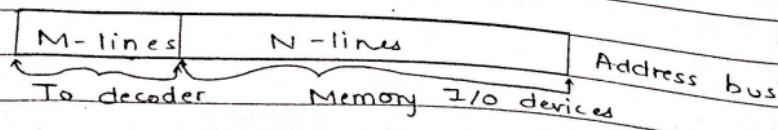
Basic Concept of Memory Interfacing:

- The primary function of memory interfacing is that the microprocessor should be able to read from and write into a given register of a memory chip. To perform the operation, the MP should
 - ① be able to select the chip.
 - ② Identify the register
 - ③ Enable the appropriate buffer.

- Memory Interfacing is the process of communication between microprocessor and memory.

Address Decoding

- The process of generating chip select (\bar{CS}) signal using the address lines of a MP and a decoder or logic to interface memory or I/O devices with microprocessor is called address decoding.
- The process of determining the range of address allocated by the MP during memory interfacing is called address decoding.



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Q1. Address decoding is of two types:

1. Full address decoding:

If all the address lines of a MP system is used to process a memory or I/O devices, it is a full address decoding. Also known as unique or absolute address decoding since the address is unique.

2. Partial address decoding:

If all the address lines of the MP system is not used to address a memory or I/O, it is called partial address decoding. The address of the memory or I/O is not unique so it is called non-unique address decoding.

Q2. Interface a (2048x8) RAM with 8085 MP. Also determine the range of address.

→ Here,

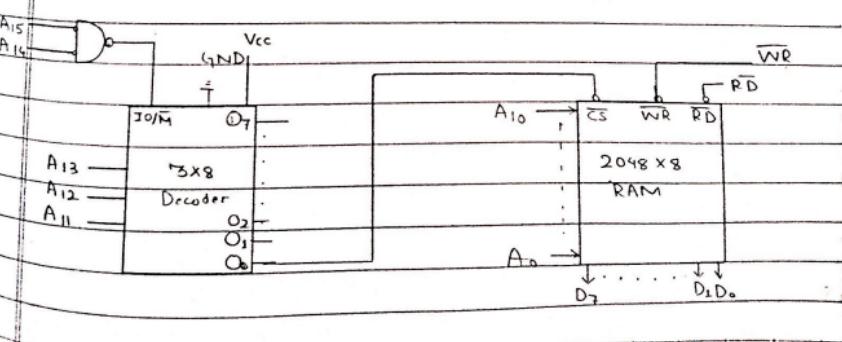
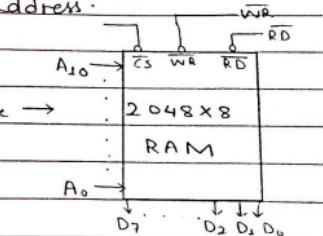
Memory capacity of RAM is :

$$C = 2048 \times 8 \quad \text{Incomplete} \rightarrow 2048 \times 8$$

$$= 2^{11} \times 8$$

∴ No. of address lines = 11

No. of data lines = 8



Address Decoding																
	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
Initial Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Final Address	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

The range of address is 0000H to 07FFH.

Interface 2KB RAM, 4KB EEPROM and 8KB EPROM with 8085 MP. Also determine the range of address. (with starting address PU26 (4000H))

Here, Memory capacity of RAM is,

$$= 2^1 \times 8$$

$$= 2^1 \cdot 2^{10} \times 8$$

$$= 2^{11} \times 8$$

∴ Address bits = 11

Data bits = 8

Memory capacity of EEPROM is,

$$= 48 \text{ k} \times 8$$

$$= 2^{18} \times 8 \quad 2^2 \cdot 2^{10} \times 8$$

$$= 2^{12} \times 8$$

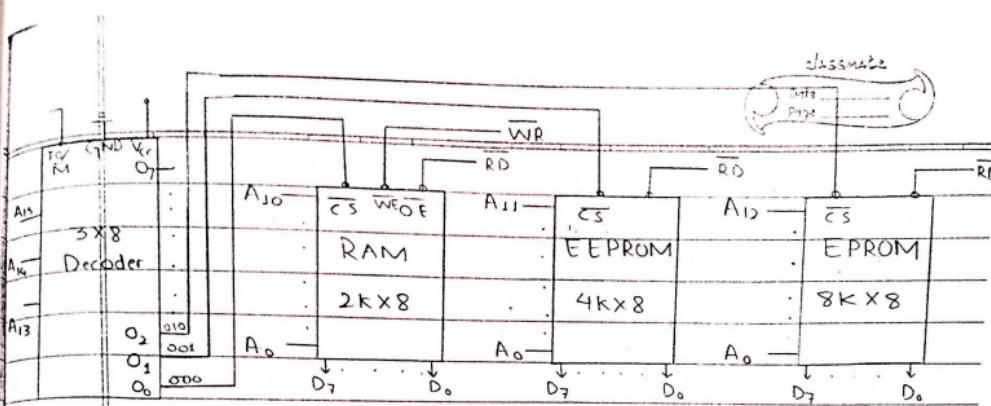
∴ Address bits = 12

Data bits = 8

EPROM : Capacity = 8k × 8 = 2¹³ × 8

∴ Address bits = 13

Data bits = 8



Address Decoding

	Address	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Range	
R	Initial	0	0	0	X	X	0	0	0	0	0	0	0	0	0	0	0	xx=00 0000H 07FFH	xx=01 0800H OFFFH
A	Final	0	0	0	X	X	1	1	1	1	1	1	1	1	1	1	1	xx=10 1000H 17FFFH	xx=11 1800H 1FFFH
M	Initial	0	0	1	X	0	0	0	0	0	0	0	0	0	0	0	0	For x=0 2000H 3000H	For x=1
E	Final	0	0	1	X	1	1	1	1	1	1	1	1	1	2	1	1	2FFFH 3FFFFH	
P	Initial	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000H to	
R	Final	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	5FFFH	
O																			
M																			

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- #1 Design an address decoding circuit to interface 4Kx8 RAM with starting address 8000H.

Memory capacity of RAM is,

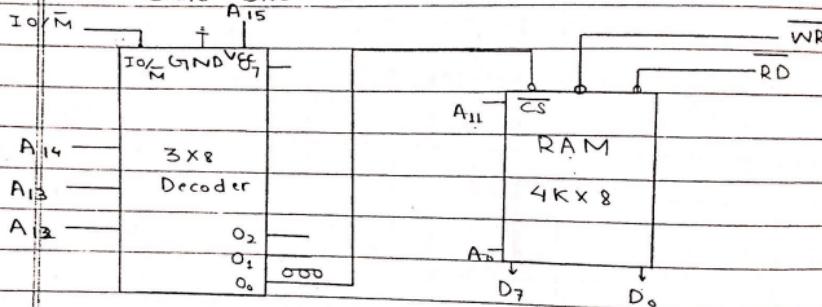
$$= 4K \times 8$$

$$= 2^2 \times 2^{10} \times 8$$

$$= 2^{12} \times 8$$

∴ Address bits = 12

Data bits = 8



	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Range
Initial	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000H
Final	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	4FFFH