

(HMOS). It is available in 3 versions: the 8086, 8086-2 and 8086-1. The clock rates are: 5 MHz for 8086, 8MHz for 8086-2 and 10MHz for 8086. 1. The 8086 microprocessor is no longer used. But the concept of its principles and structure is very useful for the understanding of other advanced Intel microprocessors.

The 8086 has 20 address lines. Using 20 address lines it can directly address up to  $2^{20}=1$  megabytes (1MB) of memory. The address lines operate in time-multiplexed mode. The 16 low-order address lines carry 16 low-order address bits at certain times, and thereafter they carry 16-bit data at other times. The 4 high-order address lines are also time-multiplexed lines. They carry 4 high-order address bits and thereafter certain status signals.

## 2.2 PIN DESCRIPTION OF INTEL 8086

Figure 2.1 (a) and (b) show the pin diagrams of Intel 8086. Figure 2.1(a) shows the signals of 8086 for minimum mode of operation. Figure 2.1(b) shows the signals for maximum mode of operation. These modes have been discussed in the subsequent sections. Its pins and signals are:

**AD<sub>0</sub>-AD<sub>15</sub> (Bidirectional)** These lines constitute time-multiplexed address/data bus. During T<sub>1</sub> clock cycle of the bus cycle they carry low-order 16-bits of address. During T<sub>2</sub>, T<sub>3</sub> and T<sub>4</sub>, they carry 16-bit data. The Intel 8284 clock generator/driver is employed to generate clock signals required for 8086. AD<sub>0</sub>-AD<sub>7</sub> carry low-order byte of data and AD<sub>8</sub>-AD<sub>15</sub> carry high-order byte of data. When AD lines carry address they are

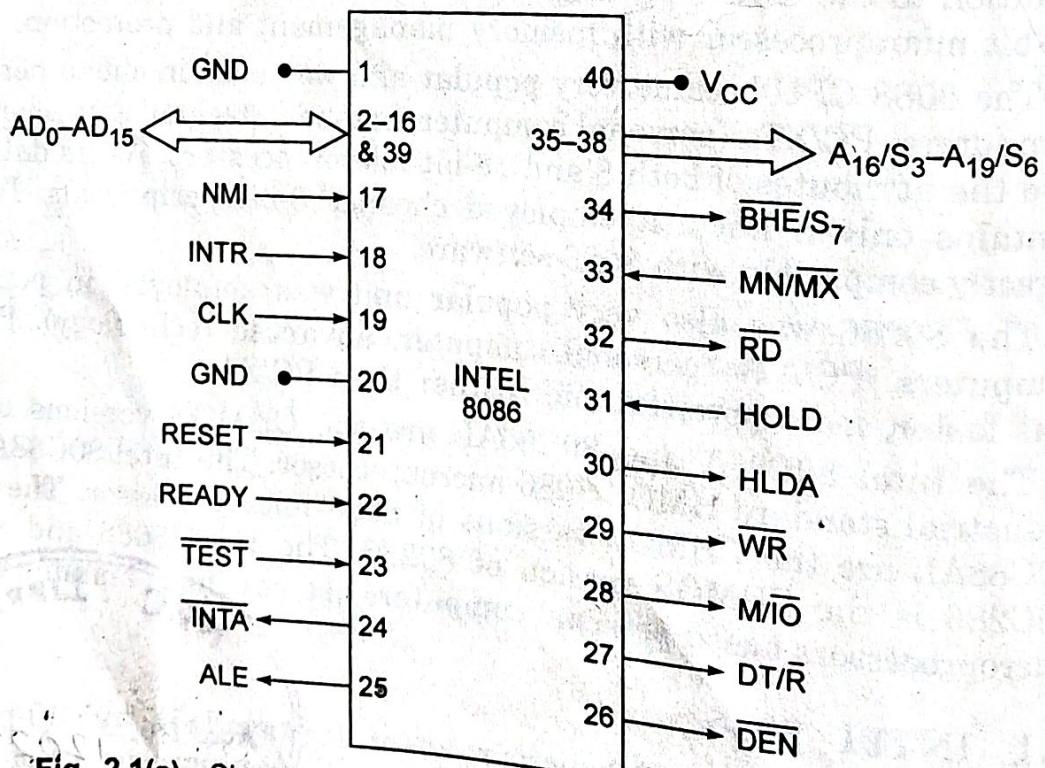
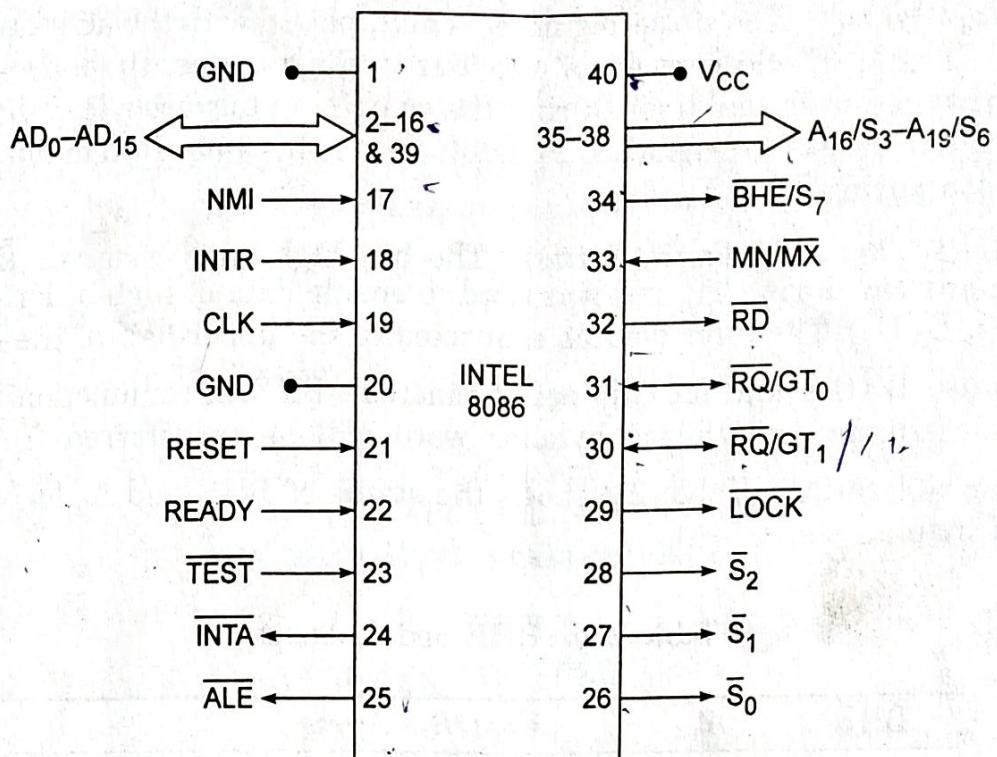


Fig. 2.1(a) Signals of Intel 8086 for Minimum Mode of Operation



**Fig. 2.1(b)** Signals of Intel 8086 for Maximum Mode of Operation

called A lines instead of AD lines, for example  $A_0-A_{15}$ . When AD lines carry data they are called D lines, for example  $D_0-D_7$ ,  $D_8-D_{15}$  or  $D_0-D_{15}$ .

**$A_{16}-A_{19}$  (Output)** These are time-multiplexed lines. During  $T_1$  they carry high-order 4 bits of memory address. During I/O operation, these lines remain low. During  $T_2$ ,  $T_3$  and  $T_4$  these lines carry status signal.

**$A_{16}/S_3$ ,  $A_{17}/S_4$  (Output)** These lines carry the address bits  $A_{16}$  and  $A_{17}$  during  $T_1$  clock cycle of the bus cycle. During remaining bus cycle (i.e. during  $T_2$  to  $T_4$ ), these lines carry the status signals  $S_3$  and  $S_4$ . These status signals are used to identify memory segments as shown in Table 2.1.

**Table 2.1** Encoding of  $S_3$  and  $S_4$

$S_4$	$S_3$	Segment Register Employed
0	0	ES
0	1	SS
1	0	CS or none
1	1	DS

**$A_{18}/S_5$  (Output)** The status signal  $S_5$  is multiplexed with the address line  $A_{18}$ . During  $T_1$  clock cycle of the bus cycle, eighteenth bit of the address is transmitted over this line. During the remaining bus cycle (i.e. during  $T_2$  to  $T_4$ ) the status signal  $S_5$  is transmitted over this line.  $S_5$  is an interrupt enable status. The status of the interrupt enable flag bit,  $S_5$ , is updated at the beginning of each clock cycle.

**$A_{19}/S_6$  (Output)** The status signal  $S_6$  is multiplexed with the address line  $A_{19}$ . During  $T_1$  clock cycle of the bus cycle, nineteenth address is transmitted over this line. During the remaining bus cycle (i.e. during  $T_2$  to  $T_4$ ) the status signal  $S_6$  is available on this line. It remains low always during  $T_2$  to  $T_4$ .

**$\overline{BHE}/S_7$  (Bus High Enable/Status)** The bus high enable signal,  $\overline{BHE}$ , remains low during  $T_1$ , and it is used to enable data of high-order data lines,  $D_8-D_{15}$ . The 8-bit devices connected to the upper-half of the data bus use  $\overline{BHE}$  signal for chip select function.  $\overline{BHE}$  in conjunction with  $A_0$  determines whether a byte or word will be transferred from/to memory locations. Table 2.2 shows the status of  $\overline{BHE}$  and  $A_0$  for word and byte access.

Table 2.2  $\overline{BHE}$  and  $A_0$  Status

$\overline{BHE}$	$A_0$	Word/Byte Access
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

The  $\overline{BHE}/S_7$  is a time-multiplexed line. During  $T_2$  to  $T_4$  the status signal  $S_7$  is transmitted on this line. It remains always high.

**$\overline{RD}$  (Output)** It is a read signal issued by the processor. It is an active low signal. It indicates that the processor is performing read operation with memory or I/O depending on the state for the  $M/\overline{IO}$  signal. This signal is used to read devices which are connected to the 8086 local bus.

**$READY$  (Input)** It is an acknowledgment received from the addressed memory or I/O device. It is an active high signal. When high, it indicates that the peripheral device is ready to transfer data.

**$RESET$  (Input)** It is a system reset and an active high signal. When it goes high the processor goes into reset state. To be effective, this signal must remain high for at least four clock cycles.

**$INTR$  (Input)** Interrupt request.

**$NMI$  (Input)** Non-maskable interrupt request.

**$\overline{TEST}$  (Input)** This signal is used to test the status of math coprocessor 8087. The BUSY pin of 8087 is connected to the  $\overline{TEST}$  pin of 8086. Sometimes the 8086 needs the result of some computation that 8087 is doing, before it can go to the next instruction of the program. In such a situation WAIT instruction is used in the program. If  $\overline{TEST}$  is high, 'WAIT' instruction causes 8086 to wait in an idle state. When 8087

completes computation, it makes BUSY signal low, thereby making TEST low. When TEST becomes low, the 8086 goes to the next instruction and continues execution of the program.

**MN/MX (Input)** Indicates operating mode of 8086. When high, the processor operates in the minimum mode. When low, it operates in the maximum mode.

**CLK (Input)** Clock Input.

**V<sub>CC</sub>** +5V power supply pin.

**GND** Ground.

The above pin description holds good for both the minimum and maximum mode of operation. The pin functions which are unique for the minimum and maximum mode of operation will be discussed in subsequent sections.

### 2.3 OPERATING MODES OF 8086

The 8086 has two modes of operation: the minimum mode and maximum mode. In a microcomputer system where only one 8086 microprocessor works as a CPU, it operates in the minimum mode of operation. In a multiprocessor and coprocessor configuration, the 8086 operates in the maximum mode of operation. The minimum mode is used in a few 8086 (or 8088) based systems with a few peripheral devices. Personal computers employing coprocessor configuration run in maximum mode. When there are large number of CPUs in a system, they operate in parallel. The status of the pin MN/MX decides the operating mode of 8086. When this pin is high, the 8086 operates in minimum mode. When it is low, the 8086 operates in maximum mode. The 24 to 31 pins of 8086 have alternate function. They issue two sets of signals, one when the 8086 operates in the minimum mode of operation and the other in the maximum mode of operation.

### 2.4 PIN DESCRIPTION FOR MINIMUM MODE

The pin functions which are unique for the minimum mode of operation are discussed in this section. The other pin functions are same as already discussed in the Section 2.2. For minimum mode of operation pin MN/MX is kept high. The pins 24-31 have unique pin functions for the minimum mode of operation as shown in Fig. 2.1. (a) which are as follows:

**INTA (Output). Pin 24 Interrupt Acknowledge.** It is active low. On receiving interrupt signal the processor issues an interrupt acknowledge signal through this line.

**ALE (Output). Pin 25 Address Latch Enable.** It is a high pulse issued by the processor during T<sub>1</sub> state of a bus cycle. The processor sends this signal to latch the address into the 8282/8283 address latch. The signal on this pin can be used to demultiplex the address, data & status lines on A<sub>00</sub>-A<sub>15</sub>, A<sub>16/S<sub>3</sub></sub>-A<sub>19/S<sub>6</sub></sub> and S<sub>4/E/S<sub>7</sub></sub>.

**DEN (Output). Pin 26 Data Enable.** In the minimum mode of operation this signal is issued by the processor to enable Intel 8286/8287 bus transceiver. It is an active low signal.

**DT/R (Output). Pin 27 Data Transmit/receive.** When the minimum mode system incorporates Intel 8286/8287 octal bus transceiver, this signal is required for the data flow control. When this signal is high, data are sent out and when it is low, data are received.

**M/IO (Output). Pin 28 Status Signal.** It is issued by the processor to distinguish a memory access from an I/O access. When this signal is high memory is accessed and when it is low, an I/O device is accessed.

**WR (Output). Pin 29 Write.** When this signal is low, the processor performs memory write or I/O write operation depending on the state of M/IO signal.

**HLDA (Output). Pin 30 HOLD Acknowledge.** On receiving HOLD signal, the processor issues a HOLD acknowledge signal through this pin. It is an active high signal.

**HOLD (Input). Pin 31** When another device in the system wants to use the address and data bus, it sends a HOLD request to the processor through this line. It is an active high signal.

## 2.5 PIN DESCRIPTION FOR MAXIMUM MODE

For the maximum mode of operation, the pin MN/MX is kept low and is grounded. The pins 24-31 have unique functions for the maximum mode of operation as shown in Fig.2.1(b) which are as follows:

**QS<sub>1</sub>, QS<sub>0</sub> (Output). Pin 24, 25 Queue Status.** The queue status is valid during the clock cycle after which the queue operation is performed. These signals provide status to allow external tracking of the internal 8086 instruction queue. Table 2.3 shows the status of QS<sub>0</sub> and QS<sub>1</sub>.

Table 2.3 Status of QS<sub>0</sub> and QS<sub>1</sub>

QS <sub>1</sub>	QS <sub>0</sub>	Characteristics
0	0	No Operation
0	1	1st byte of opcode from queue
1	0	Empty queue
1	1	Subsequent byte from queue

**S<sub>0</sub>, S<sub>1</sub>, S<sub>2</sub> (Output). Pin 26, 27, 28 Status Signals.** These signals are required by Intel 8288 bus controller to generate all memory and I/O access control signals. Table 2.4 shows the encoding of these signals.

**Table 2.4** Encoding of  $\bar{S}_0$ ,  $\bar{S}_1$  and  $\bar{S}_2$ 

$\bar{S}_2$	$\bar{S}_1$	$\bar{S}_0$	Characteristics
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

$\overline{\text{LOCK}}$  (Output). Pin 29 The LOCK, a prefix instruction, activates  $\overline{\text{LOCK}}$  signal. It is an active low signal. It remains active until the completion of the next instruction. When it goes low, all interrupts are masked and HOLD request is not granted. Consequently other devices do not get control over the system bus while  $\overline{\text{LOCK}}$  is low. In a multiprocessor system, the other devices are informed through this signal that they should not issue HOLD request.

$\overline{\text{RQ}}/\overline{\text{GT}}_0$ ,  $\overline{\text{RQ}}/\overline{\text{GT}}_1$  (Bidirectional). Pin 30, 31 Local Bus Priority Control. An external device sends a hold request to the CPU through these lines to release the local bus at the end of CPU's current bus cycle.

$\overline{\text{RQ}}/\overline{\text{GT}}_0$  has higher priority over  $\overline{\text{RQ}}/\overline{\text{GT}}_1$ . After receiving hold request, the CPU sends hold acknowledge signal through these lines.

In the maximum mode of operation  $\overline{\text{WR}}$ ,  $\overline{\text{ALE}}$ ,  $\overline{\text{DEN}}$ ,  $\overline{\text{DT/R}}$ , etc. are not directly available from the processor. Rather they are available from the bus controller 8288.

The other pin functions are same as already discussed in the Section 2.2.

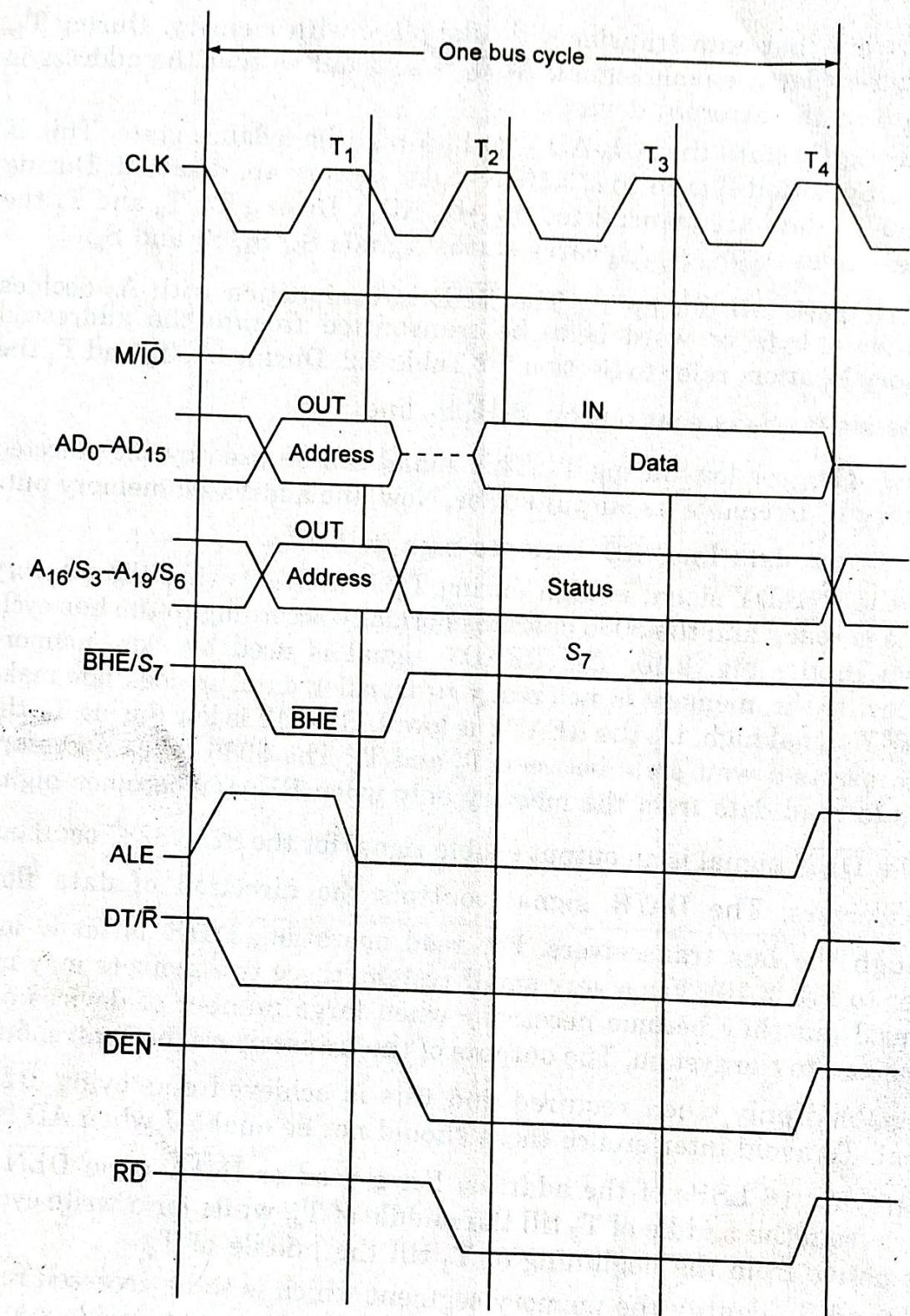
## 2.6 REGISTER ORGANIZATION OF 8086

The 8086 contains fourteen 16-bit registers. Figure 2.2 shows register organization of 8086. They are grouped into the following categories

- (i) General purpose registers
- (ii) Pointers
- (iii) Index registers
- (iv) Segment registers
- (v) Instruction pointer and status register

### 2.6.1 General Purpose Registers

There are four 16-bit general purpose registers: AX, BX, CX and DX. Each of these general purpose registers can be used either as a 16-bit register or as two 8-bit registers as shown in table 2.5. They are used



**Fig. 2.10** Timing Diagram for 8086 Memory Read Bus Cycle for Minimum Mode of Operation

8086 sends out the 20-bit memory address on the address bus. The 16 least significant bits of the address are sent out on AD<sub>0</sub>-AD<sub>15</sub> lines, and 4 most significant bits of the address on A<sub>16</sub>-A<sub>19</sub> lines. As the address lines operate in time multiplexed mode, the address remains on these lines only for the clock period T<sub>1</sub>. For the minimum mode of operation, MN/MX is kept high. The 8086 sends out a high signal on M/IO line

to indicate that data transfer will take place with memory. During  $T_1$ , an address latch enable signal, ALE, is sent out so that the address is latched in the external devices.

During  $T_2$  state the  $AD_0$ - $AD_{15}$  go into high impedance state. This is shown by dotted line in Fig. 2.10, as their drivers are disabled. During  $T_3$  and  $T_4$ , data are transmitted on  $AD_0$ - $AD_{15}$ . During  $T_2$ ,  $T_3$  and  $T_4$  the address lines  $A_{16}/S_3$ - $A_{19}/S_6$  carry status signals  $S_3$ ,  $S_4$ ,  $S_5$  and  $S_6$ .

$\overline{BHE}$  goes low during  $T_1$ . The  $\overline{BHE}$  in conjunction with  $A_0$  decides whether a byte or word is to be transmitted from/to the addressed memory location, refer to Section 2.2 Table 2.2. During  $T_2$ ,  $T_3$  and  $T_4$  the status signal  $S_7$  is sent out on  $\overline{BHE}/S_7$  line.

The  $\overline{RD}$  goes low during  $T_2$ . This signal can be used by the selected memory IC to enable its output buffer. Now, the addressed memory puts data on the data line.  $\overline{RD}$  becomes high in  $T_4$ .

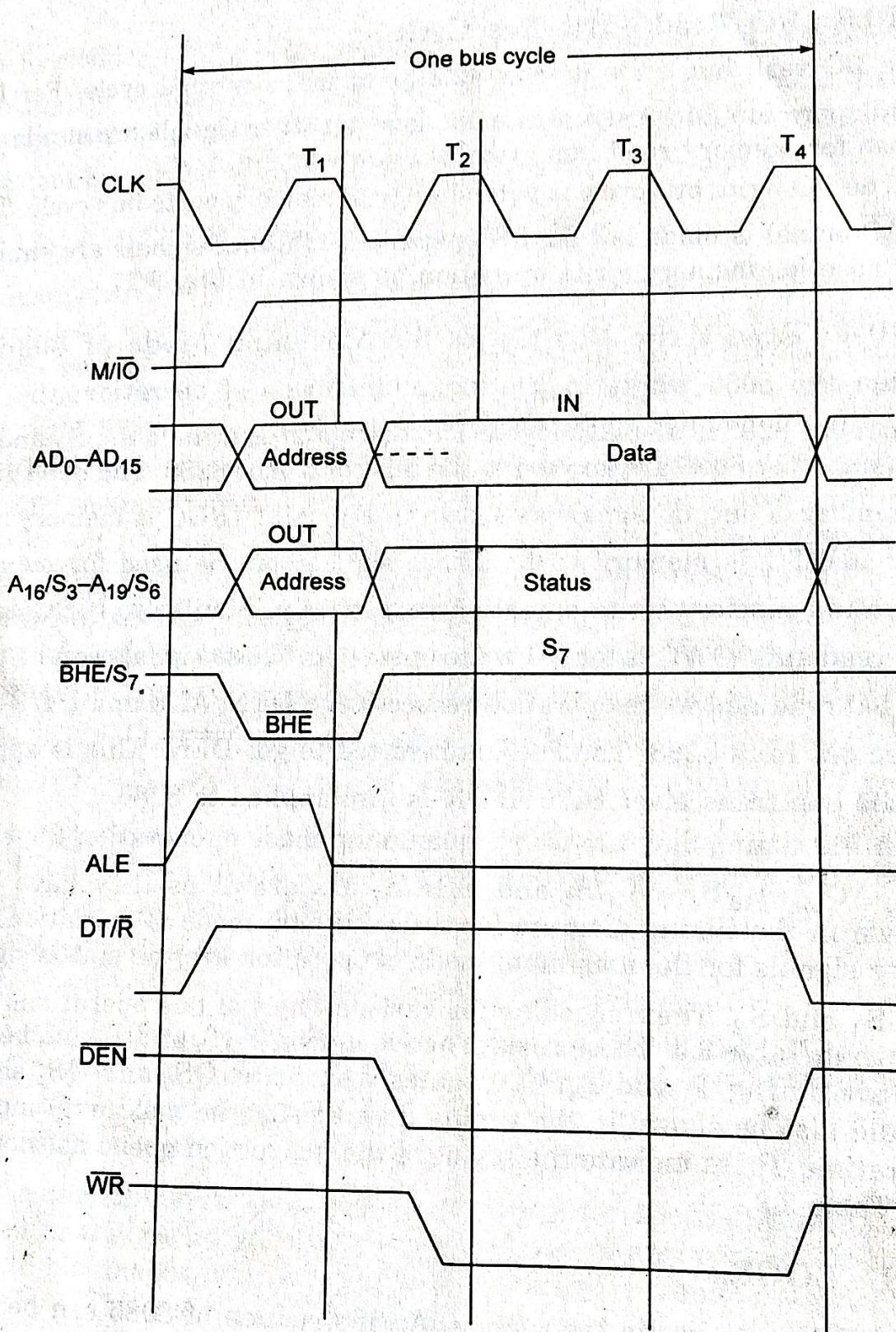
If the READY signal is high during  $T_2$ , it indicates that the memory device is ready and the 8086 operates normally according to the bus cycle shown in the Fig. 2.10. The READY signal is used by slow memory devices. If the memory is not ready to transfer data, it does not make READY signal high, i.e. the READY is low. If READY is low during  $T_2$ , the 8086 inserts a wait state between  $T_3$  and  $T_4$ . The 8086 takes necessary steps to read data from the memory only when READY becomes high.

The  $\overline{DEN}$  signal is an output enable signal for the 8286/8287 octal bus transceivers. The  $DT/\overline{R}$  signal controls the direction of data flow through the bus transceivers. For read operation,  $DT/\overline{R}$  is made low (refer to Fig. 2.10). For a very small system, these transceivers may not be used but they become necessary when large number of devices are connected to the system. The outputs of the transceivers (buffers) should be enabled only when required and this is achieved employing  $\overline{DEN}$  signal. To avoid interference these should not be enabled when AD bus is carrying 16 LSBs of the address. For a read or  $\overline{INTA}$  cycle  $\overline{DEN}$  is active from the middle of  $T_2$  till the middle of  $T_4$ , while for a write cycle, it is active from the beginning of  $T_2$  till the middle of  $T_4$ .

$S_3$  and  $S_4$  identify the memory segment which is to be accessed refer to Table 2.1., Section 2.2 for more details.  $S_5$  is interrupt enable status. The status of the interrupt enable flag bit,  $S_5$  is updated at the beginning of each clock cycle.

### 2.10.2 8086 Bus Cycle for Memory Write for the Minimum Mode

The memory write bus cycle as shown in Fig. 2.11 is similar to the read bus cycle. In case of write bus cycle,  $\overline{WR}$  goes low in  $T_2$  to enable write



**Fig. 2.11** Timing Diagram for 8086 Memory Write Bus Cycle for Minimum Mode of Operation

operation and again becomes high in T<sub>4</sub>. The signal DT/R is made high for transmitting data to the memory through transceivers. All other signals remain similar to those for read cycle. AD<sub>0</sub>-AD<sub>15</sub> is not disabled in T<sub>2</sub> and the data to be sent out are put on these lines.

### 2.10.3 I/O Read/Write Bus Cycle

The I/O read bus cycle is very similar to memory read cycle. For I/O read operation,  $M/\overline{IO}$  signal is made low. All other signals are similar to those for memory read bus cycle as shown in Fig. 2.10.

The I/O write bus cycle is very similar to memory write bus cycle. The  $M/\overline{IO}$  signal is made low for I/O operation. All other signals are similar to those for memory write operation as shown in Fig. 2.11.

### 2.10.4 Read/Write Bus Cycles for Maximum Mode of 8086

When the 8086 works in the maximum mode of operation, the bus controller 8288 is also employed. The three status signals  $\overline{S}_0$ ,  $\overline{S}_1$  and  $\overline{S}_2$  generated by 8086 are applied to the bus controller 8288. The 8288 gives a number of output signals as shown in Fig. 2.9.  $\overline{MRDC}$  is memory read and  $\overline{MWTC}$  is memory write. These signals can be used for memory read and memory write operation respectively. Similarly,  $\overline{IORC}$  is for I/O read and  $\overline{IOWC}$  is for I/O write operation. These signals can be used for I/O read and write operation respectively. DEN, ALE and DT/ $\overline{R}$  also come out from 8288. The DEN is inverted to get  $\overline{DEN}$ . This is applied to the bus transceiver 8286. DT/ $\overline{R}$  is also applied to 8286.

In the timing diagram for the maximum mode of operation the clock,  $AD_0-AD_{15}$ ,  $A_{16}/S_3 - A_{19}/S_6$  and  $BHE/S_7$  are drawn as they have been shown in the timing diagram for the minimum mode of operation. The other signals for the maximum mode of operation are the status signals  $\overline{S}_0$ ,  $\overline{S}_1$  and  $\overline{S}_2$ . Their encoding for various types of bus operations is as shown in Table 2.4. These remain active during  $T_1$ ,  $T_2$  and  $T_4$  and become passive during  $T_3$  and  $T_w$ .  $T_w$  denotes wait state.  $QS_0$  and  $QS_1$  signals should also be shown in the timing diagram for the maximum mode of operation. These indicate the status of the instruction queue as shown in the Table 2.3.

### 2.11 LOCK