

Assignment 1 and 2.

Define microprocessor. What are the essential differences between Von Neumann and Harvard architecture?

A microprocessor is a multipurpose, programmable, clock-driven, register based electronic device that read binary instruction from a storage device called memory, accepts binary data as input and processes data according to those instruction and provides results as outputs.

2nd part :

Although Von Neumann and Harvard architecture are computer architecture for data operation and their organizational process. But the main difference lies in the design of architecture. In Harvard architecture Program Memory instructions and data memory are placed in different segment of the system whereas, In Von neumann architecture, both are placed inside the same block. As a result they have their own merits and demerits in their operations.

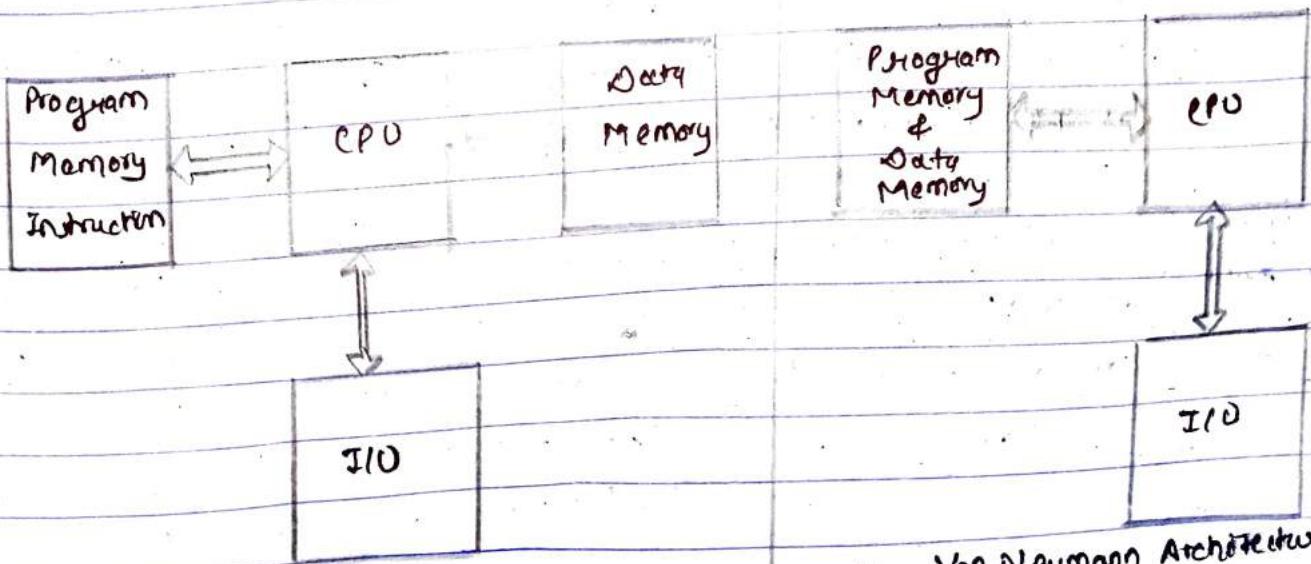


fig : Harvard Architecture.

fig : Von Neumann Architecture.

2. Compare and contrast microprocessor, micro-controller and micro-computer. Explain which is better for high speed operation.

Ans.

Microprocessor	Micro-controller	Micro-computer
<p>Definition: A microprocessor is a the processor on a ^{clock driven semiconductor} single chip called a device consisting of electronic Micro-processor. It is a chips manufactured by using small & low-cost micro- either a LSI or VLSI technique.</p> <p>que.</p>	<p>The processor on a single chip called a Micro-processor. It is a small & relatively inexpensive computer with a microprocessor as its central processing unit (CPU).</p>	<ul style="list-style-type: none"> It is a small & relatively inexpensive computer with a microprocessor as its central processing unit (CPU).
<p>Usage: Can be used in various domain of systems such as PC, embedded system etc.</p>	<p>Mostly used in embedded system.</p>	<p>-</p>
<p>Versatility: Very versatile, as every part can be added to it or removed from it as per requirement.</p>	<p>All the configurations are fixed during its manufacturing time.</p>	<p>-</p>
<p>Speed/ Performance: It is more powerful in its operation, as it can operate from MHz to GHz.</p>	<p>It has less performance compared to microprocessor, which has processor in and can operate in it. So, its performance depends upon the processor used, hard disk used and the memory capacity.</p>	<p>It has less performance It is just a computer compared to microprocessor which has processor in it. So, its performance depends upon the processor used, hard disk used and the memory capacity.</p>

3. Write an 8085 ALP to find out the largest number in an array available from memory location starting from 2500H to 2540H and store the result in register B.

Ans:

LXI H, 2500H

MVI C, 0BH

loop: MOV A, M

INX H

MOV B, M

CMP B

JC skip

MOV B, A

skip DCR C

JNZ loop

HLT

4. Write a program to check 81's complement of the data stored in address 2000H and store the result in 2000H.

Ans. LDA 2000H ; load the number(data) in accumulator.

CMA ; complement number

STA 2000H ; transfer the complement number to 2000H.

HLT. ; stop the program.

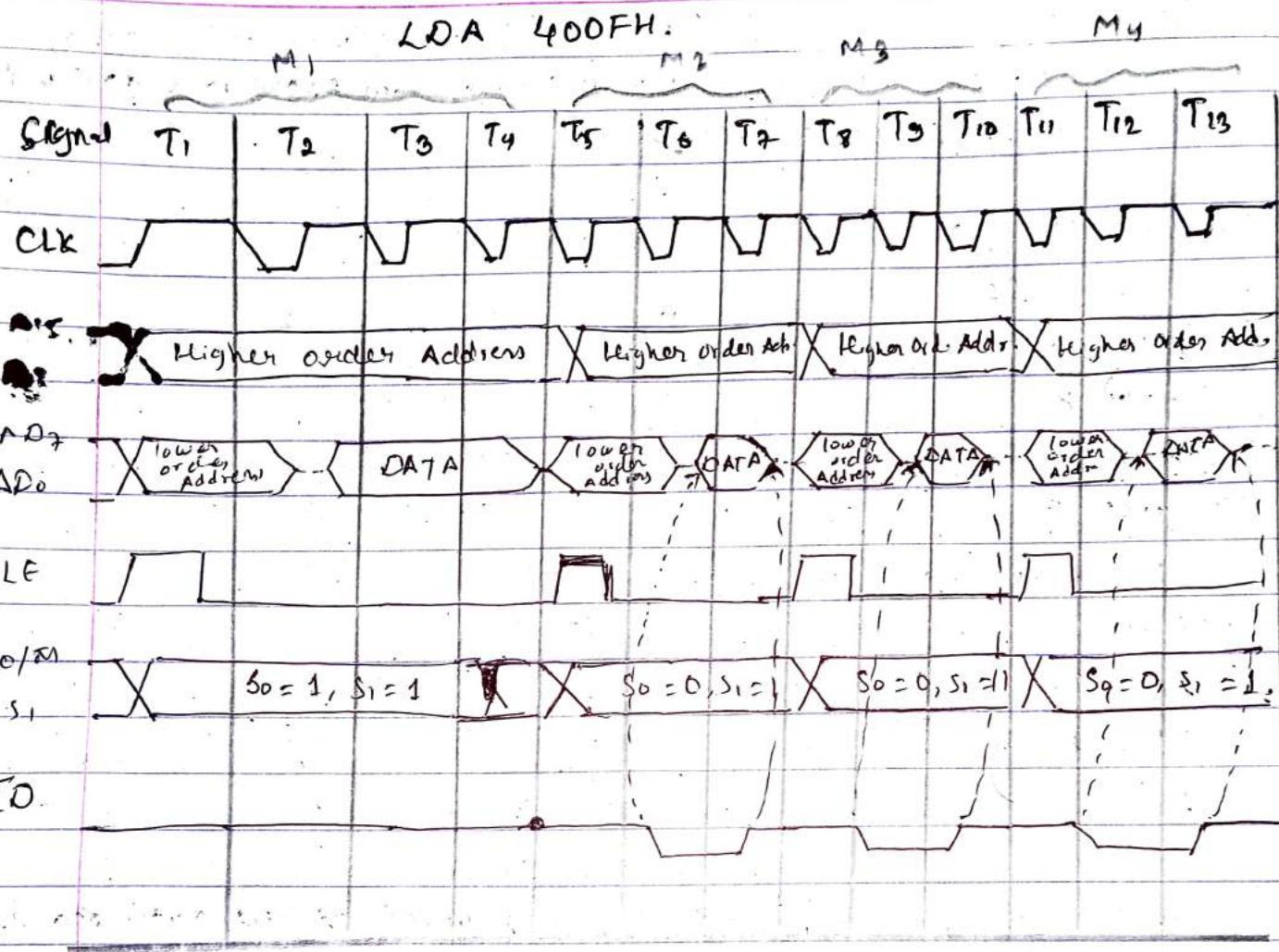
5. Draw the timing diagram for instruction LDA 400FH.

Ans. Here LDA = Load Accumulator Direct.

LDA 400FH is 8 byte instruction, and have 4 machine cycle. i.e. M1 = opcode fetch.

M2 = Read

M3 = Read + M4 = Read.



6. Explain the evolution of Intel series microprocessors from 16-bit processor to 64-bit processor.

Ans. The evolution of Intel series microprocessors from 16-bit processor to 64-bit processor are described below :

16-bit microprocessor:

8086

- Introduced in 1978.
- First 16 bit microprocessor.
- Clock speed is 5 to 10MHz.

- Data bus is 16-bit and address bus is 20-bit.
- It had 29k transistors.
- Used in: CPU of microcomputer.

8088:

- Introduced in 1979.
- It is also 16-bit processor.
- Could execute 0.5 million instruction per second.

80286:

- Introduced in 1982.
- Clock speed was 8 MHz.
- Could address 16MB of memory.
- Could execute 1 million instruction per second.

32-bit processor:

80386:

- First 32-bit processor.
- Could address 4GB of memory.
- Clock speed varied from 16MHz to 83MHz, depending upon version.
- Different versions:
 - 80386 DX.
 - 80386 SX etc.

80486:

- Had 1.2 million transistor.
- Clock speed varied from 16MHz to 100MHz.
- 8kB of cache memory was introduced.

Pentium I, II, III, & Pentium IV.

- Cache memory was increased upto 0.56KB from 8KB.
- Clock speed increased from 1GHz to 3GHz.
- Had increased in number of millions of transistors.

Intel Dual core

- Introduced in 2006.
- Has 2 cores.
- Suppored SMT (Simultaneously Multithreading Technology).

64 Bit Microprocessors:

Intel Core 2

- Introduced in 2006.
- First 64 bit processor.
- Clock speeds from 1.2GHz to 3GHz.
- Has 291 million transistors.

Intel Core i7

- Introduced in 2008.
- Has 4 physical cores.
- Clock speeds from 2.66GHz to 3.33GHz.
- Has 781 million transistors.

Intel Core i5

- Has 4 physical cores.
- Has 781 million transistors.

Intel core i9.

→ Introduced in 2017.

→ Has 10 physical cores.

→ Clock speed from 2.3 GHz to 4.5 GHz.

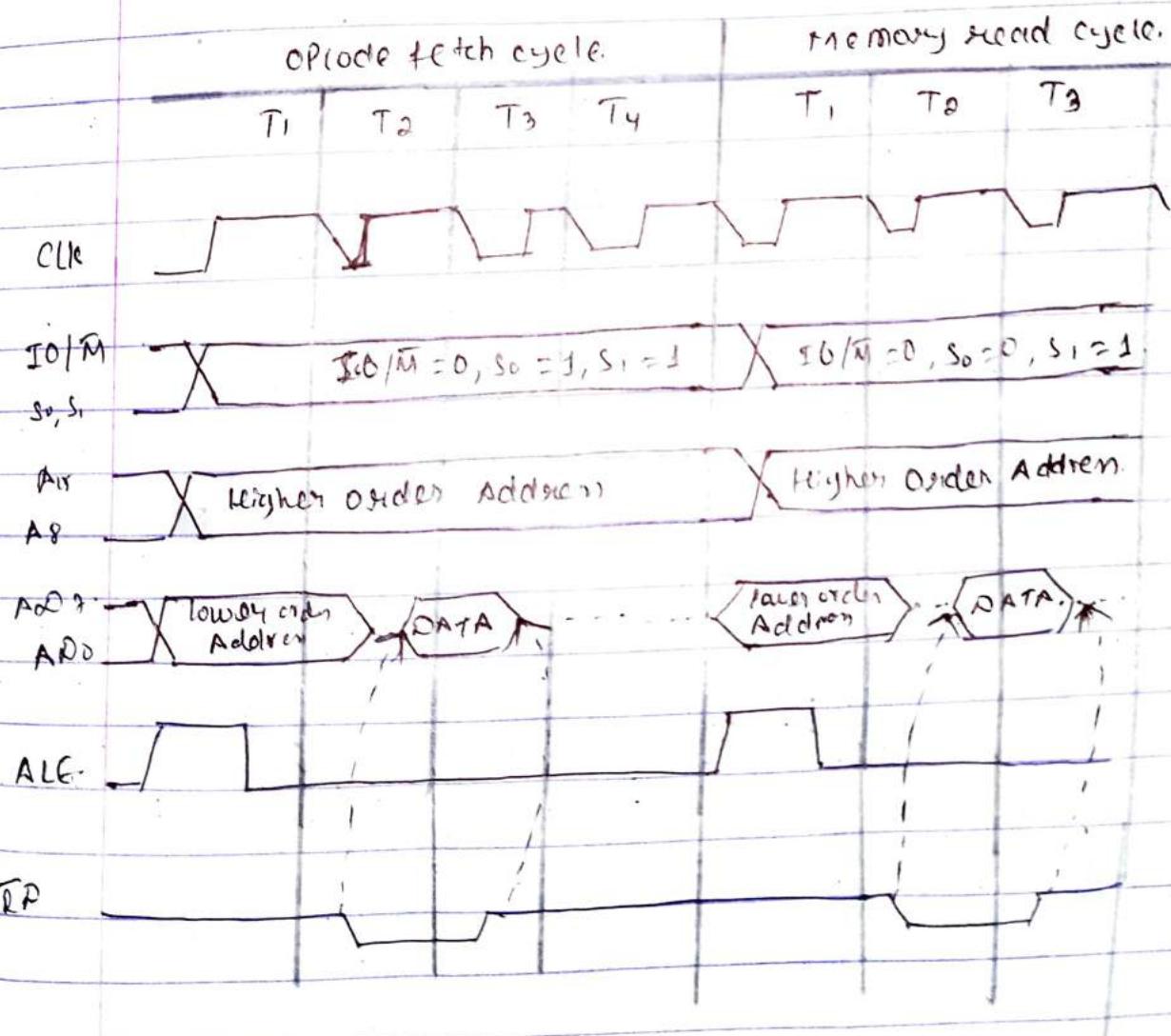
→ Has around 7 billion transistors.

7. Draw a timing diagram of:

a) ADD 45H (b) MVI 17,32H.

Ans. Here, ADD 45H is of 2 byte code and has 2 machine cycle.

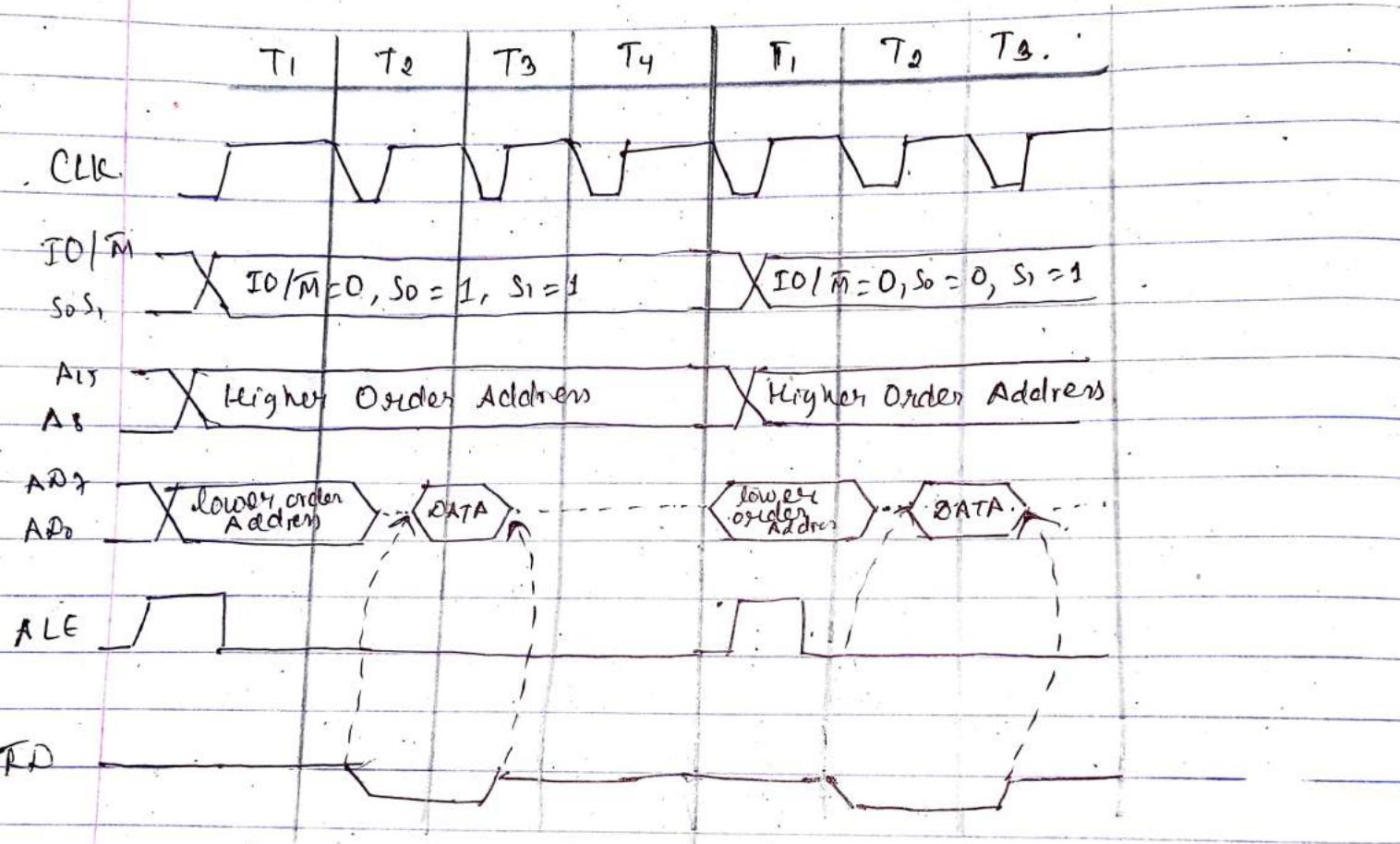
Where, T1 = Opcode fetch & T2 = Read cycle.



→ MVI M, 32H

It is a two byte instruction and will have 2 machine cycle.

M₁ = Opcode fetch and M₂ = Read cycle.



8. Why various addressing modes are used in microprocessor?

Describe addressing mode of Intel 8085 with examples.

Ans. Addressing modes are used in microprocessor in order to specify / express operand differently in the instruction expression.

In 8085, there are 5 ways of specifying operands in the expression, which are described below:

a. Immediate Addressing Mode:

In this mode, the data ~~is~~ are specified in the instruction itself. The data will be part of program instruction.
Ex: MVJ A, 05H ; ADD 55H.

b. Register Addressing Mode:

If the data is present in the register and the register are specified in an instruction, then it is called register addressing mode.

Ex: MOV A,B ; ADD B.

c. Direct Addressing mode:

In this mode, the address of the data is specified in the instruction. The data will be in memory.

Ex: STA 2000H, LDA 4000H.

Indirect

d. Register Indirect Addressing mode:

If the register pair which contains the address of data is specified in the instruction, then it is called register indirect addressing mode.

Ex: LDAX B, STAX D etc.

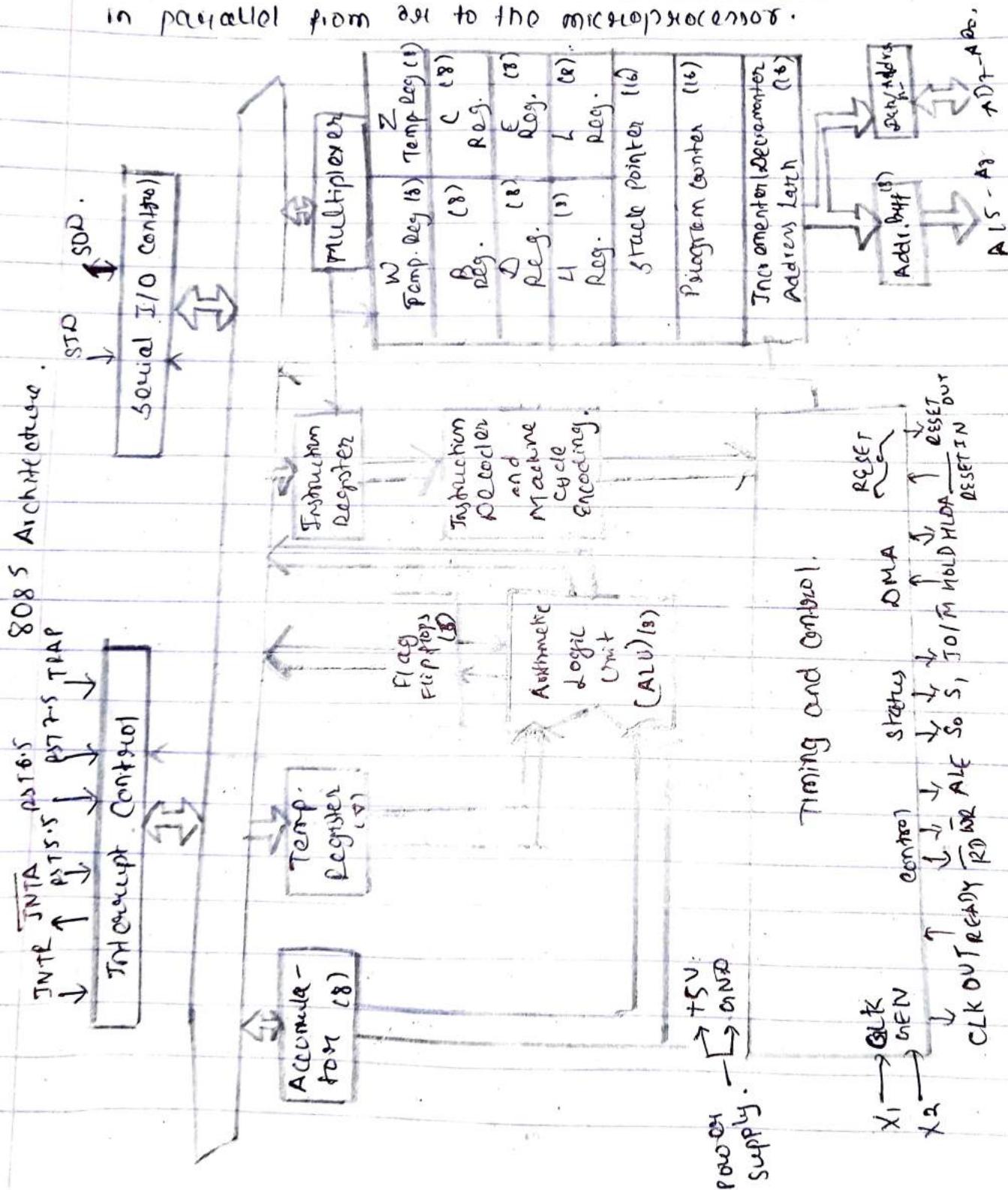
e. Implied Addressing Mode:

If the opcode in an instruction tells about the operand, then it is called implied addressing mode.

Ex: RAL, RRC etc.

Q. Why Intel 8085 is called 8 bit microprocessor? Describe architectural details of 8085 with diagram in brief.

Ans. The Intel 8085 is called 8 bit microprocessor Because it's data bus is 8-bit wide and hence 8-bit data can be transmitted in parallel from memory to the microprocessor.



Description of different segment of 8085 block diagram:

- Accumulator:

It is a 8 bit general purpose register. It is connected to ALU. So, most of the operations are done in Accumulator.

- Temporary Register:

It is not available for user. All the arithmetic and logical operations are done in the temporary register but user can't access it.

- Flag Register:

It is an 8-bit register which consists of 5 flip-flops used to know status of various operation done.

- Timing and Control unit:

This unit synchronizes all the microprocessor operations with the clock and generates the control signals necessary for communication b/w the microprocessor and peripherals.

- Instruction Register and Decoder:

The instruction register and decoder are part of ALU. When an instruction is fetched from memory, it is loaded in the instruction register. The decoder decodes the instruction and establishes the sequence of events to flow.

- Interrupt control:

It accepts different interrupts like TRAP, RST 55,

RST 6.5, RST 7.5 and INTR. Here, INTA is interrupt acknowledgement signal.

Serial IO Control:

It is used to accept and send the serial 1 bit data by using SID and SOD signals and it can be performed by using SIM and RIM instructions.

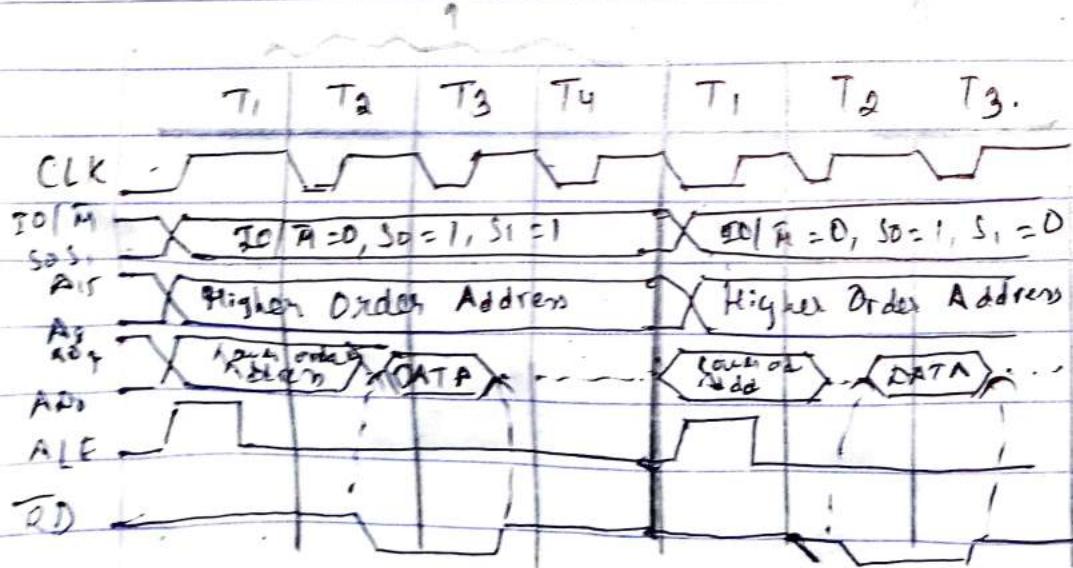
Register Array:

- W, Z registers are Temporary Registers are not available to user.
- B, C, D, E, H and L are general purpose register.
- SP (stack pointer) is a 16-bit register which holds the stack during stack operation.
- PC (Program Counter) is a 16-bit register which holds the address of next instruction to be fetched.

10. Draw and explain the timing diagram of ORI 14H in 8085.

Ans. Here, ORI 14H is 2 byte instruction and will have 2 machine cycles.

M₁ = opcode fetch and M₂ = memory read.



11. Write a program to copy the content of "TBL1" which contains 10 numbers in "TBL2"?

Ans.

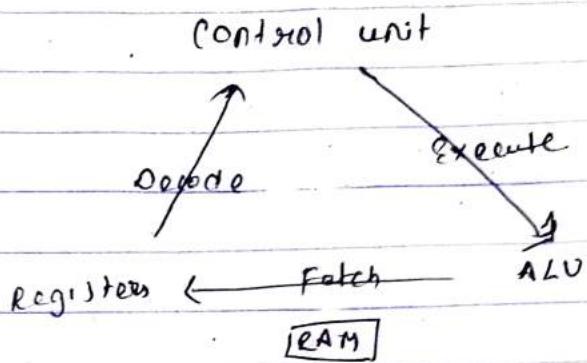
12. Explain fetch, decode, execution process in an instruction cycle.

Ans. The main job of CPU is to execute programs using the fetch-decode-execute cycle (also known as instruction cycle). This cycle begins as soon as we turn on the computer.

To execute the program, the program code is copied from secondary storage into the main memory. The CPU's program counter is set to the memory location where the first instruction in the program has been stored, and execution begins. The program is now running.

In a program, each machine code instructions take up a slot in the main memory. These slots (or memory locations) each have a unique memory address. The program counter stores the address of each instruction and tells the CPU in what order they should be carried out.

When a program is being executed, the CPU performs the fetch-decode-execute cycle which repeats over and over again until reaching the STOP instruction.



13. Explain the bus configuration of 8085/8086 microprocessor.

ANS. To define, A bus is a path or a collection of wires or lines that carries data, address and control signals.

There are three buses in Microprocessors:

a. Address Bus.

b. Data Bus.

c. Control Bus.

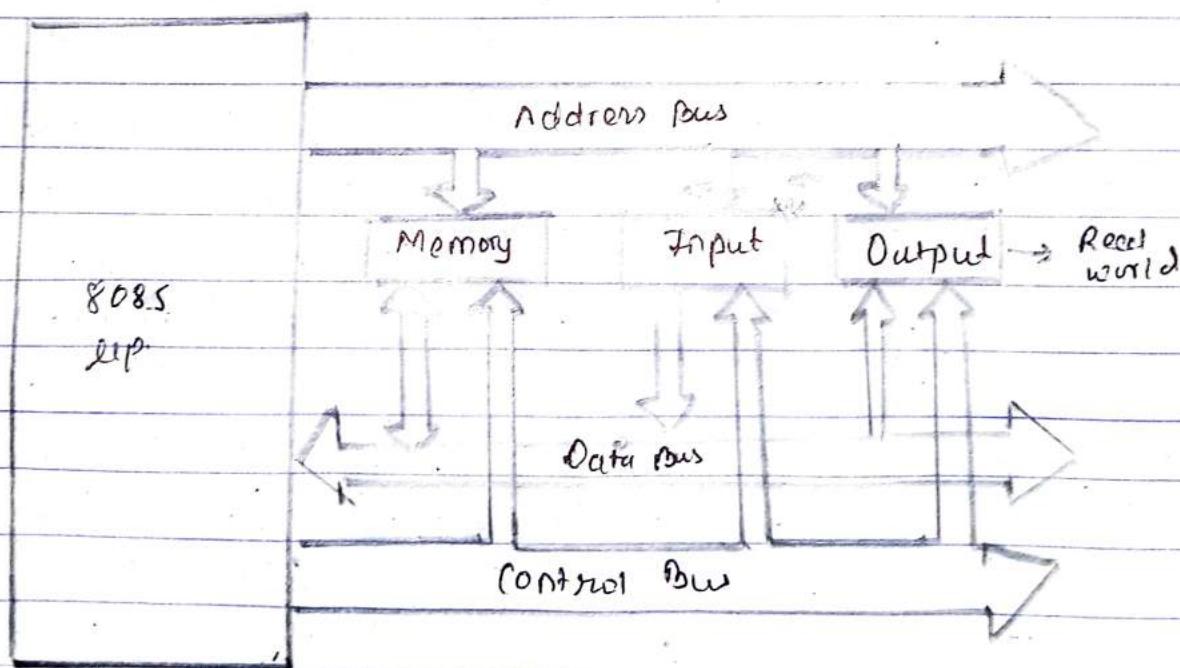


fig : Bus structure of 8085 CPU.

a. Address Bus:

The bus over which the CPU sends out the address of the memory location is known as Address bus. In 8085 UP, Address bus is of 16-bit width.

b. Data Bus:

8085 microprocessor has 8 bit data bus. The data bus are the path in UP which carries in and out data to the microprocessor.

c. Control Bus:

This bus carries control signals and directs the operation in the microprocessor.

8086 Bus can be categorized into two types:

- a. Synchronous Bus.
- b. Asynchronous Bus.

Synchronous Bus:

- In a synchronous Bus, the occurrence of the events on the bus is determined by the clock.
- The clock transmits a regular sequence of 0's and 1's of equal duration.
- It doesn't make use of performance, as the occurrence is determined by clock.
- Is easy to implement.

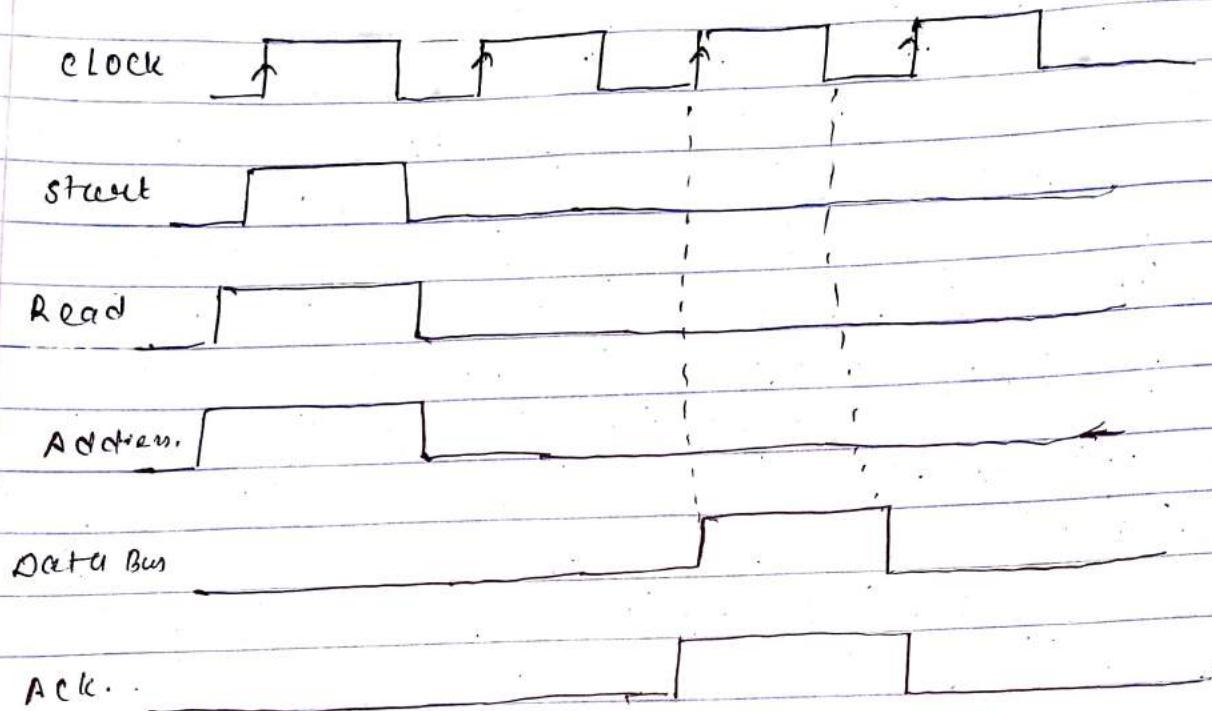


fig : synchronous Read operation.

b. Asynchronous ~~operation~~^{bus}:

→ In asynchronous operation, timing is maintained in such a way that the occurrence of event in bus depends upon the occurrence of previous event.

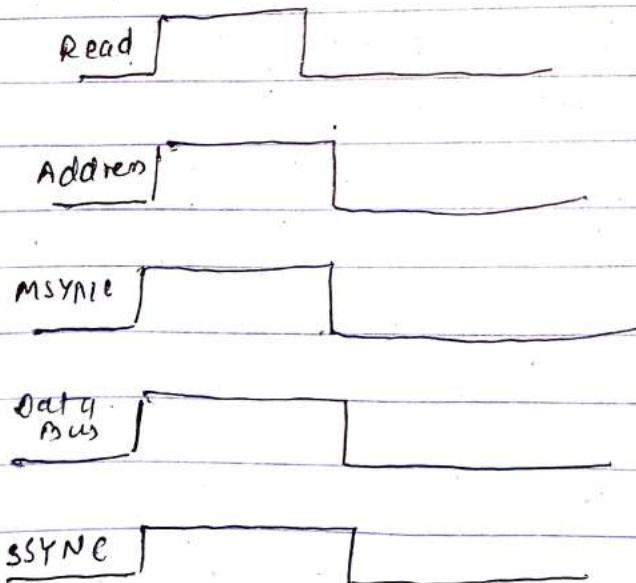


fig : Asynchronous Bus.

Q1. What are the greatest breakthroughs achieved in the successive development of microprocessor? List with their features.

Ans. In the evolution of microprocessor, there had been several breakthroughs in terms of performance/speed, operation and its power consumption and size. To list a few, following can be the improvements:

- Improved in performance: Initially CPU were very slow and were used in small operations only but now they are used in very large system to handle complex & time consuming operations. Their speed have reached to GHz from MHz.
- Improved in operation: As CPU got evolved its architecture get revised several times, and to enhance its operation capability, several new registers (memory) were introduced, the concept of caching is also added. Later on improved their capacity sizes too, which eventually improved the capability of CPU. As well as the numbers of transistors were made to millions and billions, which made microprocessor capable to execute millions of instructions per second.

Hence, in this way microprocessor had evolved over the time by making improvements and changes in several aspects of the chip.

15. WAP in 8085 to count the number of positive, negative and zero in a given series of data. The length of series is given at address 203FH and the series starts from 2040H; store your result at 2060H onwards.

Ans.

~~LDAX~~ 203FH ; read the length

~~STA~~ C ; move length value to Register C.

LXI H, 2040H

MVI B, 00H ; Initialize negative number count.

MVI D, 00H ; Initialize positive " "

MVI E, 00H ; Initialize zero number count.

begin: MOV A, M

CPI 00H ; compare if zero.

JZ zero

ANI 80H ; If MSB of number = 1 i.e. if negative.

JNZ negative.

INR D ; otherwise increase positive number count.

JMP last

zero: INR E ; increase zero number count.

JMP last

negative: INR B ; increase negative number count.

last: INX H

DEC C

JNZ begin.

LXI H, 2040H

MOV M, D ; store the positive number count

INX H

MOV M, B ; store the negative number count

INX H

MOV M, E ; store the zero number count

HLT.

16. Draw and explain the timing diagram of LDA 8050H instruction.

Ans. (Repeated Question, as same as of Q.5).

17. Describe the following PIN of 8085.

a) ALE, RST, HOLD, HLDA, and INTA.

Ans.

ALE: It is Address Latch Enable, one of the control signals of 8085. ALE is a positive going pulse generated when a new operation is started by the microprocessor. When the pulse goes high, it indicates address. When the pulse goes down it indicates data.

RST: RST are reset interrupt. They are RST 7.5, RST 6.5, RST 5.5. Also it can be discussed as RESET IN and RESET OUT; where RESET IN signal is used to reset the microprocessor by setting the program counter to zero. Whereas, the RESET OUT signal is used to reset all the connected devices when the microprocessor is reset.

HOLD: This signal indicates that another master is requesting the use of address and data buses.

HLDA (HOLD Acknowledge): It indicates that the CPU has received the HOLD request and it will relinquish the bus in the next clock cycle. HLDA is set to low after HOLD signal is removed.

INTA : It is an interrupt acknowledge signal. So, its main task is to acknowledge an interrupt coming to the microprocessor.

18. Write an 8085 assembly program to add six bytes of data : 23H, 41H, 56H, AFH, CFH and A7H ; and place the sum and carry in memory location 2500H and 2501H respectively.

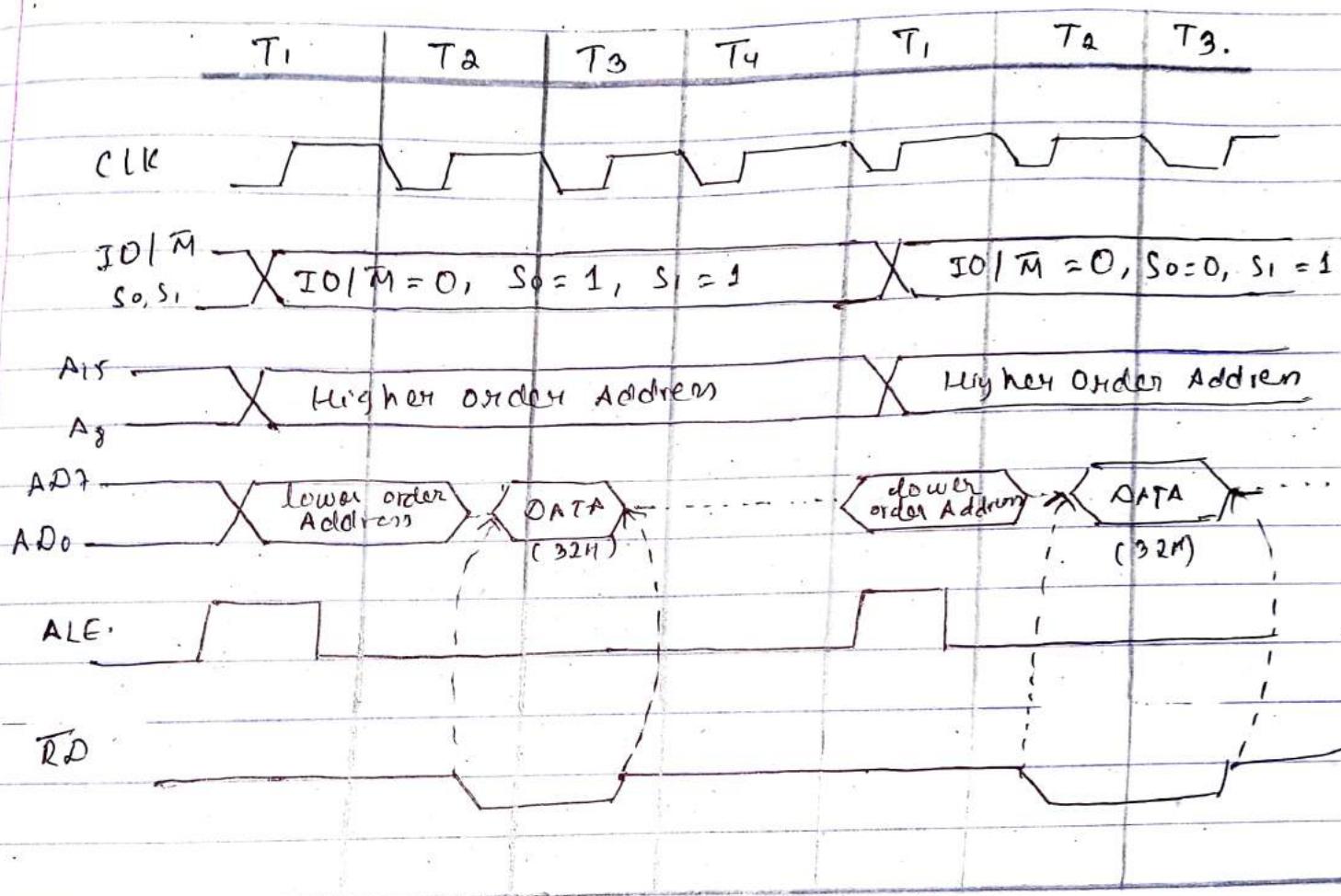
Ans.

```
MVI A, 23H  
ADD 41H  
JNC here  
INR C  
here: ADD 56H  
JNC here2  
INR C  
here2: ADD AFH  
JNC here3  
INR C  
here3: ADD CFH  
JNC here4  
INR C  
here4: ADD A7H  
JNC here5  
INR C  
here5: STAX 2500H  
MOV A, C  
STAX 2501H
```

19. Draw the labelled diagram for the instruction MVI A, Data i.e. You can assume any. data of 8 bit in length.

Ans. Let's assume DATA = 32H.

since, MVI A, 32H is a two byte instruction and will have 2 machine cycles, M_1 = Opcode fetch and M_0 = Read cycle.



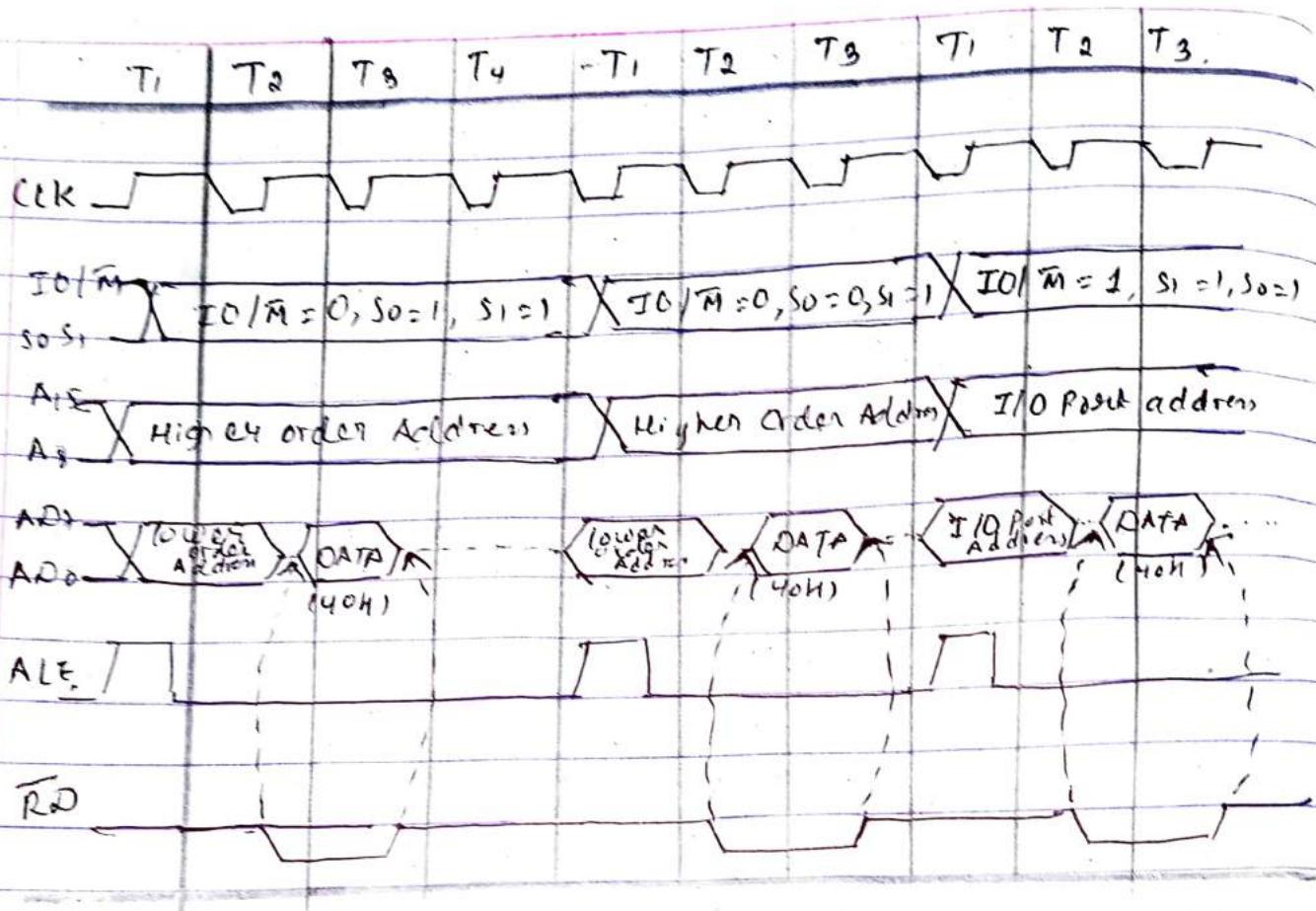
20. Draw and explain the timing diagram for the 8085 instruction IN 40H.

Ans. IN instructions inputs data to accumulator from a port of 8-bit address. The command IN 40H is 2 byte instruction and has three machine cycles, where;

M_1 = opcode fetch

M_2 = Machine Read

M_3 = I/O Read.



Q1. Write an ALP to count number of 1's in given byte.

Ans. MVI B, 00H

MVI C, 08H.

LXI H, 4000H.

main: MOV A, M

RAL

JNC loop

INR B

loop: INX H

~~DCR C~~

~~loop~~: JNZ main

MOV A, B.

HLT.

Q2. WAP to check given number is odd or even.

Ans. LDA 2050H

ANI 01H ; performs AND operation betⁿ accumulator A and
01 and store the result in A.

JZ ~~here~~ ; jump to memory locaⁿ

MVI A, 11H ; assign 11 to accumulator

JMP here2

here1: MVI A, 22H

here2: STA 3050H

HLT

[let us suppose our data is in 2050H location.
If even we had stored 22H at memory location 3050H
otherwise stored 11 at memory location 3050H]

Q3. Draw the block diagram of 8085 microprocessor and explain in brief..

Ans. (Repeated question, already done in Q. 3).

Q4. Classify the instruction according to its categories. Explain any five data transfer instruction.

Ans. In 8085, its instruction can be categorized in 6 types:

a. Data transfer Instruction.

b. Arithmetic Instruction.

c. Logical Instruction set.

d. Rotate Instruction set.

e. Branching Instruction.

f. Machine control Instruction.

Any 5 data transfer instruction are described below:

		example
→	MOV Rd, Rs MOV Rd, M MOV M, Rs.	copies (moves) the content from the source (Rs, M) to destination (Rd, M)
→	MVI Rd, 8 bit MVI M, 8 bit	Immediately copies the given data to register / memory.
→	LDA 16-bit (Load Accumulator Direct).	Copies the content of memory location specified by 16-bit address into A.
→	STA 16-bit (Store Accumulator Direct).	Copies the content of A into specified 16-bit memory address.
→	IN 8-bit.	The data from i/p port specified by 8-bit address is transferred into A.

25. Explain the register organization of 8085.

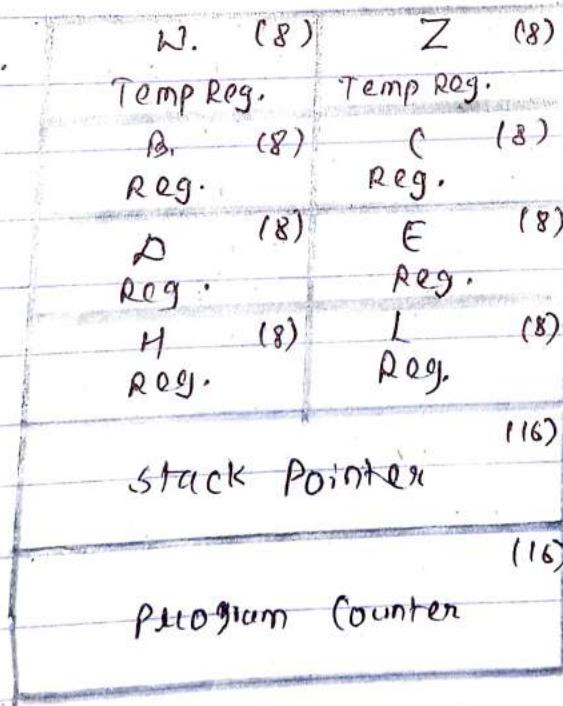
Ans. In 8085 there are several registers which are used for different purposes. To categorize; we have:

- a. Temporary Registers (W, Z): These are not available for user. These are loaded only when there is an operation to be performed.

General purpose Registers: There are six 8-bit general purpose register in 8085 namely B, C, D, E, H and L. Those are used for various data manipulations. They can be used in pairs as 16-bit registers. The register pairs are; BC pair, DE pair and HL pair. Special purpose: There are two;

- SP (stack pointer): It is a 16-bit register used to hold the address of stack during stack operation i.e. PUSH and POP operation.

- PC (Program Counter): It is a 16-bit register which holds the address of next instruction to be fetched. When a single byte instruction is executed PC is automatically incremented by 1. Upon reset PC contents are set to 1000H.



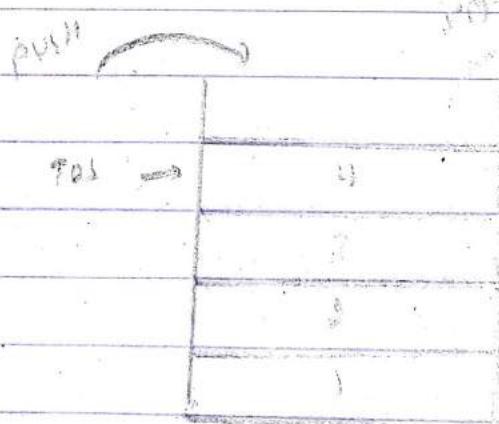
Registers of 8085 CPU

26. What is stack? Draw and explain stack memory with example.

Ans. The stack is a LIFO (last in, first out) data structure implemented in the RAM area and is used to store addresses and data when the microprocessor branches to a sub-routine. Then the return address used to get pushed on this stack. Also to swap values of two registers and register pairs, stacks are used.

e Program Counter (PC).

In stack, two special registers Stack Pointer (SP) plays a crucial role. The stack pointer register will hold the address of the top location of the stack. And the program counter register, always hold the address of memory location from where the next instruction for execution will have to be fetched.



On a stack, we can perform two operations, PUSH and POP. In case of push operation, the SP register gets decremented by 2 and new data item used to insert on to the top of the stack. On the other hand, in case of pop operation, the data item will have to be deleted from the top of stack and SP register will be increased by 2.

Fig: Interpretation of SP content.

27. Why the lower order address bus is multiplexed with data bus?

How they will be Demultiplexed?

Ans The main concern in digital electronics is to reduce the space required for building the electronic chip. Reduction of space means reduction of cost and building a efficient electronic circuits.

In 8085, the main reason of multiplexing address and data bus is to reduce the number of pins for address and data and ~~dedicate~~ dedicate those pins for other several functions of microprocessor. These multiplexed set of lines used to carry the lower order 8 bit address as well as data bus.

The lower order address bus and data bus can be demultiplexed by enabling/disabling ALE. When ALE is high (enable) then lower order address bus is selected, i.e. A₀-A₁₅ is achieved (as A₈-A₁₅ is already enabled). Whereas when ALE is made low (disable) then the data bus is selected.

In this way, demultiplexing can be done.

28. Write instructions to load the hexadecimal number 65H in register C and 92H in accumulator A. Display the number 65H at PORT0 and 92H at PORT1.

Ans. MVI C, 65H

MVI A, 92H.

OUT PORT1.

MOV A, C.

OUT PORT0.

HLT.

29. What is the output at PORT1 when the following instruction are executed? Also state the status of flag after execution.

MVI A, 8F

ADJ 72H

JL DISPLAY;

OUT PORT1

HLT

DISPLAY: XRA A

OUT PORT1

HLT,

Ans.

$$\begin{array}{r} 8F \Rightarrow 10001111 \quad AC = 1 \\ + 72 \quad + 01110010 \\ \hline 100000010101 \\ \text{P} \quad \underbrace{0} \quad \underbrace{\cancel{1}}_{= 05H} \end{array}$$

so we get carry so we will go to DISPLAY label.

XRA A. = Exclusive OR Accumulator.

We have, content of Accumulator = 05H.

30. Specify the contents of the registers and the flag status as the following instructions are executed.

Ans.

i. MVI A, 00H ; A = 00H

ii. MVI B, F8H ; B = F8H.

iii. MOV C, A ; C = 00H.

iv. MOV D, B ; D = F8H.

v. HLT.

flag status will be same, as there is no carry or zero.