MID-SEMESTER EXAMINATION, November-2025
Computer System Organization-1 (CA3121)

Program: MCA
Full Marks: 30

Semester: 1st
Time: 2 Hours

Subject/Course Learning Outcome	*Taxonomy Level	Ques. Nos.	Marks
CO1- Able to state and explain different number systems, binary codes.	L1	1	6
CO2- Able to apply the principles of Boolean algebra, Karnaugh map Method to simplify logic expressions and implement it using gates.	L2	2,3	12
CO3-Able to analyze and design various combinational circuits	L3	4,5	12

*Bloom's taxonomy levels: Remembering (L1), Understanding (L2), Application (L3), Analysis (L4), Evaluation (L5), Creation (L6)

Answer all questions. Each question carries equal mark.

1.	(a)	Convert to hexadecimal and then to binary: $(757.25)_{10}$	2
	(b)	Convert the given number to a base 7 number $(324.43)_5$	2
	(c)	Represent in 1's complement form of the following number (i) -12 (ii) +9	2
2.	(a)	Which gates are known as universal gates and why ?	2
	(b)	Draw the logic circuit of the expression Y= A'B'C+AB'+BC using basic logic gates.	2
	(c)	Implement Y= A'+BC' only using NAND Gate.	2
3.	(a)	Find the complement of given function (a) F(A, B, C) = AB(B'C' + AC)	2

	(b)	Minimize the following expression using Boolean algebra F=(A'+B)(A+B+D)D'	2
	(c)	Consider the following minterms expression F: $F(P, Q, R, S) = \Sigma(0,2,5,7,8,10,13,15)$. What is the minimal sum-of-products form for F?	2
4.	(a)	For the following expression draw the K map and find minimum POS form of the expression $F(A, B, C, D) = \sum m(0,2,4,5,6,8) + \sum d(1,3,7,10)$.	2
	(b)	Write the truth table for Full Adder and design the circuit using logic gates	2
	(c)	Design Full Adder circuit using Half Adder and OR gate.	2
5.	(a)	Design a 3 bit 1's complement circuit. Write the truth table.	2
	(b)	Find out the minimized output expressions. Draw the circuit.	2
	(c)	Write the truth table for 8X1 MUX. Design 8X1 MUX using 4x1 MUX and 2X1 MUX.	2
		End of Questions	