Final Report

Computer Architecture FA22

We modeled our CPU from the one given in the book, with some alterations to allow for additional instructions to be created. While we were unable to implement the entire CPU, we did accomplish implementation for all I, R, and B types, as well as lw, sw, and JAL. We attempted to add the peripherals, but were unable to test our peripherals.s file.

Block Diagrams:

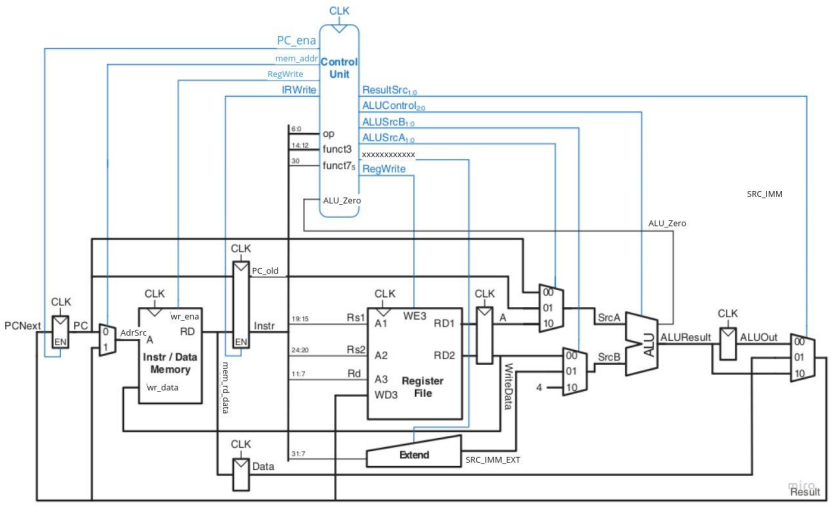

Figure 1: OBJMulticycle ProcessorOBJ

Figure 2: Multicycle Processor with data path for execute R

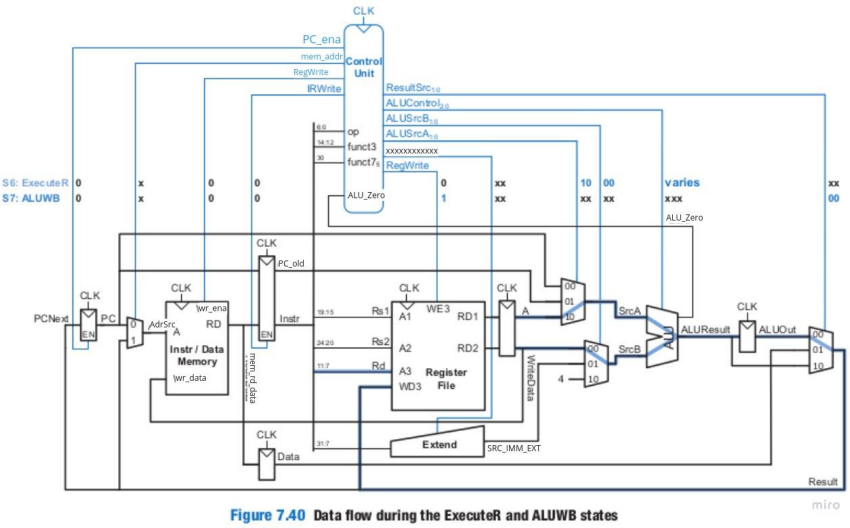

Figure 7.40 Data flow during the ExecuteR and ALUWB states

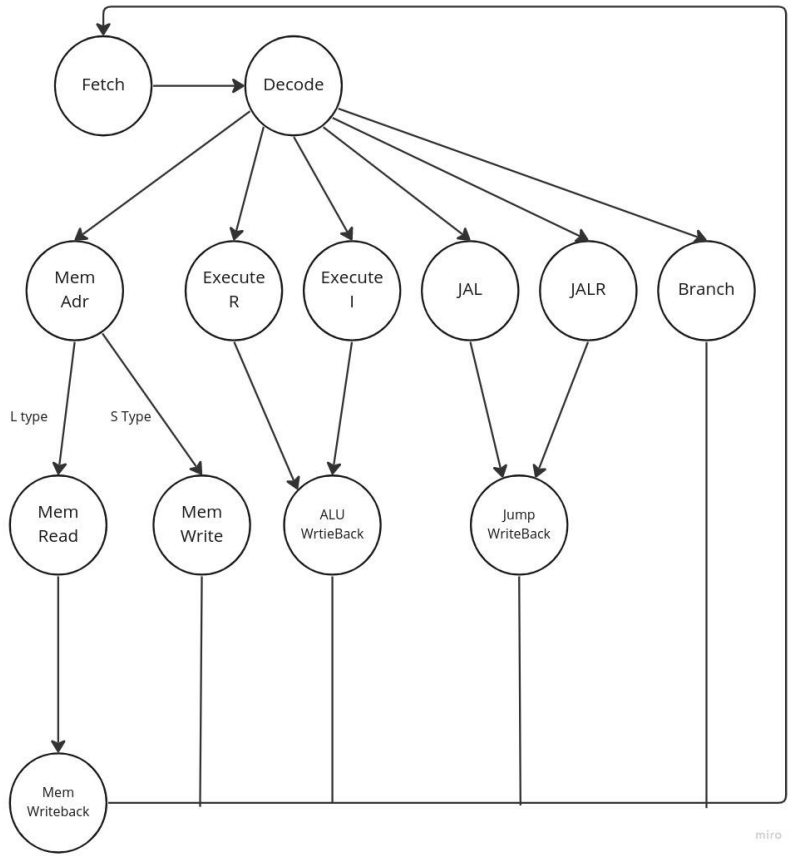

Figure 3: Our FSM