



1. Description

1.1. Project

Project Name	si4468_Receiverss
Board Name	NUCLEO-L4A6ZG
Generated with:	STM32CubeMX 6.6.1
Date	10/26/2022

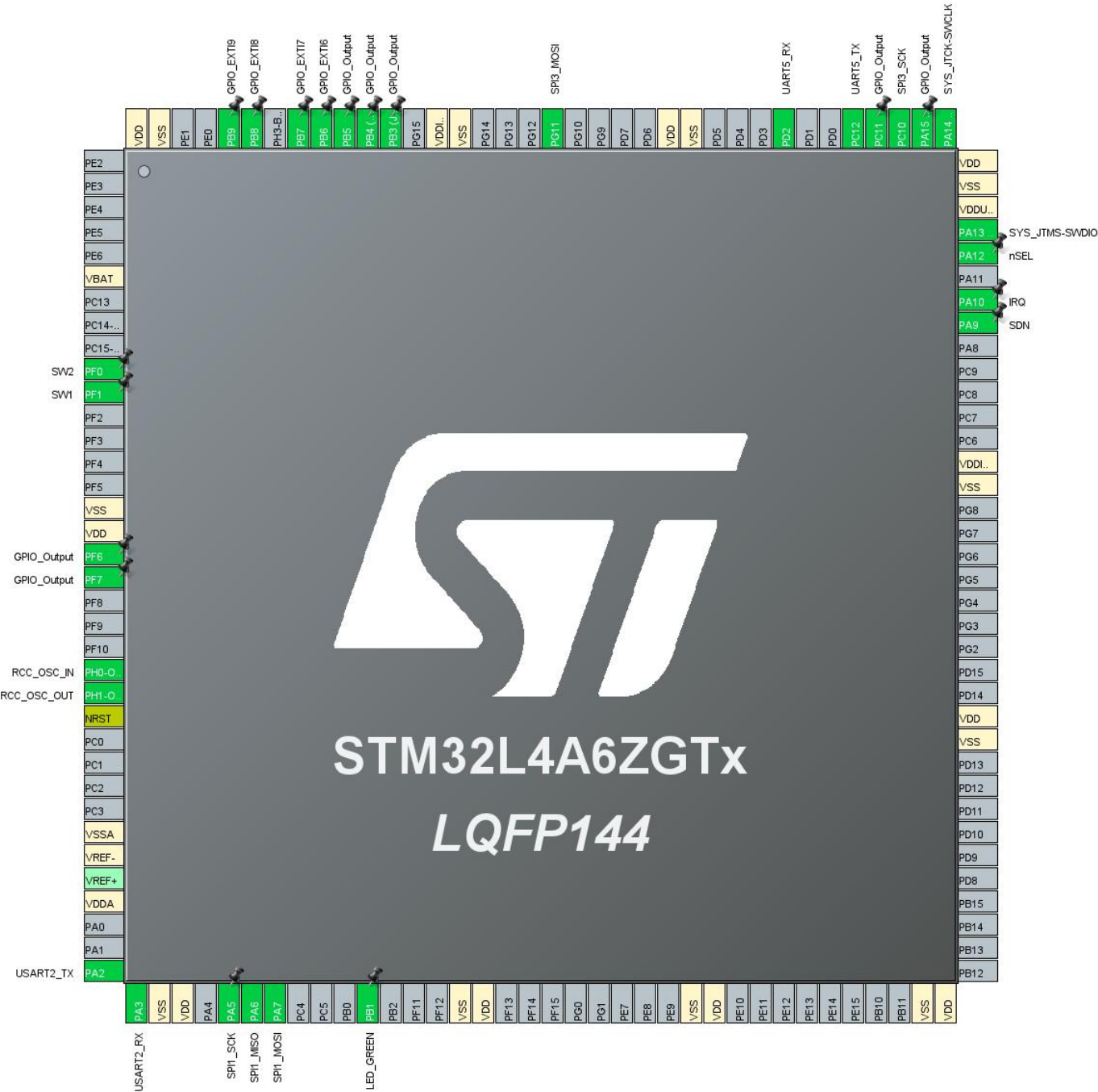
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L4A6ZGTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration



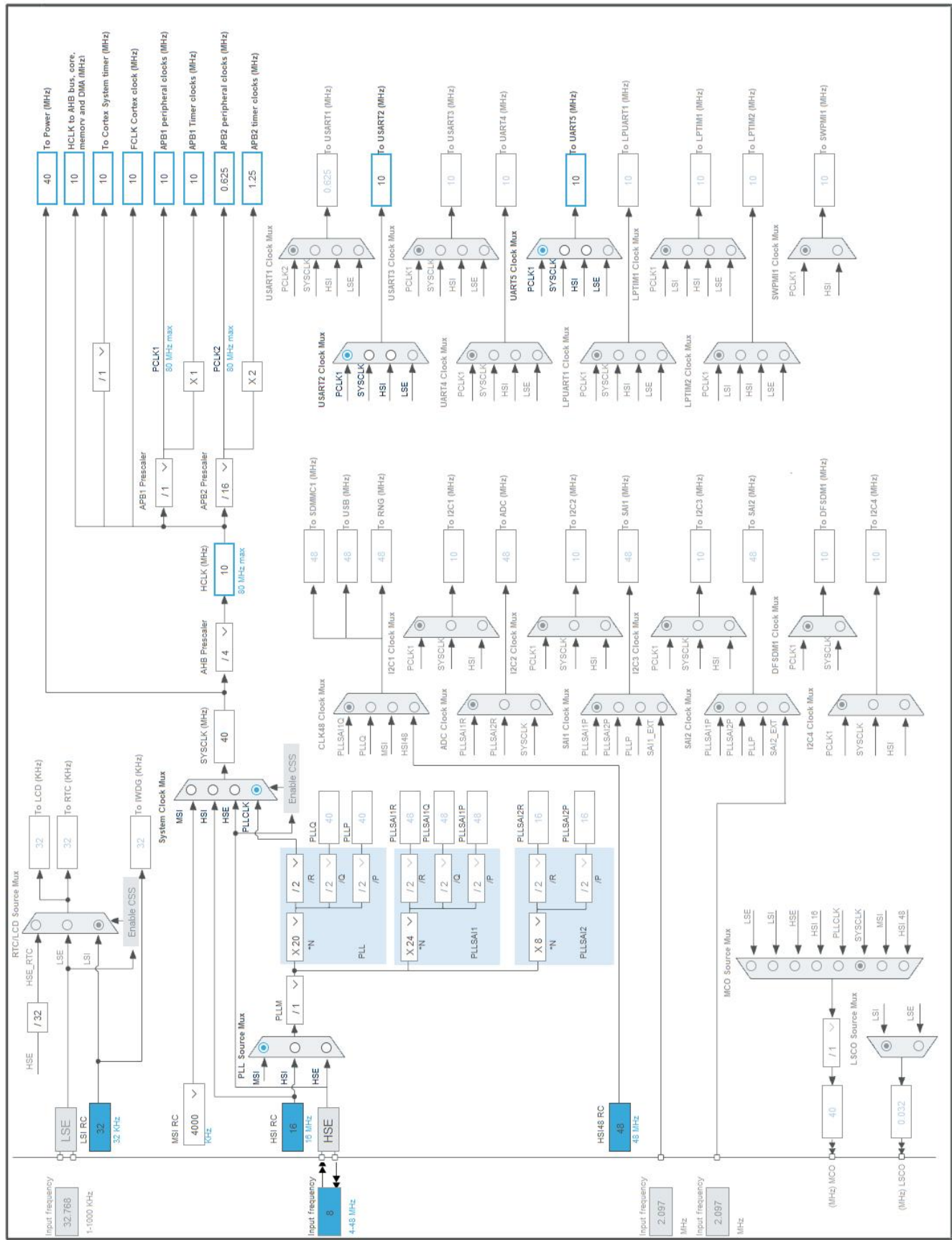
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
10	PF0 *	I/O	GPIO_Input	SW2
11	PF1 *	I/O	GPIO_Input	SW1
16	VSS	Power		
17	VDD	Power		
18	PF6 *	I/O	GPIO_Output	
19	PF7 *	I/O	GPIO_Output	
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VSSA	Power		
31	VREF-	Power		
33	VDDA	Power		
36	PA2	I/O	USART2_TX	
37	PA3	I/O	USART2_RX	
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	SPI1_MOSI	
47	PB1 *	I/O	GPIO_Output	LED_GREEN
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VSS	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDIO2	Power		
101	PA9 *	I/O	GPIO_Output	SDN
102	PA10 *	I/O	GPIO_Input	IRQ
104	PA12 *	I/O	GPIO_Output	nSEL
105	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	
106	VDDUSB	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	
110	PA15 (JTDI) *	I/O	GPIO_Output	
111	PC10	I/O	SPI3_SCK	
112	PC11 *	I/O	GPIO_Output	
113	PC12	I/O	UART5_TX	
116	PD2	I/O	UART5_RX	
120	VSS	Power		
121	VDD	Power		
126	PG11	I/O	SPI3_MOSI	
130	VSS	Power		
131	VDDIO2	Power		
133	PB3 (JTDO/TRACESWO) *	I/O	GPIO_Output	
134	PB4 (NJTRST) *	I/O	GPIO_Output	
135	PB5 *	I/O	GPIO_Output	
136	PB6	I/O	GPIO_EXTI6	
137	PB7	I/O	GPIO_EXTI7	
139	PB8	I/O	GPIO_EXTI8	
140	PB9	I/O	GPIO_EXTI9	
143	VSS	Power		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	si4468_Receiverss
Project Folder	D:\Rapi_dev_isf\workspaces\cubeide_workspace\si4468_Receiverss
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_SPI1_Init	SPI1
5	MX_USART2_UART_Init	USART2
6	MX_UART5_Init	UART5
7	MX_SPI3_Init	SPI3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L4A6ZGTx
Datasheet	DS11584_Rev2

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

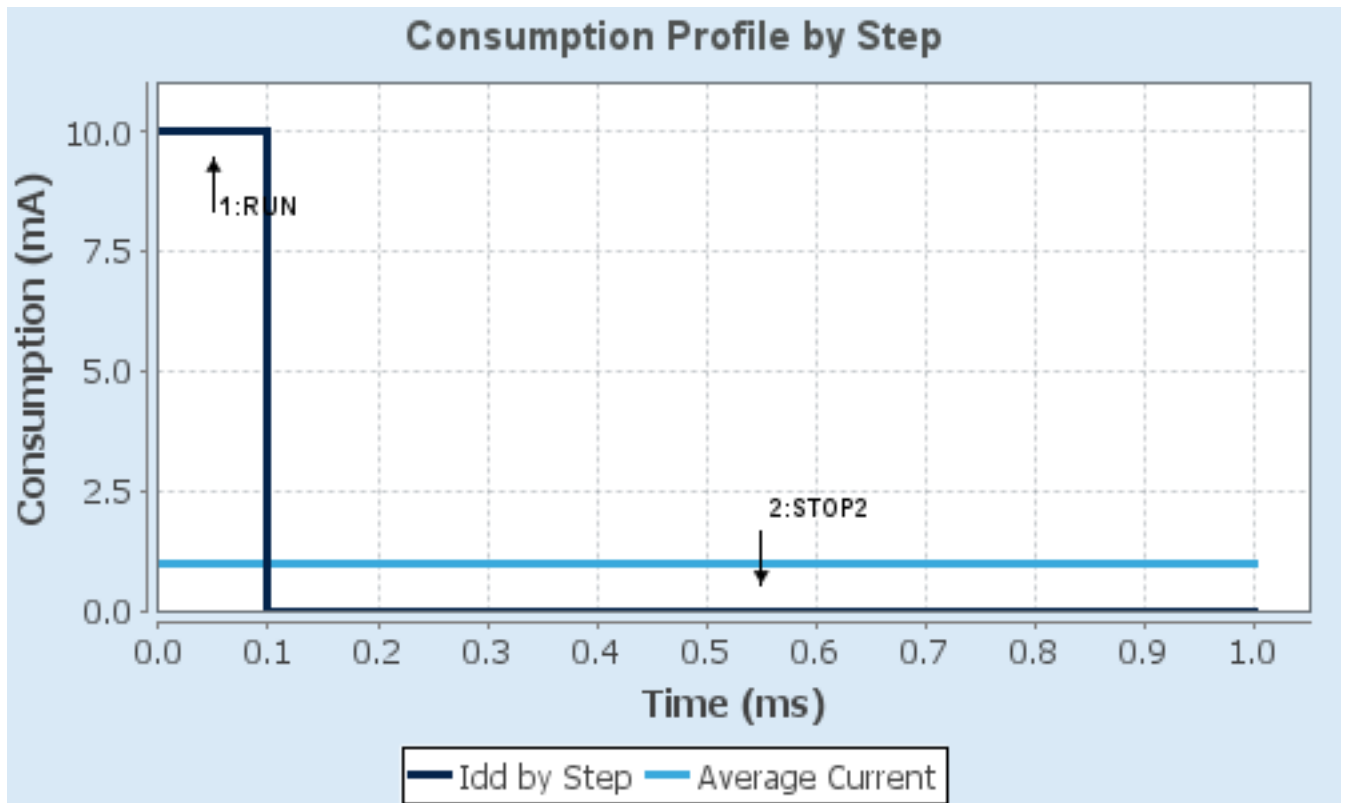
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10 mA	2.69 μ A
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	104.04	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1 mA
Battery Life	4 months, 19 days, 3 hours	Average DMIPS	100.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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7.2. SPI1

Mode: Full-Duplex Master

7.2.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits *
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	312.5 KBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.3. SPI3

Mode: Half-Duplex Master

7.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits *
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	5.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. UART5

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.6. USART2

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Medium *	
	PA6	SPI1_MISO	Alternate Function Push Pull	Pull-down *	Medium *	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Medium *	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PG11	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
UART5	PC12	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD2	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PF0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SW2
	PF1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SW1
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SDN
	PA10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IRQ
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	nSEL
	PA15 (JTDI)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB3 (JTDO/TRACESWO)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB4 (NJTRST)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PB7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PB8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PB9	GPIO_EXTI9	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
UART5_RX	DMA2_Channel2	Peripheral To Memory	Low

UART5_RX: DMA2_Channel2 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line[9:5] interrupts	true	0	0
DMA2 channel2 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
SPI1 global interrupt	unused		
USART2 global interrupt	unused		
SPI3 global interrupt	unused		
UART5 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line[9:5] interrupts	false	true	true
DMA2 channel2 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA ✓			SPI1 ✓			
GPIO ✓			SPI3 ✓			
IVIC ✓			UART5 ✓			
RCC ✓			USART2 ✓			
SYS ✓						

10. Docs & Resources

Type	Link
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
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Flyers	https://www.st.com/resource/en/flyer/flnucleolrwan.pdf
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Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstmcsuite.pdf
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- Application Notes https://www.st.com/resource/en/application_note/an4621-stm32l4-and-stm32l4-ultralowpower-features-overview-stmicroelectronics.pdf
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