S_0

111 → RF_A1
RF_D1 → T1
RF_D1 → Mem_Add
Mem_Data → T2

T1_Wr
T2_Wr

S_1

T2(11→9) → RFA1
T2(8→6) → RFA2
RF_D_1 → T3
RF_D_2 → T4
T1 → or T2(8→0) —SE→ RF_D_3
T2(11→9) → RF_A3

T3_Wr
T4_Wr
Rf_Wr, A_3 MUX_Sel
D3_MUX_Sel

S_2

T2(8→0) —SE→ or T3 → ALU_A
T2(5→0) —SE→ or T4 → ALU_B
ALU_C → T3
ALU_ZF → Z_F
ALU_CF → CF

Depending on Op_code
ADD or NAND or XIR
T3_WR
Z_Ctrl
C_Ctrl

S3

T1 → ALU_A
T2(8→0) —SE→ or +1
ALU_C → RF_D_3
111 → RF_A_3

ADD
RF_Wr

S4

T3 → Mem_Address
Mem_Data → RF_D3
T2(11→9) → RF_A3

RF_Wr

S5

T3 → Mem_Address
T4 → Mem_Address

Mem_Wr

S6

T3 → Mem_Address
Mem_Data → RF_D3
Loop_Count(2→0) → RF_A3
Loop_Count → ALU_A
+1 → ALU_B

Rf_Wr
ADD

S7

T3 → ALU_A
+2 → ALU_B
ALU_C → T3

T3_WR

S8

T3 or T1 or T2(8→0) —7S→ or T4 → RF_D_3
T2(5→3) or T2(11→9) or 111 → RF_A_3

Rf_WR

S9

Loop_Count(2→0) → RF_A1
RF_D1 → Mem_Data_In
T3 → Mem_Address
LoopCount → ALU_A
+1 → ALU_B
ALU_C → Loop_Count

Mem_Wr
ADD