# IITB RISC MULTI-CYCLE IMPLEMENTATION

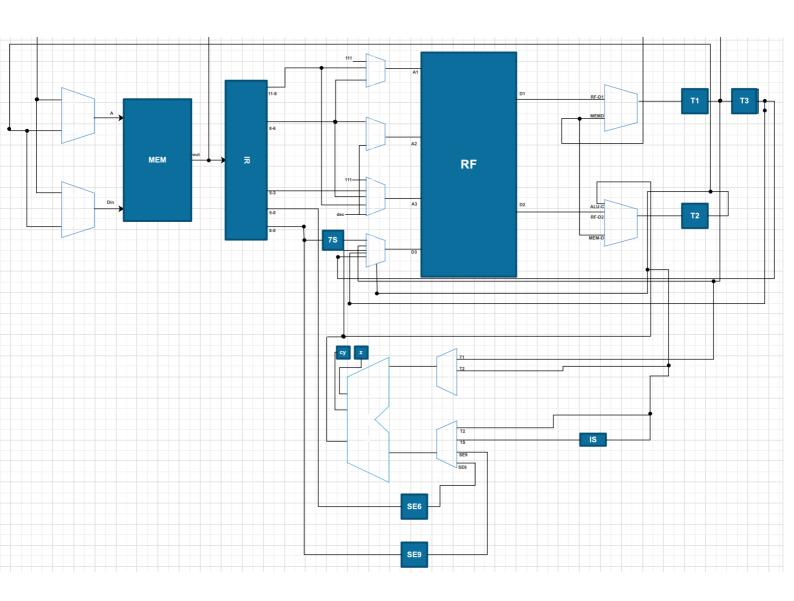
#### **TEAM MEMBERS**

- 1) ANUBHAV BHATLA
- 2) HARSHVARDHAN
- 3) NEERAJ PRABHU
- 4) OJAS PATIL

#### **COMPONENTS**

- 1) ALU
- **2) MEM**
- 3) 1-BIT SHIFTER
- 4) 7-BIT SHIFTER
- 5) 6-BIT SIGN EXTENDER
- 6) 9-BIT SIGN EXTENDER
- 7) INCREMENTER
- 8) 3-BIT 2X1 MUX
- 9) 8-BIT 2X1 MUX
- 10)3-BIT 4X1 MUX
- 11) 8-BIT 4X1 MUX
- 12) 3-BIT 3X1 MUX
- 13) 8-BIT 8X1 MUX
- **14) 1-BIT REGISTER**
- **15) 16-BIT REGISTER**
- **16) REGISTER BANK**
- **17) MEMORY**

### **DATAPATH**



## **HARDWARE FLOWCHARTS**

init

**NULL** 

SO

'111' ---> RF-A1 RF-D1---> T1

**S1** 

T1—>MEM-A MEM-D—>IR

**S\_1** 

**NULL** 

**S2** 

T1-->inc inc-->RF-D3, T3 '111'-->RF-A3

**S3** 

IR<sub>11-9</sub>—>RF-A1 IR<sub>8-6</sub>—>RF-A2 RF-D1—>T1 RF-D2—>T2

**S4** 

T1-ALU-A T2—>ALU-B ALU-c—>RF-D3 IR5-3—>RF-A3

**S5** 

T1—>ALU-A T2—>IS—>ALU-B ALU-C—>RF-D3 IR5-3—>RF-A3



**S17** dec→RF-A2 RF-D2→T2

**S18** T1—>MEM-A T2—>MEM-D

**S19** T1—>ALU-A T2—>ALU-B

**S\_19** If (z==1) then

**\$20** | '111'-> RF-A1 RF-D1->T1

T1->ALU-A IR5-0->SE6->ALU-B ALU-C-> RF-D3 '111'->RF-A3

**S22** | T3-> RF-D3 | IR<sub>11-9</sub>--> RF-A3

\$23 | T1->ALU-A | IR<sub>8-0</sub>->SE9->ALU-B | ALU-C-> RF-D3 | '111'->RF-A3

**S24** | T2-> RF-D3 '111'-> RF-A3

**S25** | T1->inc inc-> T3

\$26 \( \text{'111'} -> \text{RF-A3} \\ \text{T3} -> \text{RF-D3} \)

#### **INSTRUCTION SET**

