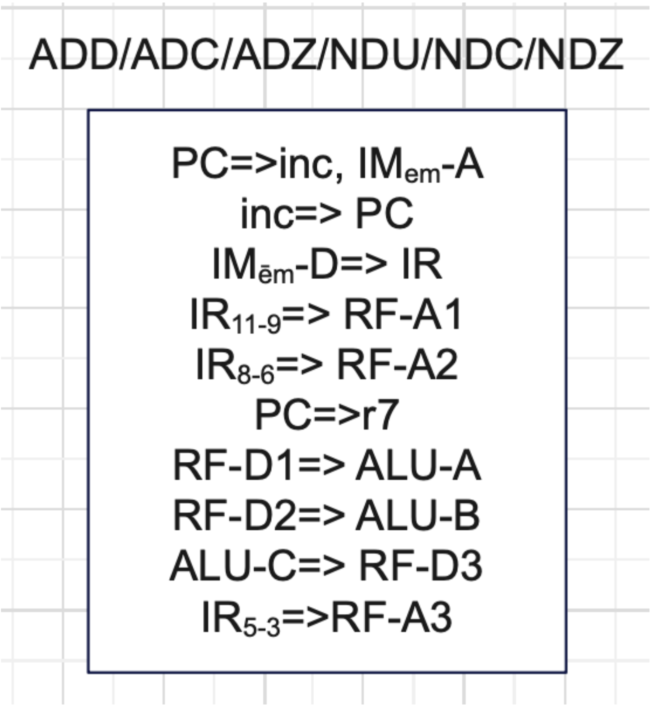
IITB RISC
MULTI-STAGE
PIPELINED MICROPROCESSOR

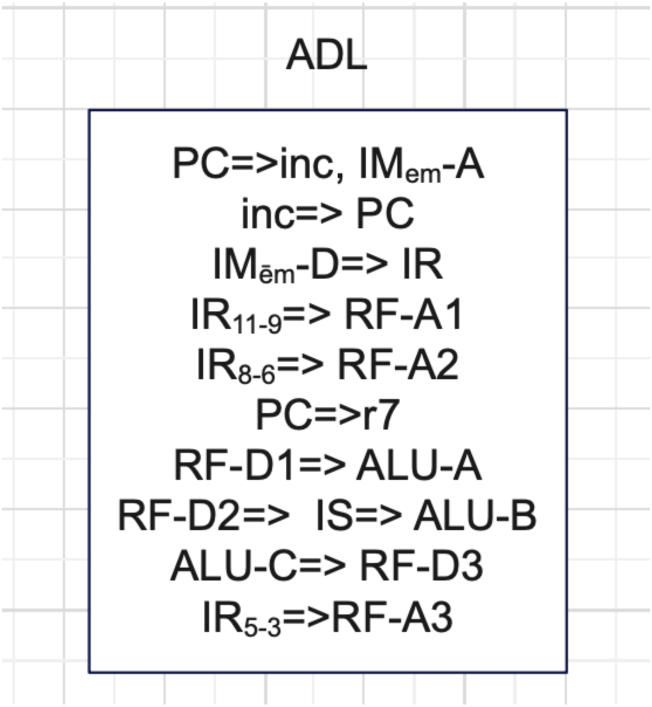
TEAM MEMBERS
ANUBHAV BHATLA
NEERAJ PRABHU
HARSHVARDHAN
OJAS PATIL

FLOW CHARTS



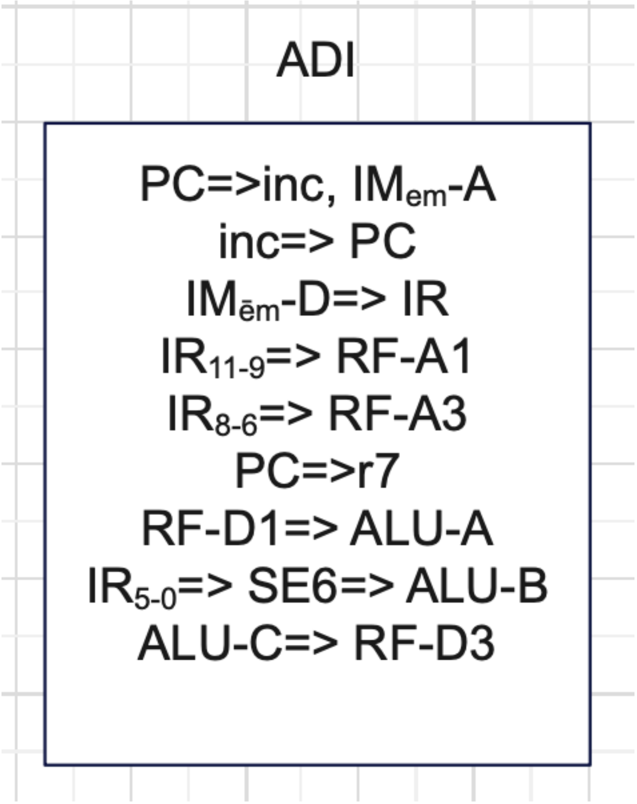
ADD/ADC/ADZ/NDU/NDC/NDZ

PC=>inc, IM$_{em}$-A
inc=> PC
IM$_{\bar{e}m}$-D=> IR
IR$_{11-9}$=> RF-A1
IR$_{8-6}$=> RF-A2
PC=>r7
RF-D1=> ALU-A
RF-D2=> ALU-B
ALU-C=> RF-D3
IR$_{5-3}$=>RF-A3



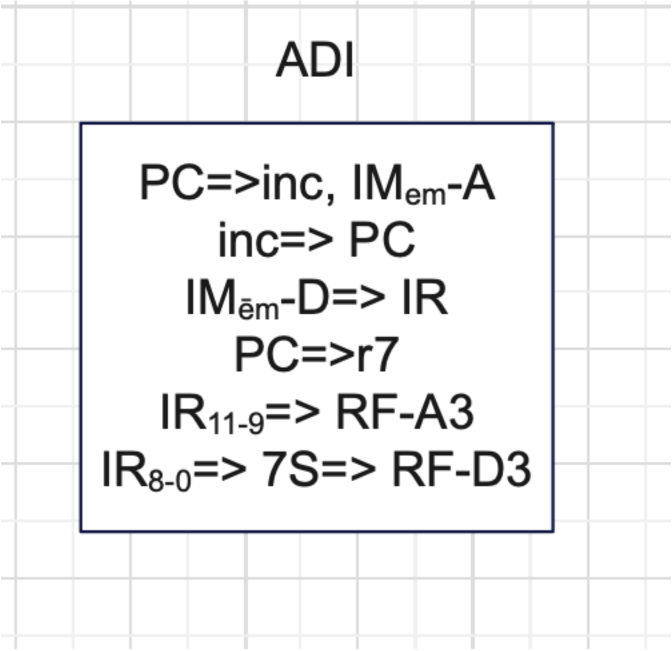
ADL

PC=>inc, IM$_{em}$-A
inc=> PC
IM$_{\bar{e}m}$-D=> IR
IR$_{11-9}$=> RF-A1
IR$_{8-6}$=> RF-A2
PC=>r7
RF-D1=> ALU-A
RF-D2=> IS=> ALU-B
ALU-C=> RF-D3
IR$_{5-3}$=>RF-A3



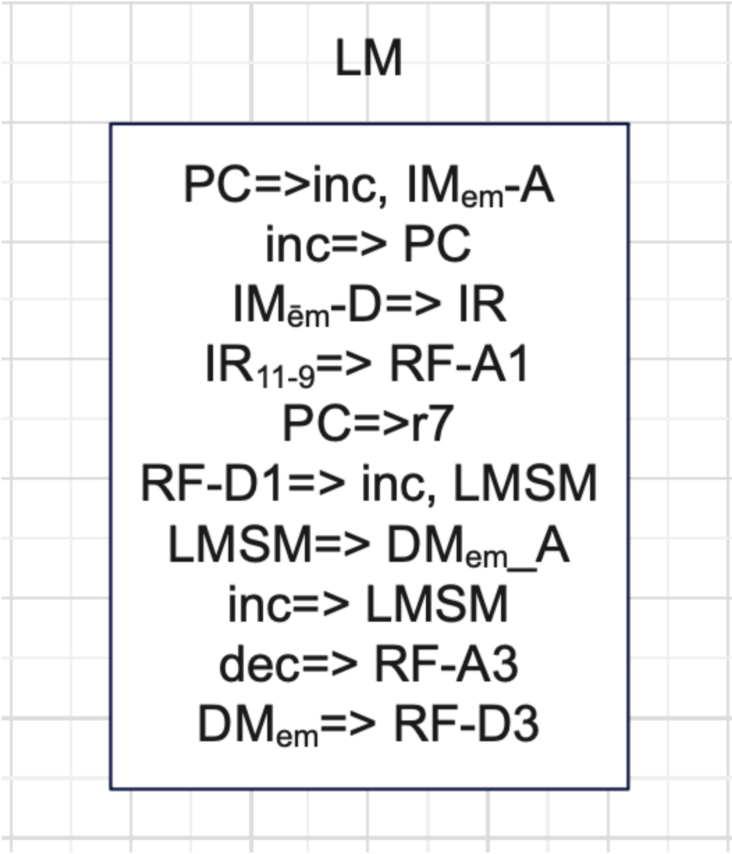
ADI

PC=>inc, IM$_{em}$-A
inc=> PC
IM$_{\bar{e}m}$-D=> IR
IR$_{11-9}$=> RF-A1
IR$_{8-6}$=> RF-A3
PC=>r7
RF-D1=> ALU-A
IR$_{5-0}$=> SE6=> ALU-B
ALU-C=> RF-D3



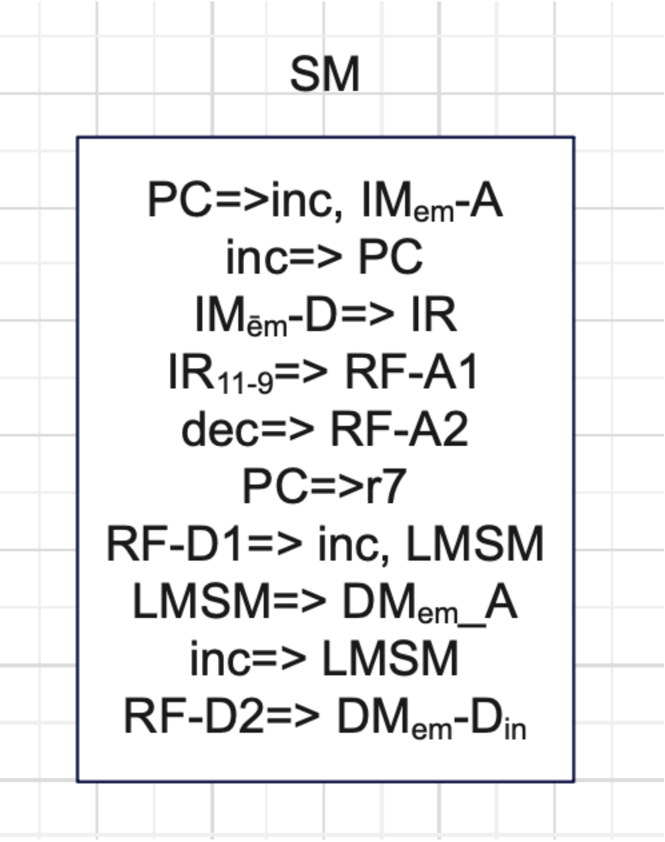
ADI

PC=>inc, IM$_{em}$-A
inc=> PC
IM$_{\bar{e}m}$-D=> IR
PC=>r7
IR$_{11-9}$=> RF-A3
IR$_{8-0}$=> 7S=> RF-D3



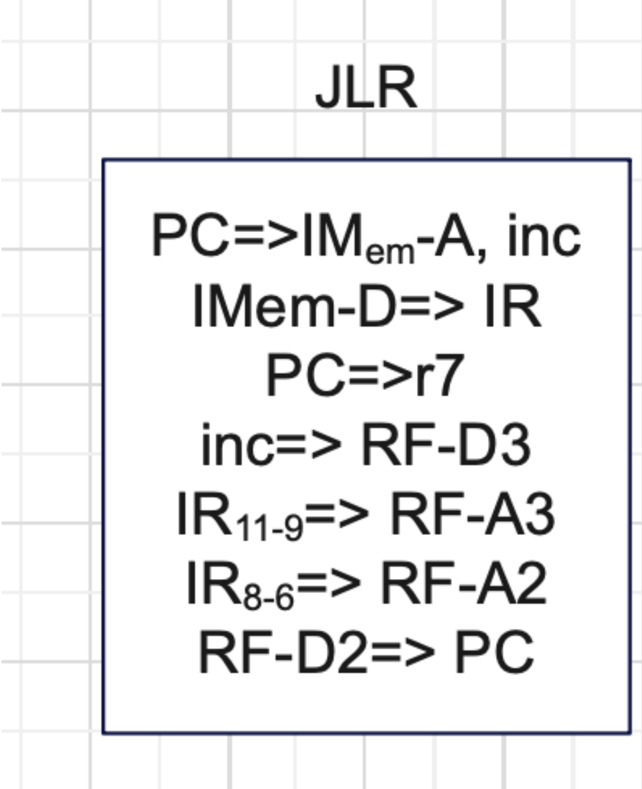
LM

PC=>inc, IM_{em}-A
inc=> PC
$IM_{\bar{e}m}$-D=> IR
IR_{11-9}=> RF-A1
PC=>r7
RF-D1=> inc, LMSM
LMSM=> DM_{em}_A
inc=> LMSM
dec=> RF-A3
DM_{em}=> RF-D3



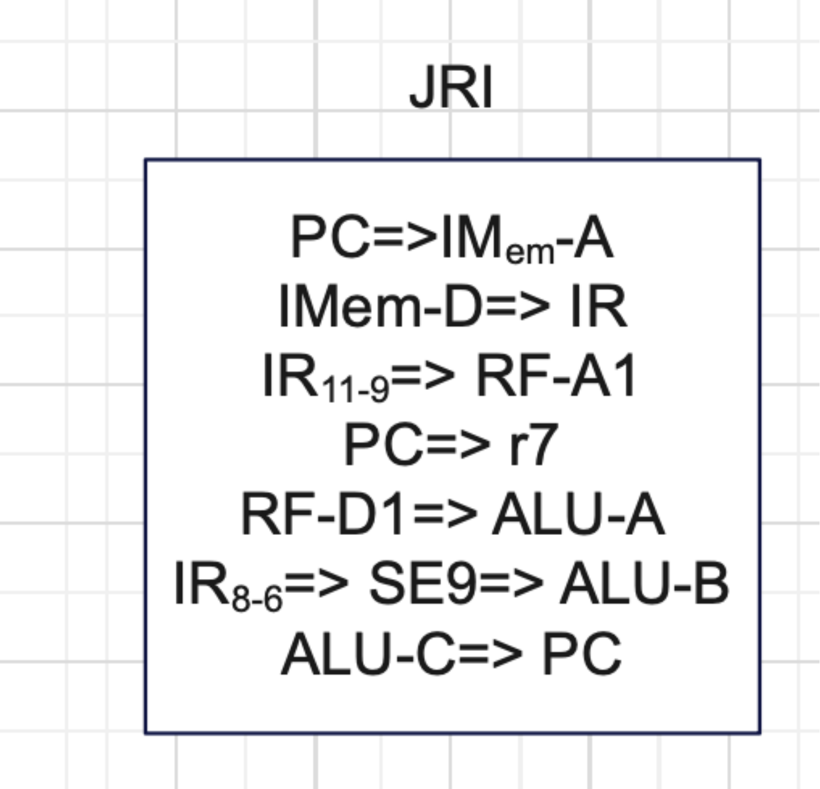
SM

PC=>inc, IM_{em}-A
inc=> PC
$IM_{\bar{e}m}$-D=> IR
IR_{11-9}=> RF-A1
dec=> RF-A2
PC=>r7
RF-D1=> inc, LMSM
LMSM=> DM_{em}_A
inc=> LMSM
RF-D2=> DM_{em}-D_{in}



JLR

PC=>IM_{em}-A, inc
IMem-D=> IR
PC=>r7
inc=> RF-D3
IR_{11-9}=> RF-A3
IR_{8-6}=> RF-A2
RF-D2=> PC



JRI

PC=>IM_{em}-A
IMem-D=> IR
IR_{11-9}=> RF-A1
PC=> r7
RF-D1=> ALU-A
IR_{8-6}=> SE9=> ALU-B
ALU-C=> PC

BEQ

PC=>inc, IM_{em}-A
IMem-D=> IR
$IR_{11\text{-}9}$=> RF-A1
$IR_{8\text{-}6}$=> RF-A2
PC=>r7
RF-D1=> ALU-A
RF-D2=> ALU-B
PC=> ALU2-A
$IR_{5\text{-}0}$=> SE6=> ALU2-B
if ALU-Z==1 then ALU2-C=> PC
else inc=> PC

JAL

PC=>inc, IM_{em}-A
IMem-D=> IR
PC=>r7
INC=> RF-D3
$IR_{11\text{-}9}$=> RF-A3
$IR_{8\text{-}0}$=> SE9=> ALU2-B
PC=> ALU2-A
ALU2-C=> PC

LHI

PC=>inc, IM_{em}-A
inc=> PC
$IM_{\bar{e}m}$-D=> IR
PC=>r7
$IR_{11\text{-}9}$=> RF-A3
$IR_{8\text{-}0}$=> 7S=> RF-D3

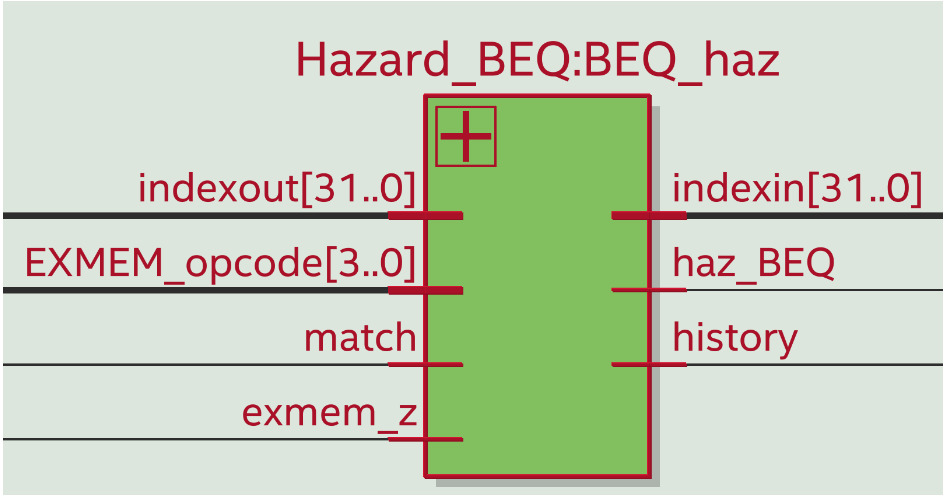
LW

PC=>inc, IM_{em}-A
inc=> PC
$IM_{\bar{e}m}$-D=> IR
$IR_{8\text{-}6}$=> RF-A1
PC=>r7
$IR_{11\text{-}9}$=> RF-A3
RF-D1=> ALU-A
$IR_{5\text{-}0}$=> SE6=> ALU-B
ALU-C=> DM_{em}-A
DM_{em}-D=> RF-D3

HAZARDS

For Hazard detection and mitigation, we have created 7 hazard blocks which work in the following manner:

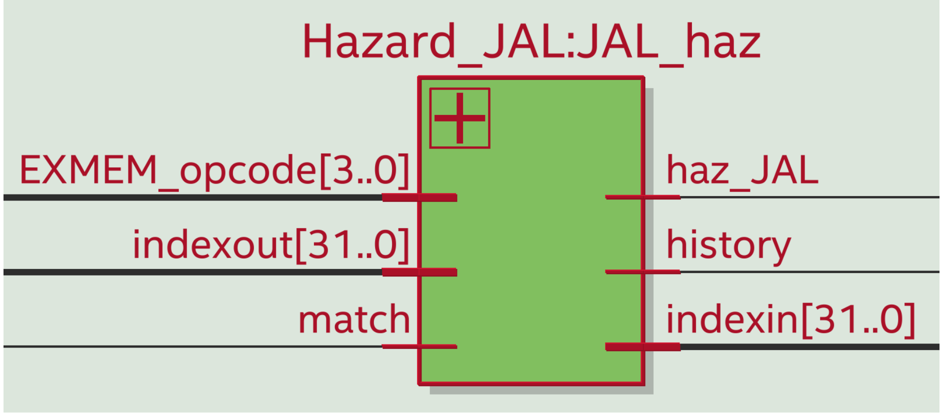
Hazard_BEQ



For the BEQ instruction, we need to branch if the zero flag is set in the Execution stage. Therefore we can have 4 possible cases:

- We predicted the branch as taken (match=’1’), and the branch was taken (EXMEM_z=’1’): The history bit will be set to ‘1’ and the haz_BEQ to ‘0’ since there was no hazard detected.
- We predicted the branch as taken (match=’1’), but the branch was not taken (EXMEM_z=’0’): The history bit will be set to ‘0’ and the haz_BEQ to ‘1’ since there was a hazard detected.
- We predicted the branch as not taken (match=’0’), and the branch was taken (EXMEM_z=’1’): The history bit will be set to ‘1’ and the haz_BEQ to ‘1’ since there was a hazard detected.
- We predicted the branch as not taken (match=’0’), and the branch was not taken (EXMEM_z=’0’): The history bit will be set to ‘0’ and the haz_BEQ to ‘0’ since there was no hazard detected.

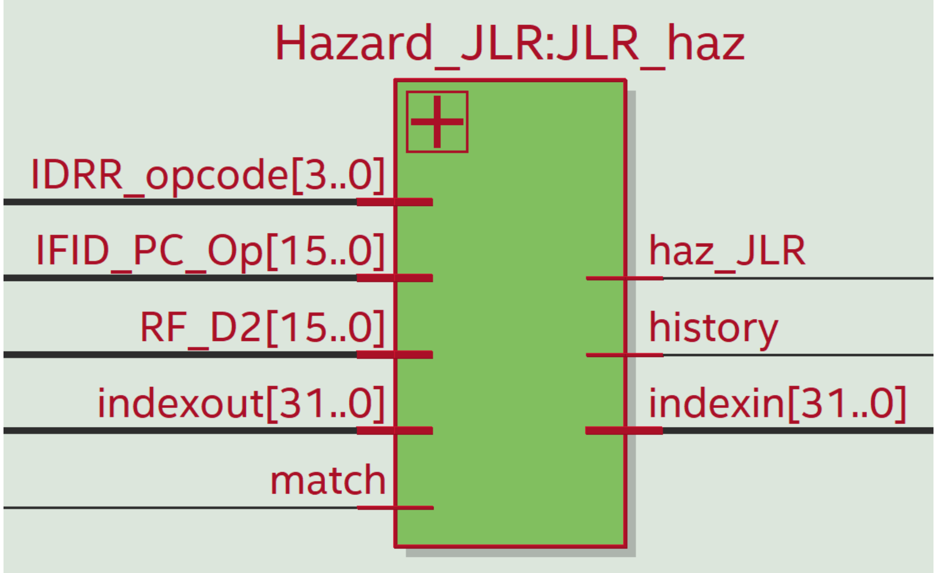
Hazard_JAL



For the JAL instruction, we need to jump to the address PC+Imm.
Therefore we can have 2 possible cases:

- We predicted the jump as taken (match='1'), and the jump was taken (EXMEM_opcode="1001"): The history bit will be set to '1' and the haz_BEQ to '0' since there was no hazard detected.
- We predicted the branch as not taken (match='0'), and the branch was taken (EXMEM_opcode="1001"): The history bit will be set to '1' and the haz_BEQ to '1' since there was a hazard detected.

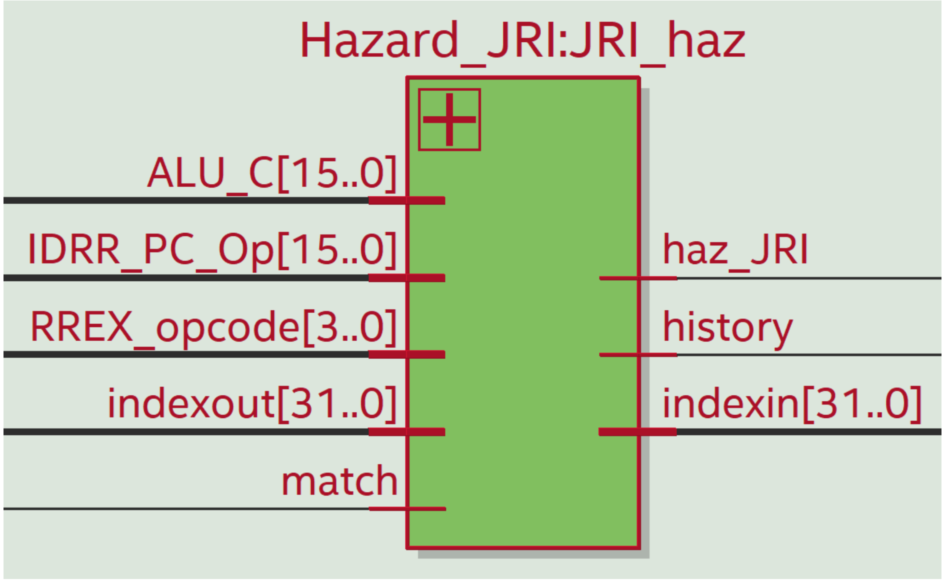
Hazard_JLR



For the JLR instruction, we need to jump to the address in regB.
Therefore we can have 2 possible cases:

- We predicted the jump as taken (match='1'), and the jump was taken (RF_D2=IFID_PC_Op): The history bit will be set to '1' and the haz_BEQ to '0' since there was no hazard detected.
- In every other case, the history bit will be set to '1' and the haz_BEQ to '1' since there was a hazard detected.

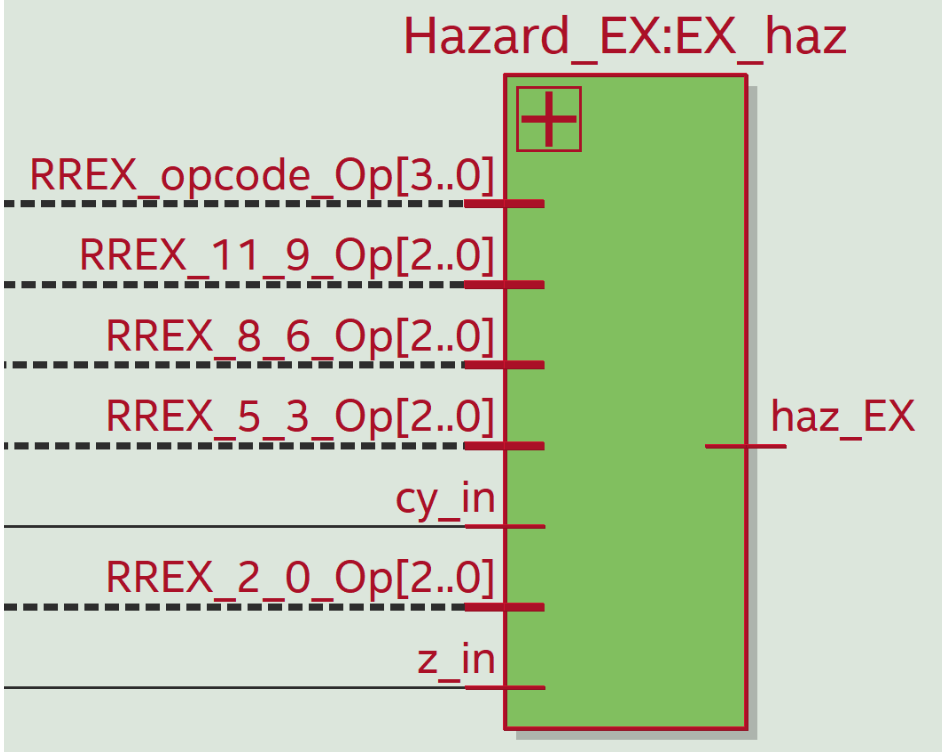
Hazard_JRI



For the JRI instruction, we need to jump to the address Ra+Imm.
Therefore we can have 2 possible cases:

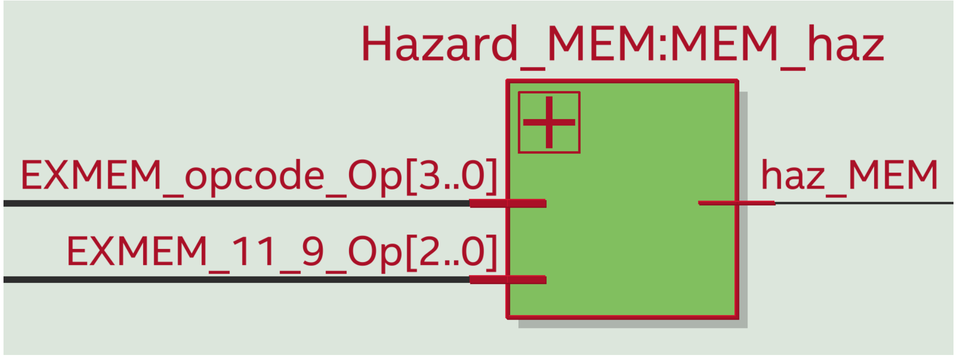
- We predicted the jump as taken (match='1'), and the jump was taken (ALU_C=IDRR_PC_Op): The history bit will be set to '1' and the haz_BEQ to '0' since there was no hazard detected.
- In every other case, the history bit will be set to '1' and the haz_BEQ to '1' since there was a hazard detected.

Hazard_EX



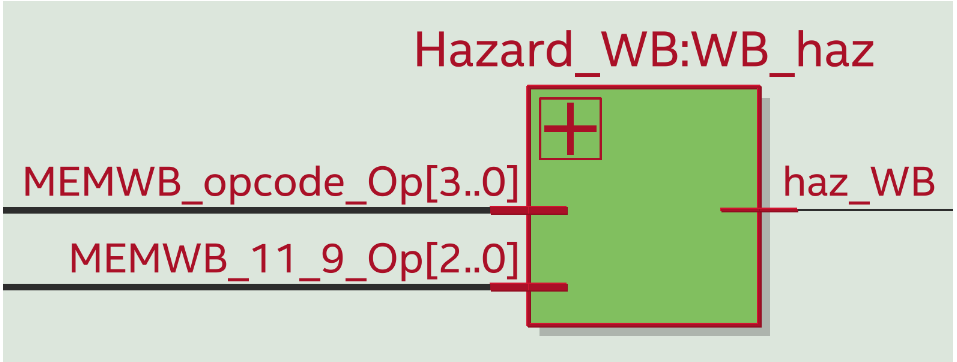
If we encounter an instruction of the form `ADD/ADC/ADZ/ADL/NDU/NDC/NDZ R7,Ra,Rb` with the necessary conditions or `ADI Rx,R7,Imm6`, we observe an R7 hazard and thus haz_EX will be set to ‘1’ and ‘0’ otherwise.

Hazard_MEM



If we encounter an instruction of the form `LW R7,Rx,Imm6`, we observe an R7 hazard and thus haz_EX will be set to ‘1’ and ‘0’ otherwise.

Hazard_WB



If we encounter an instruction of the form `LHI R7,Imm9`, we observe an R7 hazard and thus haz_EX will be set to ‘1’ and ‘0’ otherwise.