Practice Questions

- What is the use of program counter?
- What is the use of control memory?
- Distinguish between computer architecture and computer organization.
- Distinguish between direct and indirect address instructions.
- Differentiate between hardwired control and microprogrammed control organizations.
- What is program interrupt?
- What is the importance of Accumulator Logic?

Practice Questions

- Differentiate between Hardwired and Microprogrammed Control Unit.
- Explain the circuit of Accumulator logic?
- Define Interrupt. Draw Flowchart for Interrupt Cycle and explain how to handle interrupt.
- Draw the block diagram of Control Unit and explain each component. Also discuss the control timing signals.

Numerical Questions

Q 1 The following control inputs are active in the bus system. For each case, specify the register transfer that-will be executed during the next clock transition.

	S_2	S_1	S_0	LD of register	Memory	Adder
a.	1	1	1	*IR*	Read	—
b.	1	1	0	*PC*	—	—
c.	1	0	0	*DR*	Write	—
d.	0	0	0	*AC*	—	Add

Numerical Questions

Q 2 The following register transfers are to be executed in the system. For each transfer, specify:

(I) the binary value that must be applied to bus select inputs S2, S1 and S0

(2) the register whose LD control input must be active (if any)

(3) a memory read or write operation (if needed); and

(4) the operation in the adder and logic clreuit (if any).

a. A.R <-- PC

b. IR <-- M[AR]

c. M[AR] <--TR

d. AC<--DR, DR<--AC (done simultaneously)

Numerical Questions

Q3 Explain why each of the following microoperations cannot be executed during a single clock pulse in the system. Specify a sequence of microoperations that will perform the operation.

a. IR <-- M [PC]

b. AC <-- AC + TR

c. DR <-- DR + AC (AC does not change)

Numerical Solutions

Q1:

(a) Memory read to bus and load to IR: IR ← M[AR]

(b) TR to bus and load to PC: PC ← TR

(c) AC to bus, write to memory, and load to DR:

DR ← AC, M[AR]← AC

(d) Add DR (or INPR) to AC: AC ← AC + DR

Q2:

		(1) $S_2S_1S_0$	(2) Load(LD)	(3) Memory	(4) Adder
(a)	AR ← PC	010 (PC)	AR	—	—
(b)	IR ← M[AR]	111 (M)	IR	Read	—
(c)	M[AR] ← TR	110 (TR)	—	Write	—
(d)	DR ← AC AC ← DR	100 (AC)	DR and AC	—	Transfer DR to AC

Numerical Solutions

Q3:

(a) IR ← M[PC]

PC cannot provide address to memory. Address must be transferred to AR first

AR← PC

IR ← M[AR]

(b) AC ← AC + TR

Add operation must be done with DR. Transfer TR to DR first.

DR ← TR

AC ← AC + DR

(c) DR ← DR + AC

Result of addition is transferred to AC (not DR). To save value of AC its content must be stored temporary in DR (or TR).

AC ← DR, DR ← AC

AC ← AC + DR

AC ← DR, DR ← AC