Virtual memory

Virtual memory addressing is one of the possible model to access the data and programs of main memory or manage the main m/m

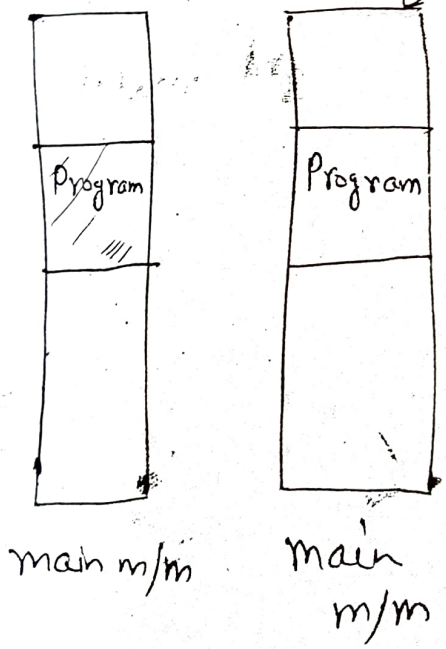
- To understand virtual m/m addressing model, we first understand the other memory-management alternative or other alternatives to store program or data in m/m

I^st model/method :- (Physical addressing)

- The programmer should know the amount of m/m present in computer
- The pgms are made by keeping in mind the physical addresses of m/m

Program's View of world :-

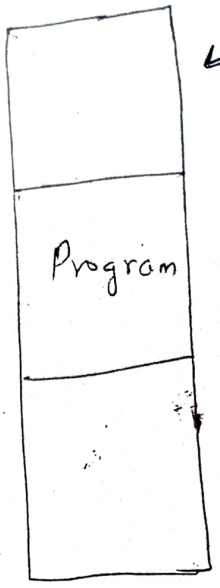
Reality



- **Dis :-**
  1. Difficult to relocate
  2. " " Swap in-swap out

(2) 2nd model (byte + offset addressing) or load time binding

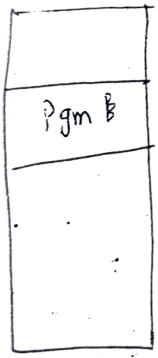
Programmer view



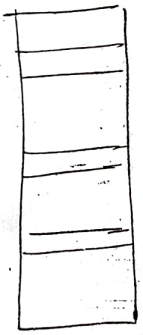
physical m/m

- H/w register used.
- Programmer think pgm starts at 0, but using H/w register, pgm relocate at other address in m/m.
- Pgm cannot be fragmented

3rd model (Virtual addressing model)



Programmer View (Virtual m/m)



Reality (Physical m/m)

- Programmer think pgm as in contiguous allocation
- But pgm is fragmented into pages.
- Not all pages are kept in m/m.

Ques:- Consider 4 cache block initially empty with following MM block reference request:

4, 5, 7, 12, 4, 5, 13, 4, 5, 7

Identify the hit ratio by using

(i) FIFO (ii) LRU (iii) DM

(iv) 2-way SAM with LRU

(v) Associative with LRU

(v) ~~4, 5, 7~~, same as LRU

4, 5, 7, 12, 4, 5, 13, 4, 5, 7
H H

(i)

4	13
5	4
7	5
12	7

Hit Ratio = $\frac{2}{10}$ = 0.2

Miss Ratio = 1 − Hit Ratio = 1 − 0.2 = 0.8

(ii) 4, 5, 7, 12, 4, 5, 13, 4, 5, 7
H H H H

4	
5	
7	13
12	7

Hit Ratio = $\frac{4}{10}$ = 0.4

Miss Ratio = 1 − 0.4 = 0.6

(iii) 4, 5, 7, 12, 4, 5, 13, 4, 5, 7
H H H

K%N = i

K%4

0	4, 12, 4
1	5, 13, 5
2	
3	7

Hit Ratio = $\frac{3}{10}$ = 0.3

Miss Ratio = 1 − 0.3 = 0.7

(iv) No. of set = $\frac{N}{P} = \frac{4}{2} = 2$

K%2 = i

4, 5, 7, 12, 4, 5, 13, 4, 5, 7
H H H H

0	4, 12
1	5, 7 13, 7

Hit Ratio = $\frac{4}{10}$ = 0.4

Miss Ratio = 1 − 0.4 = 0.6

FIFO

Ques:- Consider a 4 way set associative cache with total 16 cache blocks.
Main Memory block requests are:

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155, 2

(H)

k mod n
↓ Block No. — ↓ No. of set

Sol:- No. of set = $\frac{16}{4} = 4$

0 mod 4 = 0
255 mod 4 = 3

S_0	~~0~~, ~~4~~, ~~8~~, 216,	48, 32, 92
S_1	1, 133, 129, 73	
S_2	2	
S_3	~~255~~, 3, 159, 63	155

LRU

S_0	~~0~~, ~~4~~, ~~8~~, ~~216~~, 8,	48, 32, 92
S_1	1, 133, 129, 73	
S_2	2	
S_3	~~255~~, 3, 159, 63,	155

LRU

Ques:- Consider a fully associative cache with 8 cache blocks (0-7) and the following sequence of memory block requests:

M H H H H
4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16,
H
25, 7

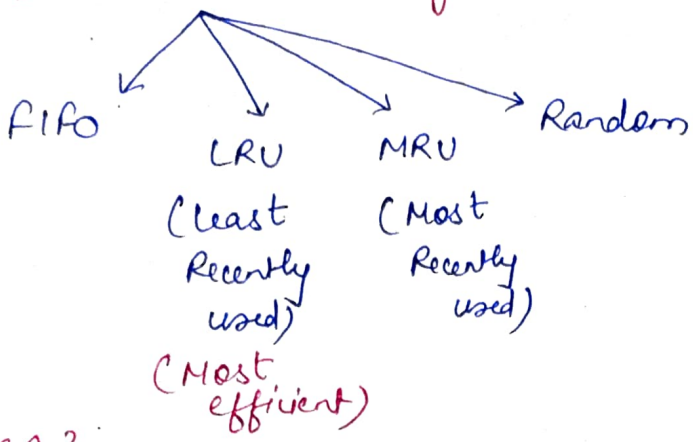
If LRU replacement policy is used, which cache block will have memory block 7? (Gate 2004)

0	~~4~~ 45
1	~~3~~ 22
2	25
3	8
4	~~19~~ 3
5	~~6~~ 7
6	16
7	35

Cache

Cache Block at = 5

Cache Replacement Algorithm



Why use CRA?

→ Miss Penalty Reduce

→ Hit increase

SO that we get optimized result.

* Cache Replacement Algo is not used in Direct Mapped Technique.
  used in only Set Associative & Fully Associative Technique