Microprocessors

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UNIT-2

Timing Diagram

Timing and Control Operation

- Timing and control operations are responsible for synchronizing the process of communication between µP and peripheral devices.
- Whenever µP has to execute any instruction, the instruction is first received by the instruction register (8-bit) through A/D (address/data) bus.
- The instruction is then passed on to the instruction decoder where it is split, decoded and then passed to the control unit to generate necessary control signals for its execution.
- Besides doing this timing and control unit also checks whether any internal or external interrupt has occurred.

Timing and Control Operation

- To execute any instruction µP has to pursue the following steps:
  1. Identify the memory location from where the instruction is to be fetched
  2. Decode the instruction using instruction decoder
  3. Perform the function specified by the decoded instruction

- All these operations are performed within a given time interval, which is provided by the clock of the system.
- With reference to the above mentioned operations certain terms can be defined.

Timing and Control Operation

The definitions are as follows

- **Instruction cycle**: Time required for completing the execution of an instruction is known as instruction cycle.
  - The 8085 instruction cycle consists of one to six machines cycles or operations.
- **Machine cycle**: It is the time required for completing a single operation.
  - This operation can be accessing memory for read/write operation or accessing I/O device.
  - There can be 3 to 6 clock periods or T-states in a machine cycle.

Timing and Control Operation

The definitions are as follows

- **T-states or clock cycles/periods (CLK)**: T-state is equivalent to one clock period.
  - It is the time in which only a subdivision of the operation can be performed.
  - The total number of T-states determines the size of the machine cycle required to perform an operation.

8085 Machine Cycle Status and Control Signals

Machine Cycle	Status			Control Signals
	IO/$\overline{M}$	S_1	S_0	
Opcode Fetch	0	1	1	$\overline{RD} = 0$
Memory Read	0	1	0	$\overline{RD} = 0$
Memory Write	0	0	1	$\overline{WR} = 0$
I/O Read	1	1	0	$\overline{RD} = 0$
I/O Write	1	0	1	$\overline{WR} = 0$
Interrupt Acknowledge	1	1	1	$\overline{INTA} = 0$
Halt	Z	0	0	$\overline{RD}$, $\overline{WR}$ = Z and $\overline{INTA} = 1$
Hold	Z	X	X	
Reset	Z	X	X	

NOTE: Z = Tri-state (high impedance)
X = Unspecified

MACHINE CYCLES OF 8085

- The 8085 is designed to execute 74 different instruction types.
- Each instruction in 8085 microprocessor consists of two part- operation code (opcode) and operand.
- The opcode is a command such as ADD and the operand is an object to be operated on, such as a byte or the content of a register.
- Some instructions are 1-byte instructions and some are multi-byte instructions.
- The processor takes a definite time to execute the machine cycles.
- The T-state starts at the falling edge of a clock.

MACHINE CYCLES OF 8085

- The 8085 microprocessor has 5 basic machine cycles.
  1. Opcode fetch cycle (4T)
  2. Memory read cycle (3 T)
  3. Memory write cycle (3 T)
  4. I/O read cycle (3 T)
  5. I/O write cycle (3 T)

Timing Diagram

- A timing diagram of an instruction is a **graphical representation of the time taken by the µP to fetch, decode and execute an instruction**.
- The size of the instruction and the frequency of the µP decides the total amount of time taken to execute an instruction.

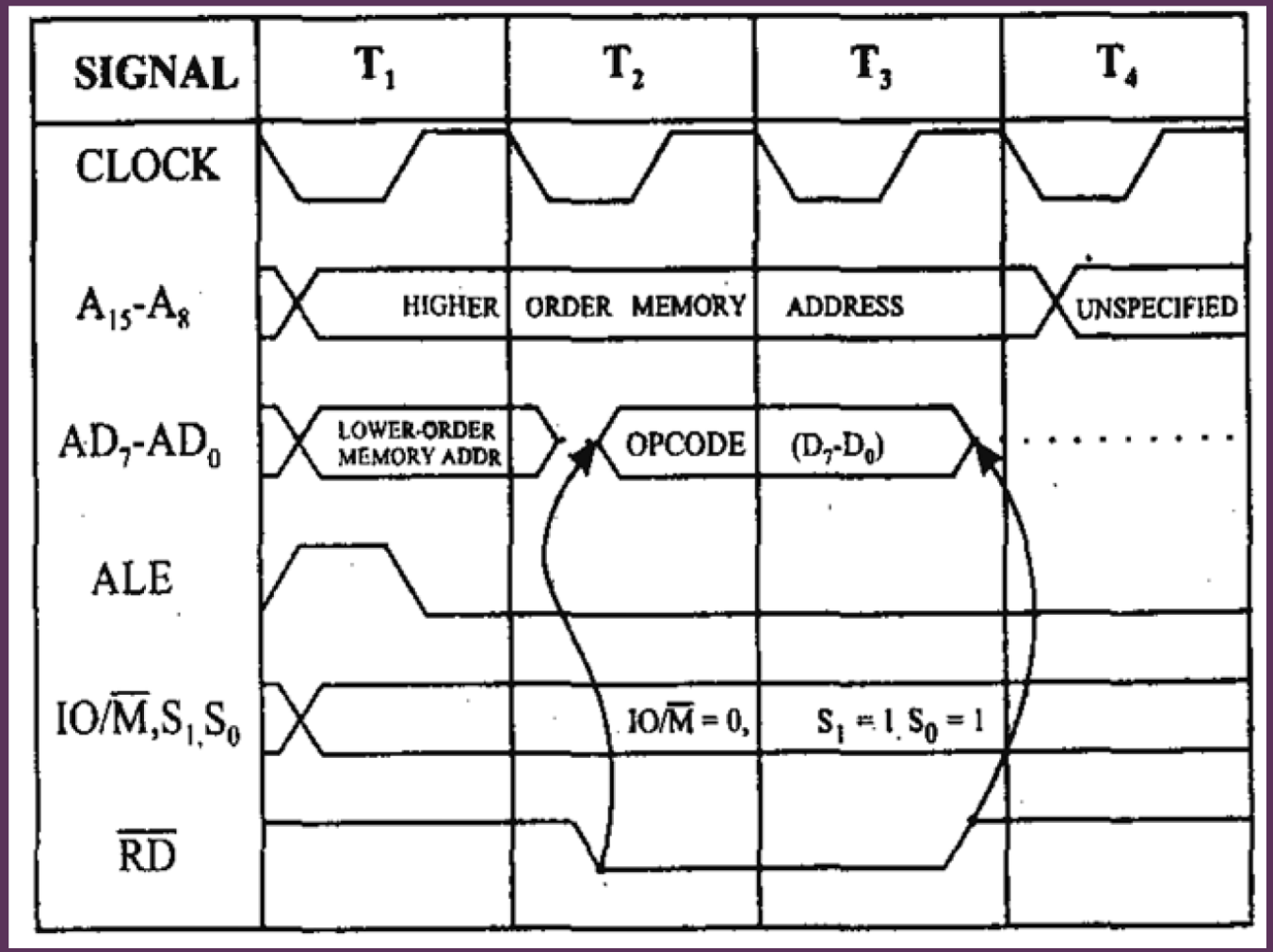
MACHINE CYCLES OF 8085

Timing of the OPCODE FETCH MACHINE CYCLE OF 8085

- Each instruction of the processor has one byte opcode.
- The opcodes are stored in memory.
- Every instruction starts with opcode fetch machine cycle.
- The time taken by the processor to execute the opcode fetch cycle is 4T.
- In this time, the first, 3 T states (T1-T3) are used for fetching the opcode from memory and the last T4 to decode and execute the opcode.

MACHINE CYCLES OF 8085

Timing of the OPCODE FETCH MACHINE CYCLE OF 8085



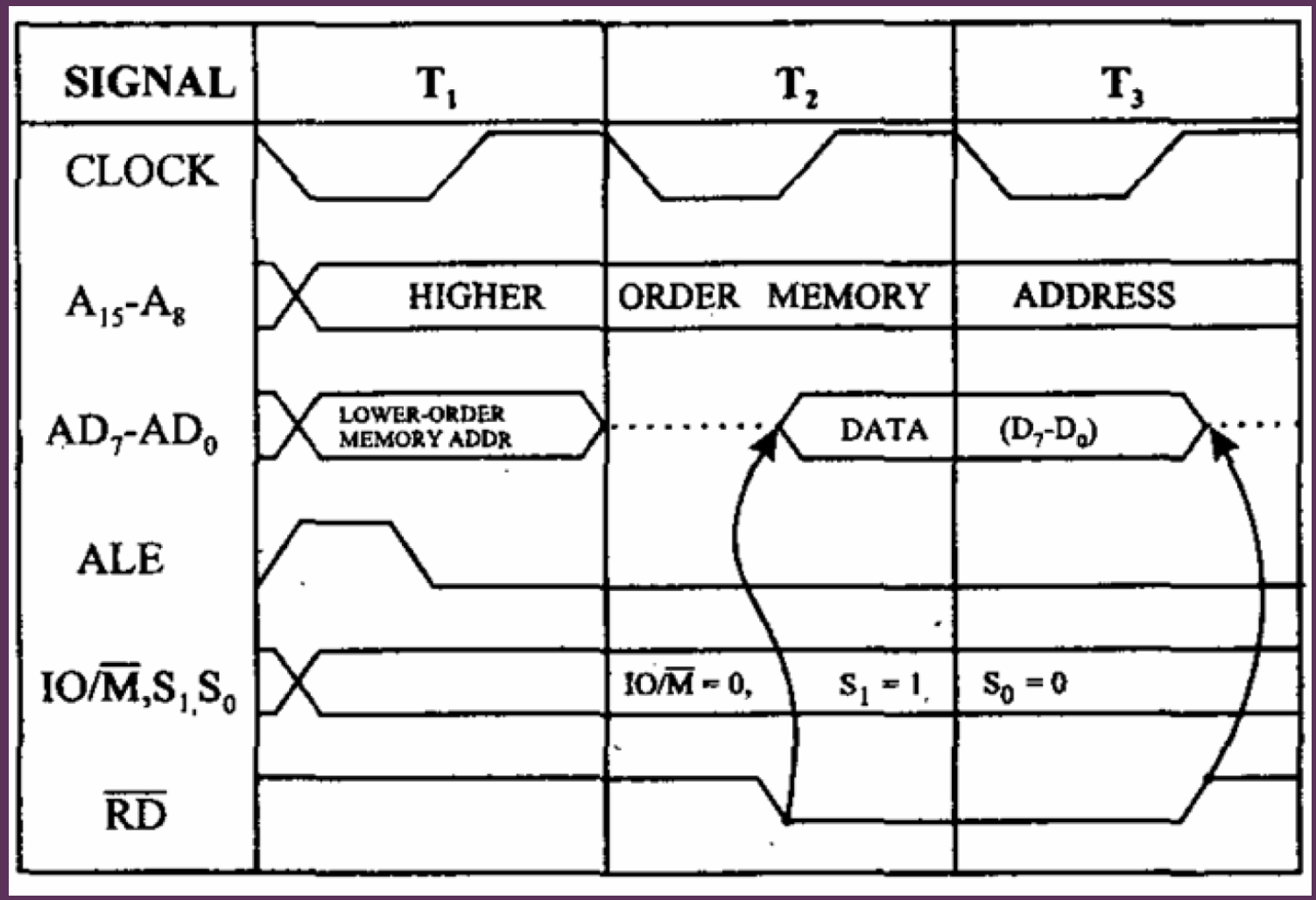
MACHINE CYCLES OF 8085

Timing of the MEMORY READ MACHINE CYCLE OF 8085

- The memory read machine cycle is executed by the processor to read a data byte from memory.
- The processor takes 3T states to execute this cycle.
- The instructions which have more than one byte word size will use the machine cycle after the opcode fetch machine cycle.

MACHINE CYCLES OF 8085

Timing of the MEMORY READ MACHINE CYCLE OF 8085



MACHINE CYCLES OF 8085

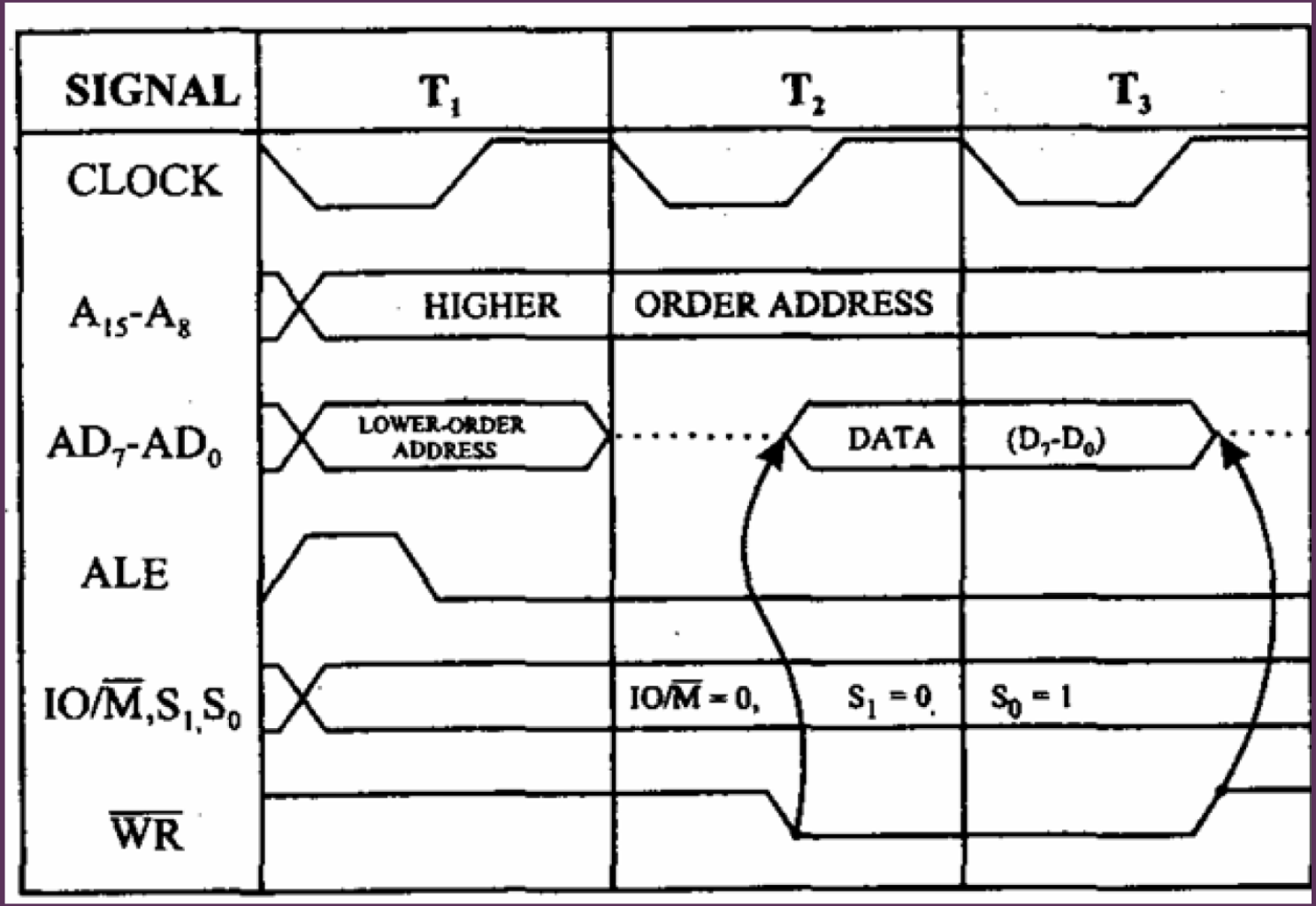
Timing of the MEMORY WRITE MACHINE CYCLE OF 8085

- The memory write machine cycle is executed by the processor to write a data byte in a memory location.

- The processor takes, 3T states to execute this machine cycle.

MACHINE CYCLES OF 8085

Timing of the MEMORY WRITE MACHINE CYCLE OF 8085



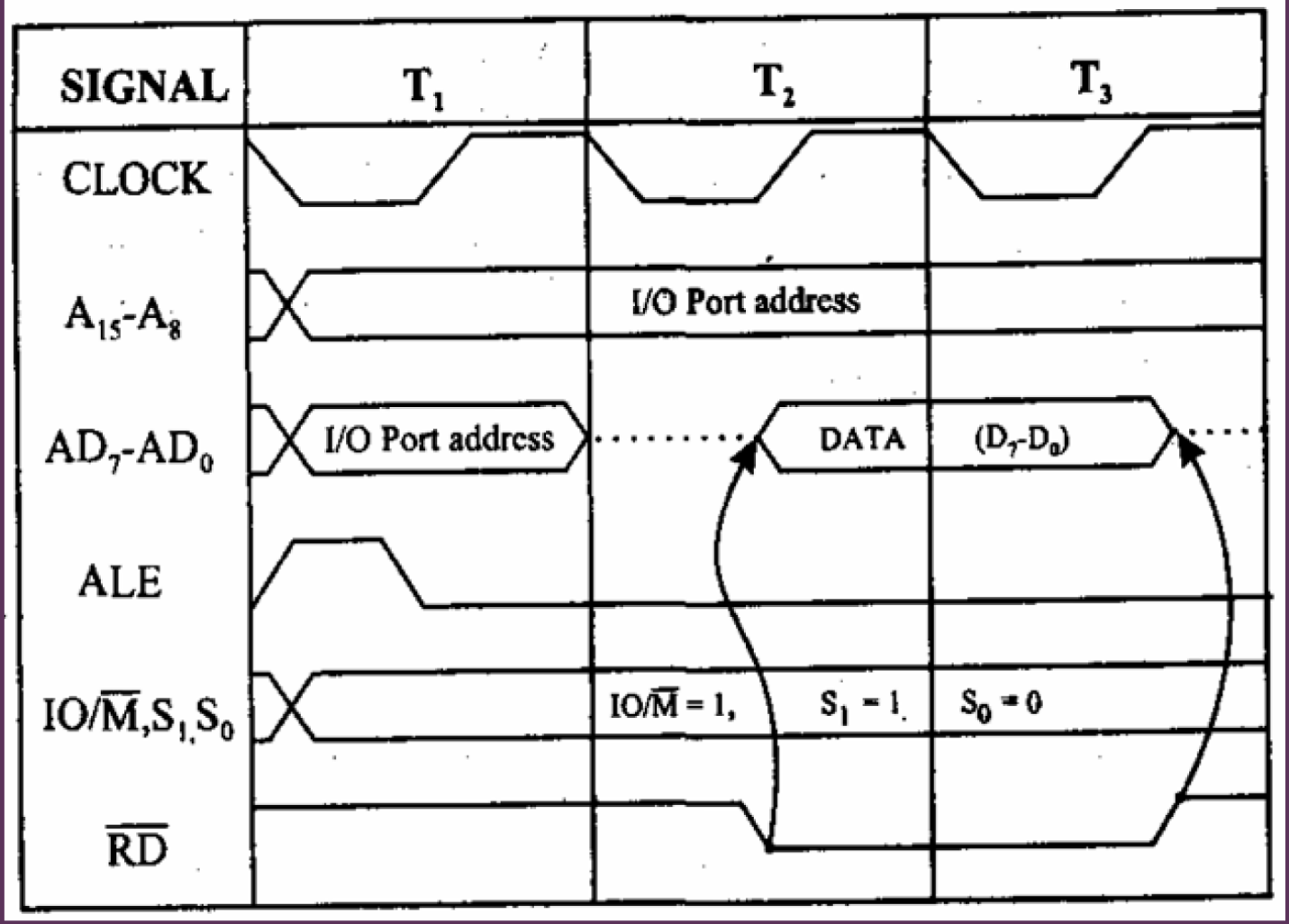
MACHINE CYCLES OF 8085

Timing of the I/O Read MACHINE CYCLE OF 8085

- The I/O Read cycle is executed by the processor to read a data byte from I/O port or from the peripheral.
- The processor takes 3T states to execute this machine cycle.
- The **IN** instruction uses this machine cycle during the execution.

MACHINE CYCLES OF 8085

Timing of the I/O Read MACHINE CYCLE OF 8085



MACHINE CYCLES OF 8085

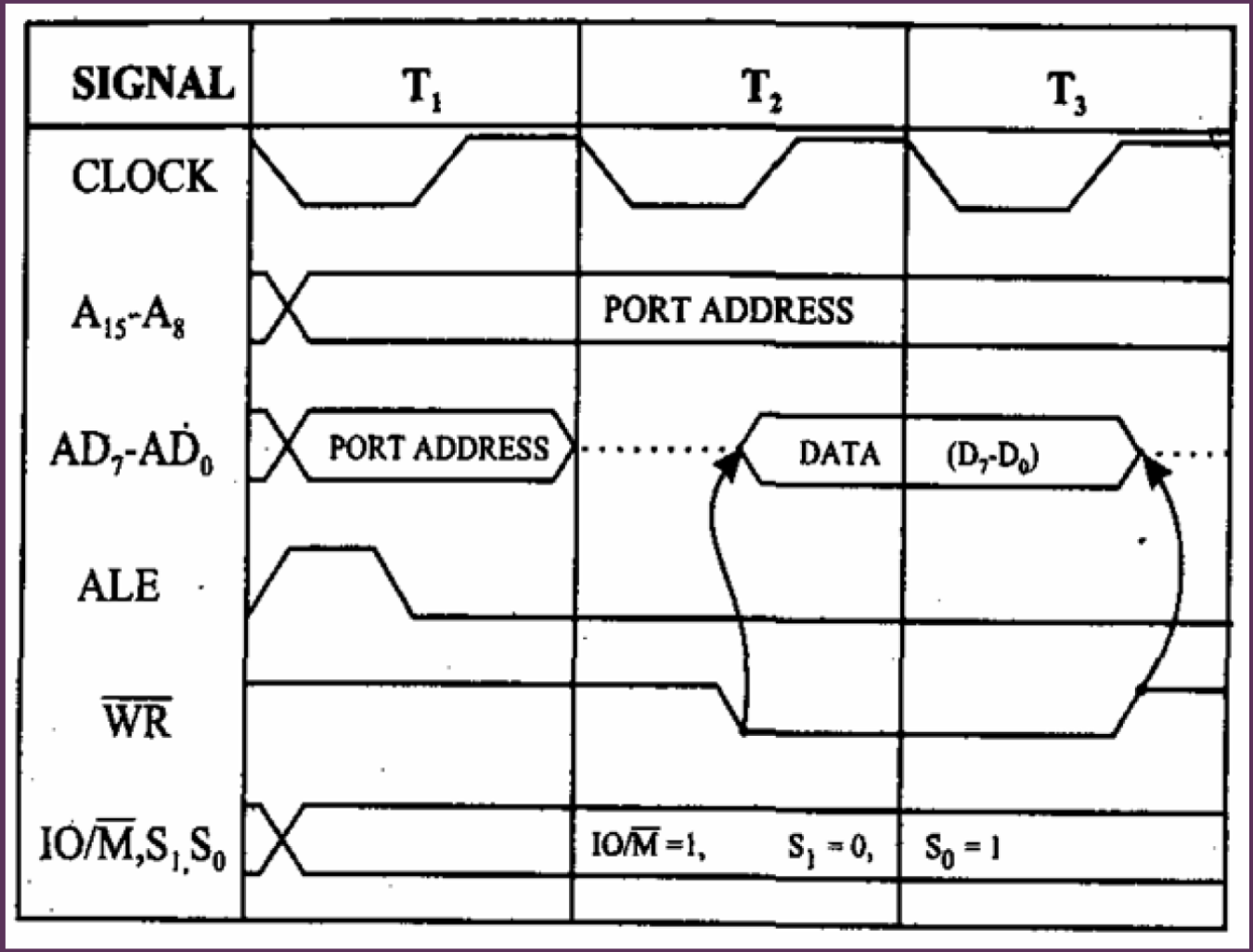
Timing of the I/O Write MACHINE CYCLE OF 8085

- The I/O write machine cycle is executed by the processor to write a data byte in the I/O port or to a peripheral, which is I/O, mapped in the system.

- The processor takes, 3T states to execute this machine cycle.

MACHINE CYCLES OF 8085

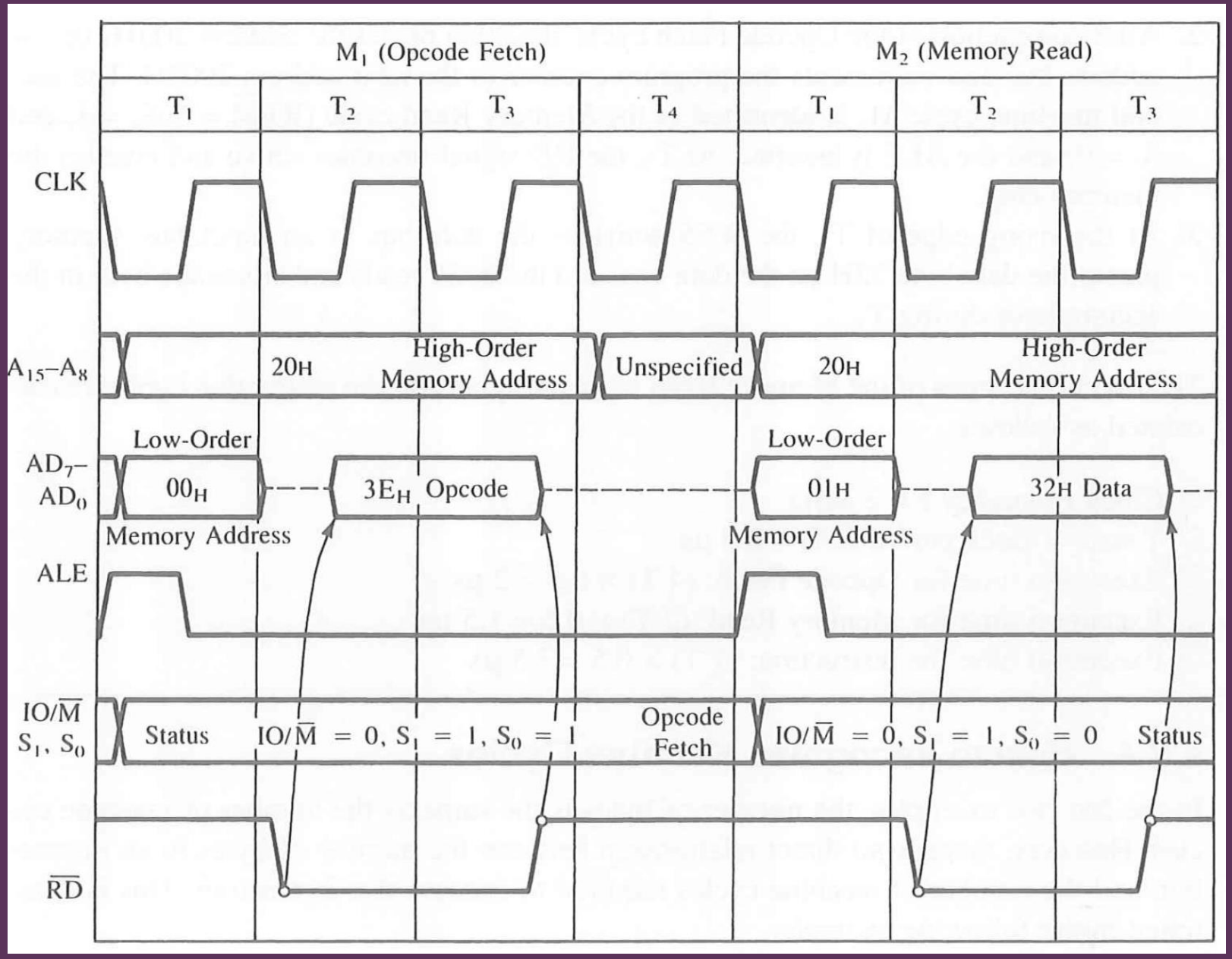
Timing of the I/O Write MACHINE CYCLE OF 8085



MACHINE CYCLES OF 8085

8085 Timing for the Execution of the Instruction:

MVI A, 32 H



MACHINE CYCLES OF 8085

- Calculation of execution time of Opcode fetch cycle, machine cycle and instruction cycle:
  - Let the clock frequency f=5MHz
  - One T-state= clock period (1/f)=0.2µs
  - Execution time for Opcode fetch = 4 ×T = 4 × 0.2µs = 0.8 µs
  - Execution time for Memory read = 3 ×T = 3 × 0.2µs = 0.6 µs
  - Execution time for instruction = 7 ×T = 7 × 0.2µs = 1.4 µs

MACHINE CYCLES OF 8085

Explain the machine cycles of the following 3-byte instruction when it is executed.

Opcode	Operand	Bytes	Machine Cycles	T-States	Operation
STA	2065H	3	4	13	This instruction stores (writes) the contents of the accumulator in memory location 2065H

MACHINE CYCLES OF 8085

The machine codes are stored in memory locations 2010H, 2011H, and 2012H as follows: the 16-bit address of the operand must be entered in reverse order, the low-order byte first, followed by the high-order byte.

Memory Address	Machine Code		
2010	0011	0010 → 32H	Opcode
2011	0110	0101 → 65H	Low-order address
2012	0010	0000 → 20H	High-order address

MACHINE CYCLES OF 8085

1. In the first machine cycle, the 8085 places the address 2010H on the address bus and fetches the opcode 32H.
2. The second machine cycle is Memory Read. The processor places the address 2011H and gets the low-order byte 65H.
3. The third machine cycle is also Memory Read; the 8085 gets the high-order byte 20H from memory location 2012H.
4. The last machine cycle is Memory Write. The 8085 places the address 2065H on the address bus, identifies the operation as Memory Write ($IO/\overline{M} = 0$, $S_1 = 0$, and $S_0 = 1$). It places the contents of the accumulator on the data bus AD_7–AD_0 and asserts the $\overline{WR}$ signal. During the last T-state, the contents of the data bus are placed in memory location 2065H.