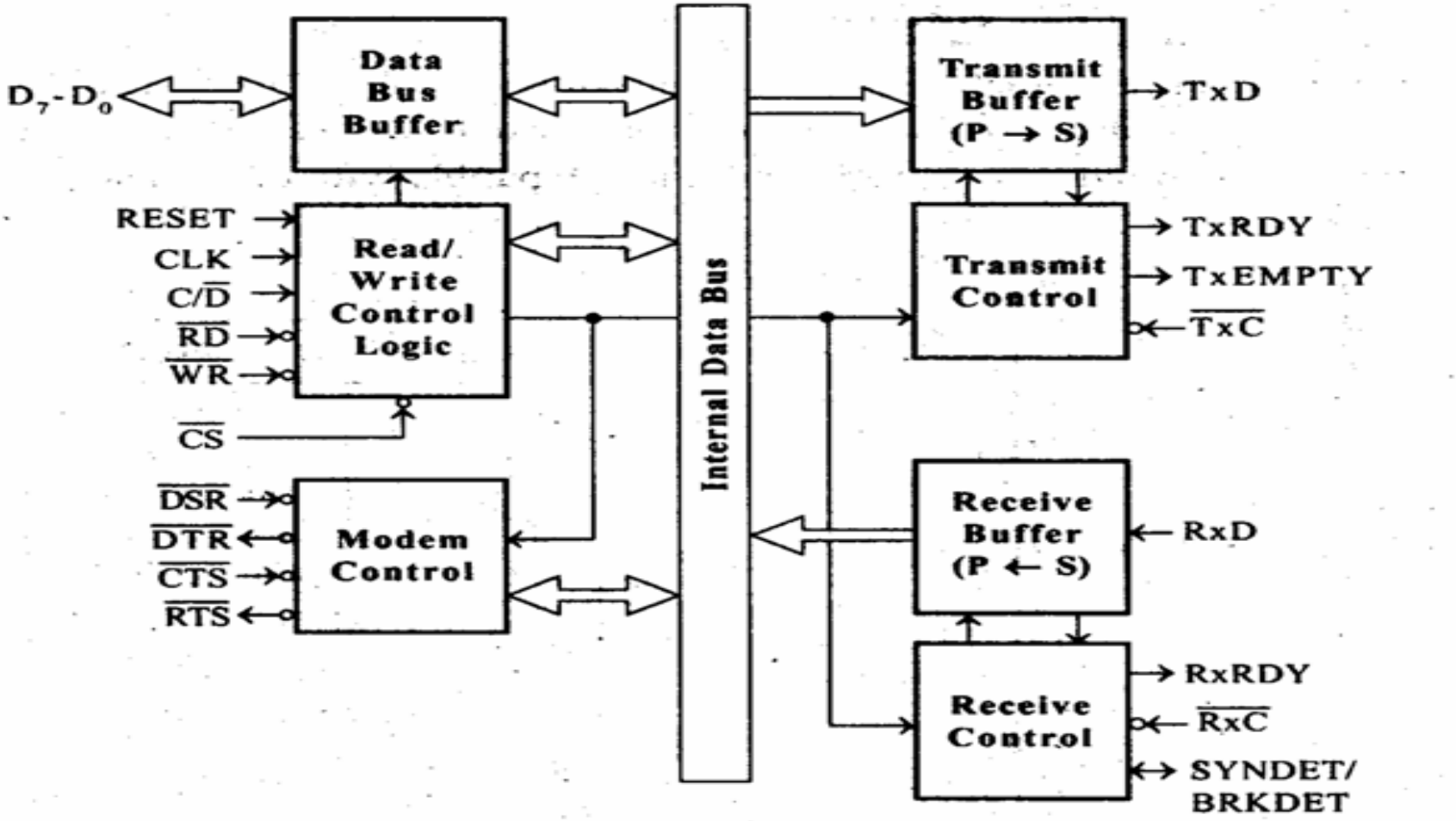
USART :8251

- 8251 is universal synchronous asynchronous receiver transmitter (USART).
- It takes data serially from peripheral (outside devices) and converts into parallel data. After converting the data into parallel form, it transmits it to the CPU.
- Similarly, it receives parallel data from microprocessor and converts it into serial form. After converting data into serial form, it transmits it to outside device (peripheral).

Block Diagram of 8251



Read/Write control logic of 8251

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Operation
1	X	X	X	Invalid
0	0	0	1	data CPU< ----- 8251
0	0	1	0	data CPU ----- > 8251
0	1	0	1	Status word CPU < ----------8251
0	1	1	0	Control word CPU---------- > 8251

MODEM Control Signals of 8251

- **DSR:** Data Set Ready signal is an input signal.
- **DTR:** Data terminal Ready is an output signal.
- **CTS:** It is an input signal which controls the data transmit circuit.
  RTS: It is an output signal which is used to set the status RTS.

HEMANT SINGH POKHARIYA, Assistant Proffesor CSE DEPT
GRAPHIC ERA DEMEED TO BE UNIVERSITY DEHADUN

Transmit buffer and control signals

- **TXD:** It is an output signal, if its value is one, means transmitter will transmit the data.
- **TXRDY:** It means transmitter is ready to transmit data character.
- **TXEMPTY:** An output signal which indicates that TXEMPTY pin has transmitted all the data characters and transmitter is empty now.
- **TXC:** An active-low input pin which controls the data transmission rate of transmitted data.

Receive buffer and control signals

- **RXD:** An input signal which receives the data.
- **RXRDY:** An input signal indicates that it is ready to receive the data.
- **RXC:** An active-low input signal which controls the data transmission rate of received data.
- **SYNDET/BD:** An input or output terminal. External synchronous mode-input terminal and asynchronous mode-output terminal.

Thanks For Watching