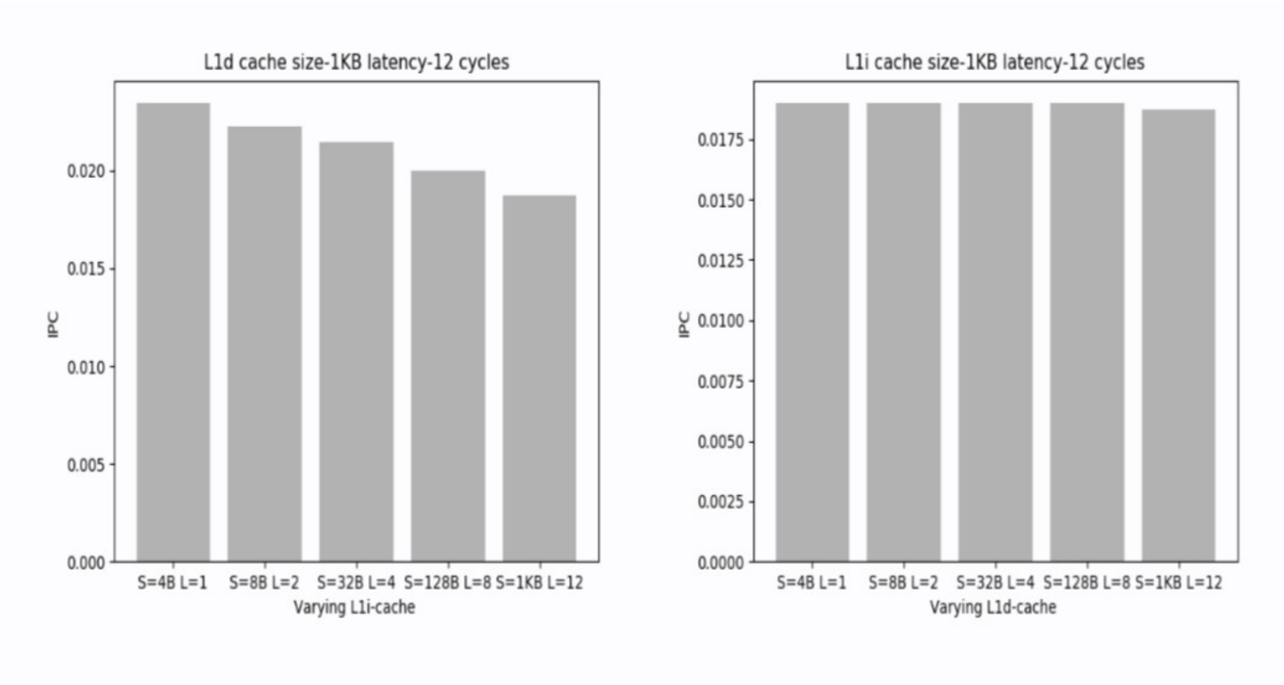
1 Graphs

Here are the graphs.

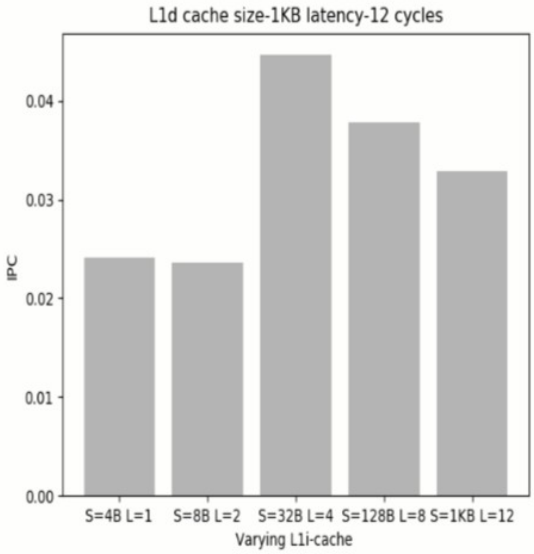
For each program we have plotted CPI vs Varying cache size.
First we have fixed the L1d Cache(1KB and 12 cycles-latency) and varied the size of L1i cache. Then we have fixed the L1i Cache(1KB and 12 cycles-latency) and varied the size of L1d cache.

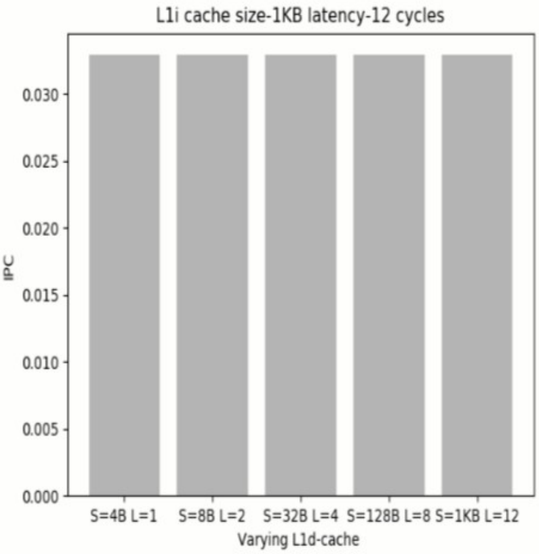


1.1 even or Odd

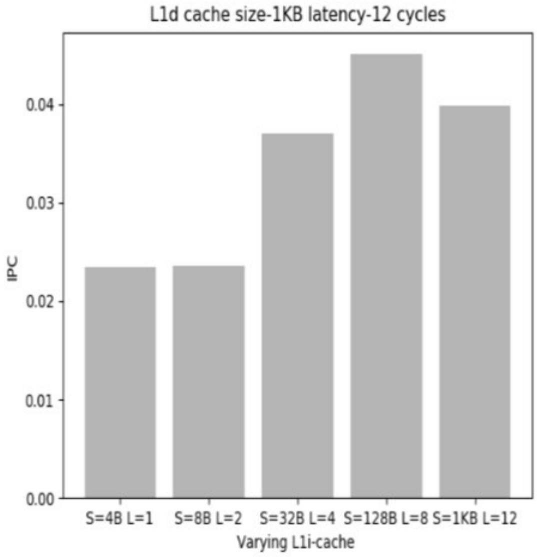
These are the graphs for evenorodd program.

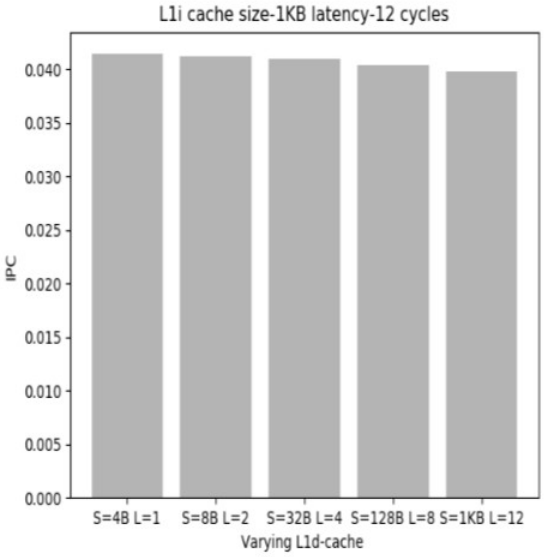
1.2 Prime



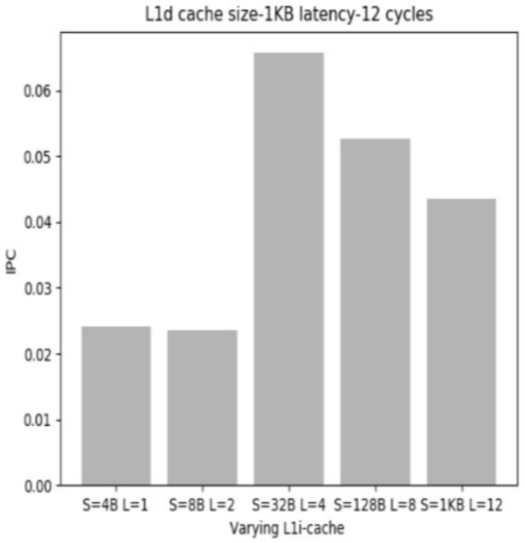


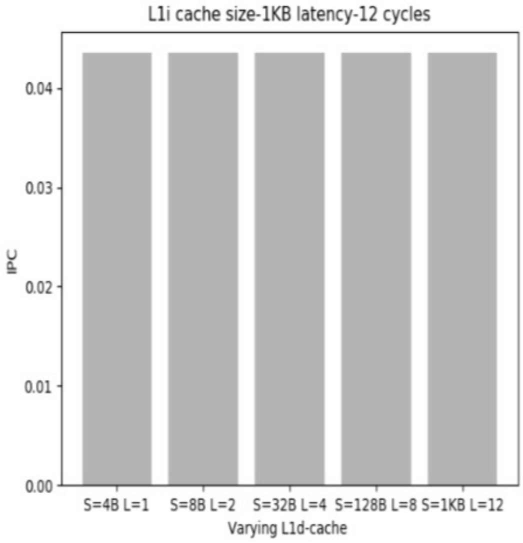
1.3 fibonnacci



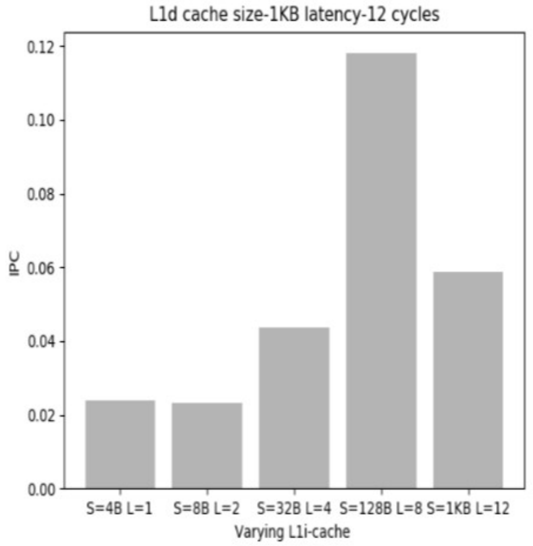


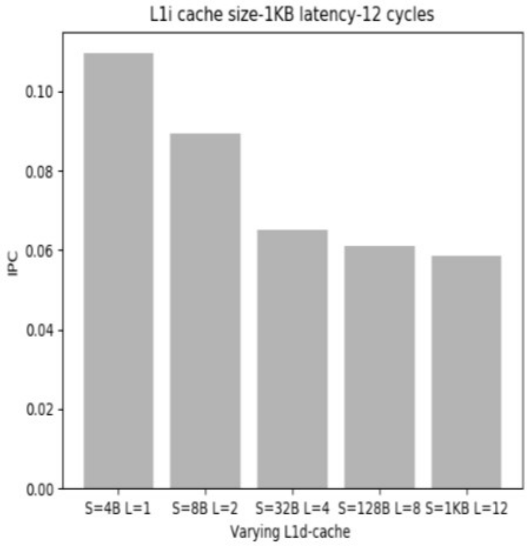
1.4 palindrome





1.5 descending





Observation

On increasing the cache size you can keep more no. of instructions/ data in the cache, which increases the hit rate and thus increasing intruction per cycle (IPC).

On increasing the cache size, the latency of the cache(no.of cycles to fetch from memory) increases and hence the IPC wil decrease

So on increasing cache size both hit rate and latency increases, both of which have opposite effects on IPC,therefore we getan optimal size of cache where the IPC is maximum.

We observe normal distribution graph when we vary L1i cache keeping L1d cache fixed as all the instructions are fetchedfrom the memory. In the other graph when we fixed the l1i cache and change the size of L1d we, dont see much differencein the IPC values for different sizes. This is because the no. of load and store operations are very less in our program andhence the L1d cache dosen’t play much of a role.No.of in load and store instructions are significantly higher in descending program, which can be seen in the graph also.we can see that on increasing cache size the IPC keeps on decreasing because we are using data from different address eachtime, so hit rate in nearly zero and for fetching each data value we require more time as the latency is increasing.