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2D Semiconductor FETs—Projections and Design for Sub-10 nm VLSI

Wei Cao, *Student Member, IEEE*, Jiahao Kang, *Student Member, IEEE*, Deblina Sarkar, *Student Member, IEEE*, Wei Liu, *Member, IEEE*, and Kaustav Banerjee, *Fellow, IEEE*

Abstract—Two-dimensional (2D) crystal semiconductors, such as the well-known molybdenum disulfide (MoS_2), are witnessing an explosion in research activities due to their apparent potential for various electronic and optoelectronic applications. In this paper, dissipative quantum transport simulations using nonequilibrium Green's function formalism are performed to rigorously evaluate the scalability and performance of monolayer/multilayer 2D semiconductor-based FETs for sub-10 nm gate length very large-scale integration (VLSI) technologies. Device design considerations in terms of the choice of prospective 2D material/structure/technology to fulfill sub-10 nm International Technology Roadmap for Semiconductors (ITRS) requirements are analyzed. First, it is found that MoS_2 FETs can meet high-performance (HP) requirement up to 6.6 nm gate length using bilayer MoS_2 as the channel material, while low-standby-power (LSTP) requirements present significant challenges for all sub-10 nm gate lengths. Second, by studying the effects of underlap (UL) structures, scattering strength, and carrier effective mass, it is found that the high mobility and suitably low effective mass of tungsten diselenide (WSe_2), aided by the UL, enable 2D FETs for both HP and LSTP applications at the smallest foreseeable (5.9 nm) gate length. Finally, possible solutions for sub-5 nm gate lengths, specifically anisotropic 2D semiconductor materials for HP and sub- kT/q switch (2D tunnel FET) for LSTP, are also proposed based on the effects of critical material parameters on the device performance.

Index Terms—2D FET, 2D materials, 2D semiconductors, 2D tunnel-FET (TFET), anisotropic materials, black phosphorus, high-performance (HP), low-dimensional materials, low-power, molybdenum disulfide (MoS_2), scaling, transition metal dichalcogenide (TMD), tungsten diselenide (WSe_2), very large-scale integration (VLSI).

I. INTRODUCTION

THE atomic scale thicknesses of 2D semiconductors offer high scalability to FETs using them as channel materials, which is the primary motivation for researchers to explore them for the FET application in sub-10 nm nodes [1], [2]. Although conventional bulk semiconductors, such as silicon and germanium, can also be made very thin, 2D semiconductors own extra advantages, specifically, atomically smooth and dangling bond-free surface, and uniform and fixed (with the number of layers) thickness, as schematically shown

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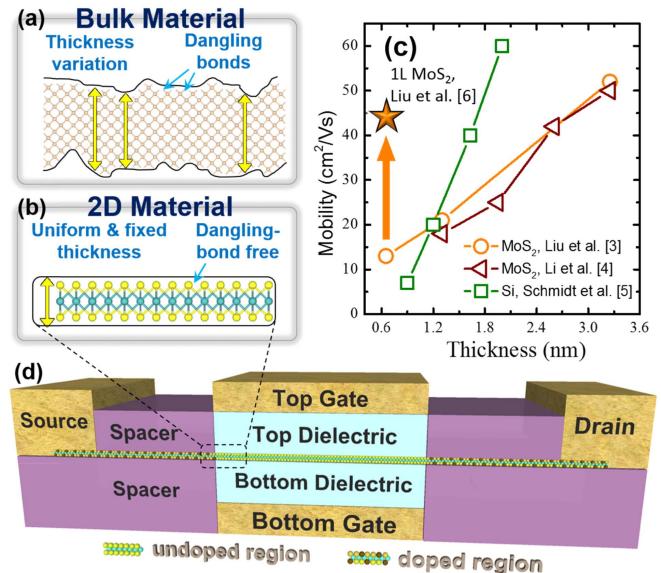


Fig. 1. (a) Issues of bulk material during thickness scaling for FET application. (b) Advantages of 2D materials over bulk materials. (c) Carrier mobility degradation with reduced material thickness for Si and MoS_2 . An improved mobility recently achieved in monolayer (1L) MoS_2 with thickness of 0.65 nm is also included. (d) Schematic of a DG 2D FET.

in Fig. 1(a) and (b). These advantages intrinsically suppress possible trap generation, carrier scattering, and thickness (and hence bandgap) variation, guaranteeing robust device performance. By comparing the carrier mobilities in molybdenum disulfide (MoS_2) [3], [4], the most widely studied 2D semiconductor, and in the mainstream Si [5] during thickness scaling, as shown in Fig. 1(c), it is found that the mobility degradation rate with decreasing thickness in MoS_2 is much slower with respect to that in Si, leading to higher mobility at the extremely scaled (monolayer or 1L) thickness. With continuous improvement in material quality, and proper gate dielectric engineering, the mobilities in MoS_2 and other 2D materials can be further improved, as recently demonstrated in [6] with the mobility in monolayer MoS_2 boosted to $44 \text{ cm}^2/\text{V} \cdot \text{s}$ [see Fig. 1(c)]. Note that the FET channel thickness scaling is imposed by gate length scaling as reflected by a general scaling formula $L_{g,\min} \geq \beta(T_{ch}\varepsilon_{ch}/\varepsilon_{ox})^{1/2}$ [7], [8], where $L_{g,\min}$ is the minimum gate length in order to maintain good device electrostatics, β is a constant that generally should be > 2.5 . T_{ch} (T_{ox}) is the channel (gate oxide) thickness, and ε_{ch} (ε_{ox}) is the dielectric constant of channel (gate oxide). The ultrasmall T_{ch} of 2D semiconductors enable ultrasmall $L_{g,\min}$ of 2D FETs.

The successful experimental demonstration of monolayer MoS_2 -based top-gate FET in [1] attracted intensive research

efforts in this arena, which has, so far, rendered fruitful outcomes, such as the realization of a large-scale MOCVD growth of MoS₂ [9] and a stable doping technique [10], and the demonstration of high-performance (HP) 2D FETs with low contact resistance [3], [11], and high mobilities [6], [12], [13]. In parallel with these experimental achievements, several theoretical works [14]–[24] have been carried out to evaluate the scalability of monolayer/multilayer 2D FETs based on semiconductor-on-insulator (SOI) or double-gate (DG) FET topology, as schematically shown in Fig. 1(d). However, most of them are based on ballistic transport simulations [14]–[20], or non self-consistent back scattering estimations [21], [22]. It has recently been reported that MoS₂ suffers from remote phonon scattering in high- k dielectric environment and has an intrinsic phonon limited room-temperature mobility of only $\sim 60 \text{ cm}^2/\text{V} \cdot \text{s}$ [25]. Moreover, Liu *et al.* [24] reported, by considering phonon scattering only, that the performance of monolayer MoS₂ FET is far from ballistic even at sub-10 nm nodes. So far, the reported scaling analyses on a few transition metal dichalcogenide (TMD) materials, seem generally negative in terms of meeting the ITRS requirements, and no efforts have been made to provide possible solutions for overcoming the apparent challenges. Therefore, a comprehensive performance/scalability evaluation of monolayer/multilayer TMD- and other 2D semiconductor FETs based on the dissipative transport theory, along with practical solutions to meet the ITRS requirements is highly desirable. We present such an evaluation platform and propose solutions for sub-10 nm 2D FETs in this paper. It is worth noting that “xx nm node” used throughout this paper refers to the actual gate length if not specified otherwise, rather than the “ITRS node,” which is much larger.

II. SIMULATION METHODOLOGY

A. Device Structure

In section III, both the SOI and the DG configurations will be discussed based on the device structure shown in Fig. 1(d). In SOI configuration, the bottom gate electrode is connected to the ground, and the bottom gate dielectric thickness is fixed to be 50 nm, which ensures that the bottom gate capacitance is small enough and does not contribute to the total gate capacitance. In DG configuration, the top and the bottom gates are symmetric, and connected together. HfO₂ (dielectric constant $\epsilon_{\text{HfO}_2} = 23.5$) is used as both the top and the bottom gate dielectric. The dielectric materials between the gate and the source/drain contacts are called spacer in this paper for simplicity. Parameters such as effective-oxide-thickness, supply voltage V_{dd} , body thickness (only for Si device) at each node (or gate length L_g) used throughout this paper are adapted from ITRS tables [26] and also listed in Table I.

B. Channel Materials

MoS₂, as the most studied 2D semiconductor, is taken as a representative 2D channel material in this paper. Whenever MoS₂ is unable to meet the ITRS requirements, the study is extended to other 2D semiconductors by changing critical parameters that affect the device performance. Relevant

TABLE I
SCALING PARAMETERS ADAPTED FROM ITRS TABLES [26]

| Year of Production | | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 |
|--------------------|--------------|------|------|------|------|------|------|
| L | L_g (nm) | 10.2 | 9.2 | 8.2 | 7.4 | 6.6 | 5.9 |
| | EOT (nm) | 0.8 | 0.75 | 0.71 | 0.68 | 0.64 | 0.6 |
| | V_{dd} (V) | 0.65 | 0.63 | 0.61 | 0.59 | 0.56 | 0.54 |
| H | L_g (nm) | 9.7 | 8.9 | 8.1 | 7.4 | 6.6 | 5.9 |
| | EOT (nm) | 0.59 | 0.56 | 0.53 | 0.5 | 0.47 | 0.45 |
| | V_{dd} (V) | 0.66 | 0.64 | 0.62 | 0.61 | 0.59 | 0.57 |

LSTP: low stand-by power; HP: high performance; L_g : gate length; EOT : effective oxide thickness; V_{dd} : supply voltage

TABLE II
PARAMETER DEPENDENCE ON THE NUMBER OF MoS₂ LAYERS [1], [3], [15], [25], [27]–[29]

| # of MoS ₂ layers | | 1 | 2 | 3 |
|--|---|---------|------------------|-------------------|
| Mobility ($\text{cm}^2/\text{V}\cdot\text{s}$) | Experimental (the same recipe) | ~10 | ~20 | ~30 |
| | Theoretical (high- k environment) | ~60 | ~95 [#] | ~130 [#] |
| | $\epsilon_{\parallel}/\epsilon_{\perp}$ | 2.8/4.2 | 4.2/6.5 | 4.9/7.5 |
| ΔE_{K-A} (meV) | | 270 | 190 | 130 |

$\epsilon_{\parallel}/\epsilon_{\perp}$: in-plane/out-of-plane dielectric constant; ΔE_{K-A} : energy difference between the lowest K valley and the second lowest A valley; [#]: interpolated values between 1L and bulk mobility.

parameters dependent on the number of 2D semiconductor layers [1], [3], [15], [25], [27]–[29] are listed in Table II. Note that the effective masses of MoS₂ and other typical semiconductors negligibly change with the number of layers [15]. Theoretical mobility limits in Table II are used for MoS₂, while an optimistic mobility of $200 \text{ cm}^2/\text{V} \cdot \text{s}$ is used for the Si device in the simulations. A high source/drain doping of $6.5 \times 10^{13} \text{ cm}^{-2}$ is used to ensure ohmic source/drain to metal contacts [13], [30].

C. Developed Quantum Transport Solver

Scattering events are basically inevitable in a practical device environment, which should be taken care of in the device simulation. Besides phonon scattering, other scattering sources, such as electron-electron scattering, impurity/defect scattering, and so on, may also exist in the devices. Including all these scattering sources into the numerical simulation is computationally unaffordable. Venugopal *et al.* [31] and Anantram *et al.* [32] developed an approach based on the concept of Büttiker probes [33], to treat the scattering events in electronic devices. This approach is capable of capturing the essential physics of scattering while being computationally efficient. Fig. 2(a) and (b) shows a schematic of Büttiker probes, which can be briefly described as follows. These probes absorb carriers passing by, and disturb their momentum and energy, and then desorb them back into the channel, just like the effect of real scattering events, while they do not change the number of carriers passing by, i.e., the net current (I_i) at each probe (i) remains zero

$$I_i = \int_{-\infty}^{\infty} I_i(E_l) dE_l = 0 \quad (1)$$

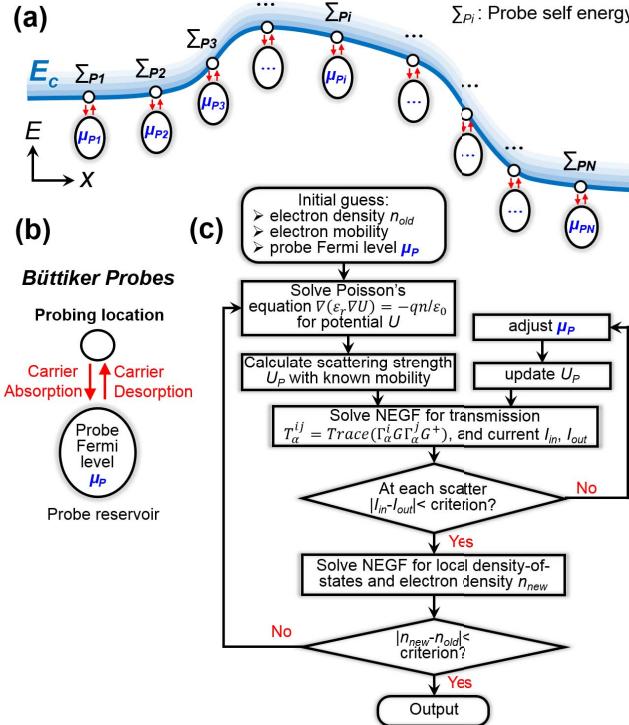


Fig. 2. (a) The conduction band (E_c) of a typical n-type MOSFET from source (left) to drain (right) and the concept of Büttiker probes in the treatment of scattering events. (b) Zoomed-in view of a single Büttiker probe, which is inserted at every mesh point along the channel. The probe Fermi levels μ_{Pi} ($i = 1, 2, \dots, N$) are adjusted to obtain zero net current at each scatter. \sum_{Pi} : probe self-energies. (c) Programming scheme in the simulation. q is the elementary charge, ϵ_r is dielectric constant, and ϵ_0 is the permittivity of vacuum. Γ_α^i is the broadening function [32]. All the parameters are calculated at each location in the device. Note that the entire simulation process essentially involves solving partial differential equations, which are converted to matrix equations for numerical solutions. The matrix form accounts for properties at all mesh points in the device. The matrix equation provides a vector solution, which inherently includes the simultaneous solutions at all mesh points in the device.

where E_l is the longitudinal component (along the device length direction) of the total energy of the charge carriers, and

$$I_i(E_l) = \frac{q}{\hbar^2} \sum_\alpha \sqrt{\frac{2m_t k_B T}{\pi^3}} \sum_j T_\alpha^{ij} \left\{ \mathcal{F}_{-1/2}(\mu_{Pi} - E_l) - \mathcal{F}_{-1/2}(\mu_{Pj} - E_l) \right\} \quad (2)$$

where q is the elementary charge, \hbar is the reduced Planck's constant, m_t is the transverse effective mass (along the device width direction) of carriers, α is the transverse mode index, i/j denote the probe index, k_B is Boltzmann's constant, T is the temperature, $\mu_{Pi/j}$ are the Fermi levels assigned to each probe, $\mathcal{F}_{-1/2}$ is the Fermi-Dirac integral of order $-1/2$ [34], and T_α^{ij} denotes the transmission between probes i and j through transverse mode α . In the outer loop of the self-consistent simulation scheme [Fig. 2(c)], Poisson's equation is solved to obtain the electrostatics, and effective mass transport equation is solved with a nonequilibrium Green's function (NEGF) [32]

$$G = [EI - H - \Sigma]^{-1} \quad (3)$$

to get charge distribution. Here, E is the energy, I is an identity matrix, H is the device Hamiltonian that defines

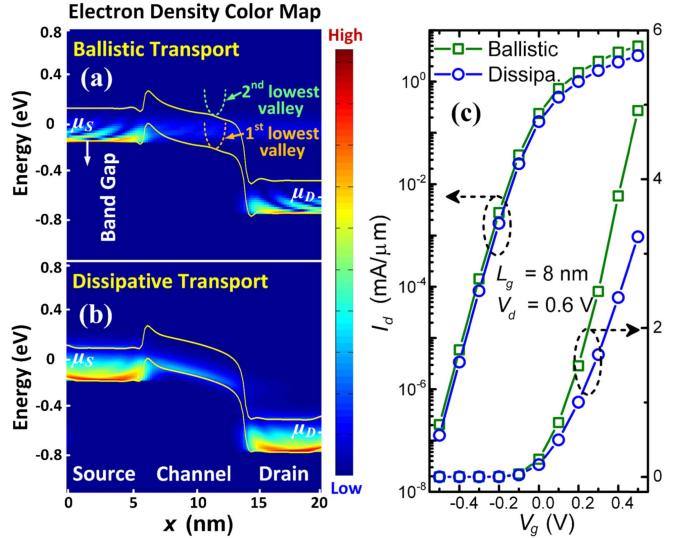


Fig. 3. Energy resolved electron density (brighter color indicates higher density). (a) Ballistic transport—electron wave propagates without energy relaxation (flat color contour in the channel). (b) Dissipative transport—carriers keep relaxing energy (bent color contour in the channel). (c) Transfer characteristics in linear scale (right) and log scale (left) show that drain current is overestimated by the ballistic simulation even for gate length as small as 8 nm.

the rule for the carrier behavior in the device, and Σ is the self-energy matrix. The interlayer coupling term in the device Hamiltonian for multilayer devices is set to be zero, due to the weak interlayer interaction [15]. In the inner loop, once transmission T_α^{ij} and current distribution I_{in} and I_{out} are obtained from NEGF, $\mu_{Pi/j}$ are adjusted to meet the current continuity requirement i.e., equation (1). The key parameter in this dissipative transport quantum simulation, scattering strength (U_P), is obtained from experimentally measurable low-field mobility, and described in the form of probe self-energy \sum_{Pi} . Readers are referred to [31] for more detailed information about this approach.

D. Dissipative Versus Ballistic Transport

Fig. 3(a) and (b) shows the electron density color map obtained with the ballistic transport simulation as well as the dissipative transport simulation used in this paper, respectively. The difference in essential physics can be clearly observed from the fact that the electrons keep relaxing energy during dissipative transport from the source to the drain, compared with the conserved energy during the ballistic transport. On the other hand, the drain current predicted by ballistic and dissipative transport simulations is also different even for gate length as small as 8 nm, as shown in Fig. 3(c), indicating the necessity of dissipative transport simulation in accurately evaluating the performance of MoS₂ FET and other 2D FETs.

III. RESULTS AND DISCUSSION

A. Device Electrostatics Evaluation

In short-channel FETs, fringing electric fields from source/drain regions could be strong enough to laterally penetrate through the channel and spacer/gate dielectric, and affect the channel potential, thereby degrading the gate control, and leading to the so-called short-channel effect [35]. The use of

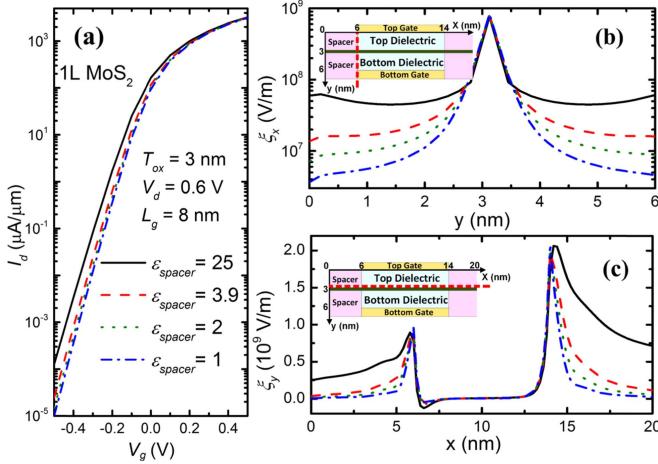


Fig. 4. (a) Transfer characteristics show improved subthreshold characteristics using low- k spacer. ϵ_{spacer} is the dielectric constant of the spacer material. (b) Lateral component ξ_x (along the x -direction) of electric field at the source/channel junction. (c) Vertical component ξ_y (along the y -direction) of electric field at the gate dielectric/channel interface. Insets in (b) and (c): cross-sectional view of the device topology being studied. Dashed red lines (insets): locations where electric fields are extracted. Note that the effect of spacer uncovered is valid in all the operational regions of the 2D FET.

2D semiconductors as FET channel significantly eliminates the fringing electric field path through the channel because of their atomic scale thickness. However, the path through spacer/gate dielectric cannot be eliminated, because the gate dielectrics have to be thick enough, especially for high- k dielectric in the mainstream technology, in order to suppress gate leakage. Although gate dielectrics have to be high- k material for good gate control, the spacers do not have to be. Fig. 4(a) shows the subthreshold characteristics of monolayer (1L) MoS₂ FET with different spacers (i.e., different dielectric constants). It can be observed that low- k spacers provide steeper subthreshold slopes, which is attributed to the fact that fringing electric fields from the source/drain are suppressed by low- k spacers, as confirmed by the lateral component ξ_x and the vertical component ξ_y of fringing electric fields shown in Fig. 4(b) and (c), respectively. The red dashed lines in Fig. 4(b) and (c) (insets) represent the locations, where ξ_x and ξ_y are extracted, respectively. In the remaining sections, SiO₂ is used as spacer material if not specified otherwise.

In Fig. 5(a) and (b), subthreshold swing (SS) and drain-induced-barrier-lowering (DIBL), which are two important indicators of device electrostatics, are evaluated for both the DG and the SOI structures from the monolayer (1L) to the three layer (3L) MoS₂ as well as for Si-based ultrathin-body (Si UTB) DG FETs. It is shown that 2D MoS₂ FETs outperform Si devices because of their atomically thin channel. On the other hand, SOI topology can only sustain good electrostatics for 1L MoS₂, while DG topology can do so for up to 3L. The reason is that channel potential in SOI devices is greatly affected by the source/drain fringing electric field through the thick bottom gate dielectric, which is effectively suppressed in DG devices. Therefore, the SOI topology is less capable of deriving the real advantages of 2D FETs. In the following sections (from section III.B until the end of this paper), discussions on 2D FETs will be focused on

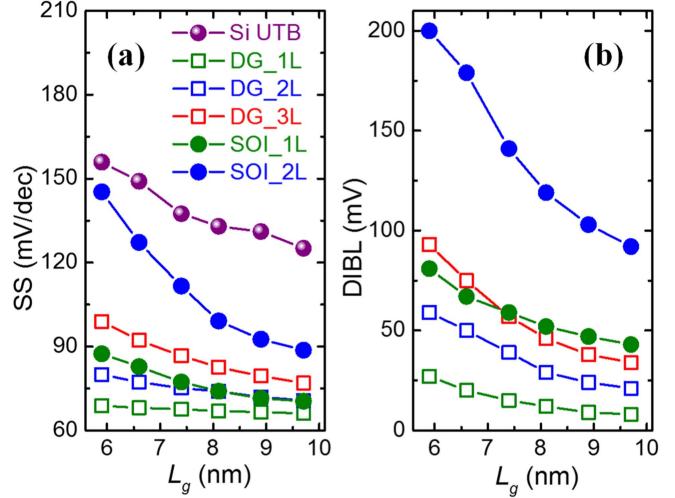


Fig. 5. (a) SS and (b) DIBL with gate length scaling for 1L–3L MoS₂ FETs, and Si UTB DG FETs (only SS shown). DG and SOI: double-gate and semiconductor-on-insulator structures, respectively.

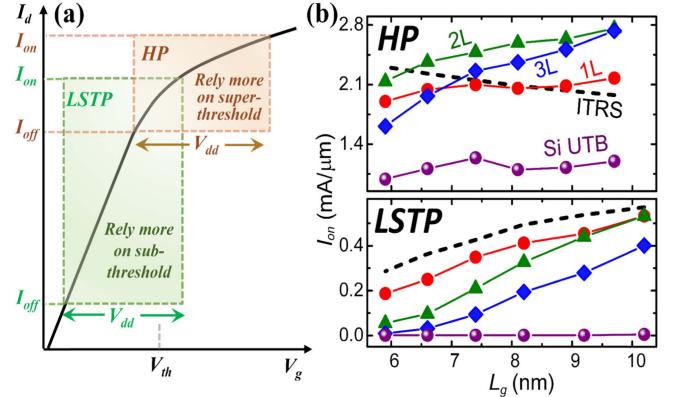


Fig. 6. (a) Schematic of the method used for obtaining I_{ON} and the design priorities for LSTP and HP technologies. (b) ON-current (I_{ON}) versus gate length for 1L–3L MoS₂ FETs, and Si UTB DG FETs. Black dashed lines: ITRS requirement for I_{ON} . HP and LSTP: high-performance and low-standby-power technologies, respectively.

the DG topology with 1L, 2L, and 3L 2D semiconductor as channel.

B. ON-Current Evaluation

The performance and power consumption are the two most important measures for FETs in very large-scale integration (VLSI) application. At a certain technology node (with fixed supply voltage V_{dd}), the standby or leakage power can be controlled by adjusting the device threshold voltage V_{th} , which can be realized by tuning the work function of gate material, or the doping density in the channel, and hence the OFF-current I_{OFF} . In particular, the low-standby-power (LSTP) application requires high V_{th} , which inevitably limits the overdrive $V_{\text{dd}} - V_{\text{th}}$, and hence ON-current I_{ON} , or the device performance. In contrast, the HP application requires large $V_{\text{dd}} - V_{\text{th}}$ to achieve high I_{ON} , which inevitably lowers V_{th} , and hence increases the standby power consumption. In this paper, I_{ON} is evaluated with I_{OFF} fixed, according to the ITRS requirements [26], as 100 nA/ μm for HP and 10 pA/ μm for LSTP applications, respectively, as schematically shown in Fig. 6(a). It is apparent that the HP relies more on the

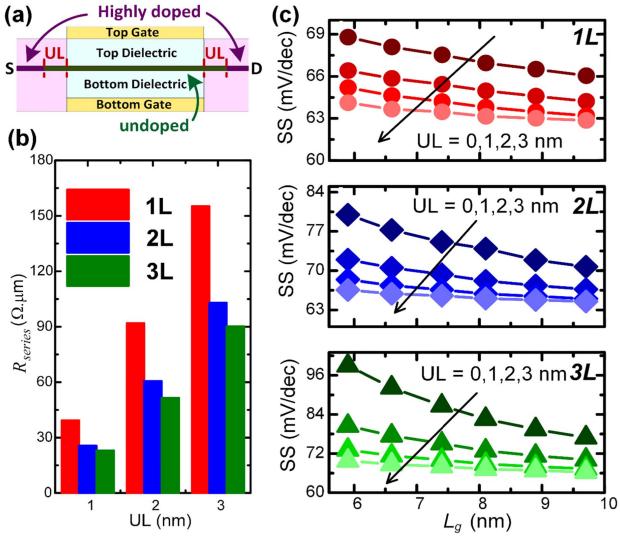


Fig. 7. (a) Schematic of UL structure. (b) Introduced series resistance R_{series} by UL, with respect to the case of UL = 0 nm. (c) SS improvement for 1L–3L MoS₂ FETs, using the UL structure.

superthreshold characteristics, while the LSTP relies more on the subthreshold characteristics, which has important implications: 1) the HP relies more on parameters, such as carrier mobility, density-of-states (DOS), and series resistance and 2) the LSTP relies more on device electrostatics, or SS. In particular, small SS helps reduce V_{th} , and thereby in increasing $V_{\text{dd}} - V_{\text{th}}$, and I_{ON} for the LSTP. Fig. 6(b) shows the calculated I_{ON} for 1L–3L MoS₂ FETs and Si UTB devices for both the HP and the LSTP applications. Si devices show very low I_{ON} compared with MoS₂ FETs, because of their poor electrostatics, as reflected in Fig. 5(a). It is also found that, for HP, 2L case provides the highest I_{ON} , and can meet the requirement up to the 6.6 nm node. In contrast, for LSTP, 1L is the closest to, although still lower than, the requirement. Compared with 1L, 2L and 3L have higher DOS for conduction and higher mobility, and thus higher current drive capability, so they have higher I_{ON} for HP. The 3L case shows lower I_{ON} than the 2L, because its worse electrostatics and hence large SS begins to degrade I_{ON} for HP, which is reflected by the rapid decreasing rate of I_{ON} with reduced L_g . Therefore, >3L must be avoided for sub-10 nm nodes. 1L has the best electrostatics, and thus the highest I_{ON} for LSTP.

C. Design Considerations

Given the inability of MoS₂ FETs in fulfilling the HP requirement at the smallest 5.9 nm node, and LSTP requirement for all sub-10 nm nodes, natural tendencies are to improve the device electrostatics and improve the mobility as discussed below.

1) *Underlap Structure:* The underlap (UL) structure, as schematically shown in Fig. 7(a), could be a choice for the former goal. Although UL increases the effective channel length, thereby introducing series resistance R_{series} in the UL regions, as shown in Fig. 7(b), for 1L–3L cases, it does lower SS for all 1L–3L cases, especially when gate length becomes short, as shown in Fig. 7(c), because it reduces

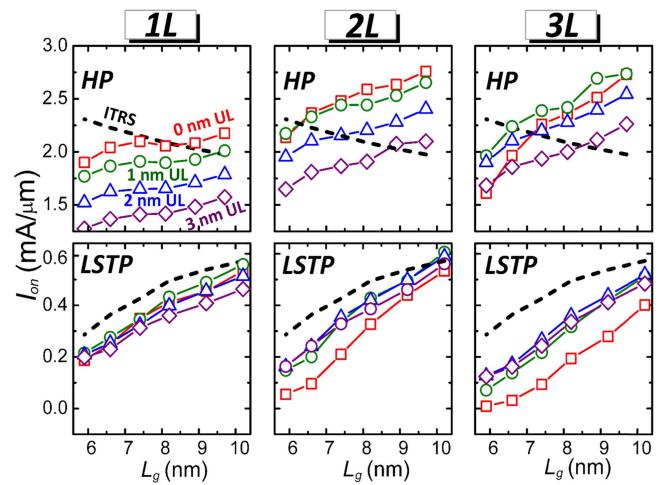


Fig. 8. I_{ON} versus gate length for 1L–3L MoS₂ FETs with the UL of 0, 1, 2, 3 nm. The top three plots are for HP, and the bottom three are for LSTP.

the source/drain-to-channel capacitive coupling, thereby suppressing the short-channel effect. These two conflicting trends determine that the length of UL should be optimized to obtain the highest I_{ON} , which is shown in Fig. 8 for 1L–3L MoS₂. SS and R_{series} primarily describe or affect the subthreshold and superthreshold characteristics, respectively, which indicates that in terms of the effects of UL, the HP relies more on R_{series} , while the LSTP relies more on the SS.

The top three subplots of Fig. 8 show the results for the HP application. For 1L case, UL simply reduces I_{ON} , because 1L device already has very good device electrostatics, the improvement in SS with UL cannot compensate the current loss due to introduced R_{series} . For 2L case, SS becomes larger compared with that of 1L [Fig. 7(c)], which indicates that the 2L device has more room for the SS improvement with UL. 1 nm UL begins to help a little bit at very small nodes. For 3L case, UL (1 and 2 nm) helps a lot, but sadly because the electrostatics of 3L devices are so poor that the effect of SS improvement begins to prevail over the effect of increased R_{series} . Even with the help of UL, the performance of 3L devices cannot compete with 2L devices, as a consequence of the mixed effects of mobility, DOS, SS, and R_{series} .

The bottom three subplots of Fig. 8 show the results for the LSTP application. For 1L case, 1 nm UL offers the highest I_{ON} , since further increasing UL does not help lower SS much while introduces much R_{series} , thus degrades I_{ON} . For 2L and 3L cases, large UL is desired, but its role is nothing but to simply compensate for the current loss caused by the relatively large SS of 2L and 3L devices. Based on above observations and analyses, 2L MoS₂ with 0–1 nm UL is optimal for HP, and 1L MoS₂ with 1 nm UL is optimal for LSTP.

2) *Mobility Improvement:* To estimate how much improved mobility can help, the ballistic transport simulation (UL is not used) is performed to obtain I_{ON} , as shown in Fig. 9. It can be observed that the HP requirement of all the nodes can be met (with 1L or 2L), while LSTP requirement beyond 7 nm node cannot, indicating that the HP requires high mobility, while only high mobility is not sufficient for the LSTP beyond 7 nm

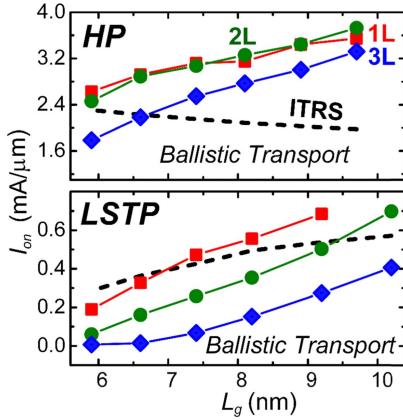


Fig. 9. I_{ON} versus gate length for 1L–3L MoS₂ FETs obtained by ballistic simulation.

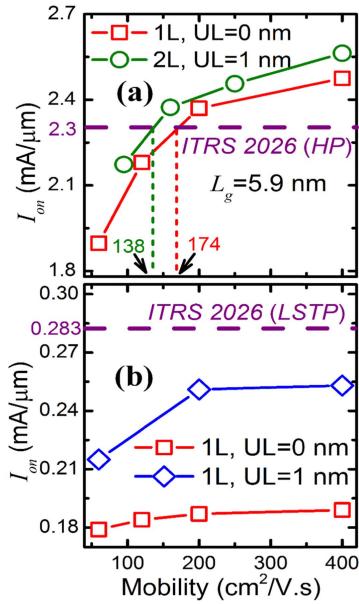


Fig. 10. Mobility improvement in order to meet (a) HP and (b) LSTP requirements at the 5.9 nm node.

nodes. As expected, the smallest 5.9 nm node is the most challenging one, which is the focus in the remaining sections. The dissipative transport simulation is performed to study how high the mobility should be in order to meet the requirements at the 5.9 nm node. The obtained optimal combinations—2L device with 1 nm UL for HP, and 1L device with 1 nm UL for LSTP—are studied. The 1L device without UL is also simulated as a reference for comparison. Note that when varying the mobility, only scattering rate is changing, effective mass is artificially kept the same. As shown in Fig. 10(a), the 2L device with 1 nm UL needs a mobility of 138 cm²/V·s to meet the HP requirement, while 1L device without UL needs 174 cm²/V·s. Note that the former is expected to be much easier to achieve than the latter, since carriers in 2L would experience less scattering compared with that in 1L, which has been indicated by the observed increasing trend of mobility with the number (or thickness) of 2D material layers in Fig. 1(c). Such mobility boost can be achieved by engineering the dielectric environment, such as inserting h-BN buffer layer between a high- k dielectric

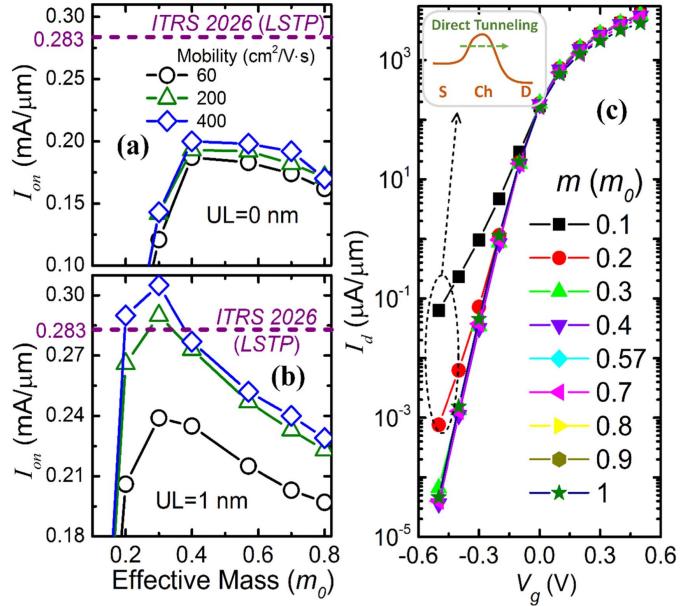


Fig. 11. Effective mass is varied to meet the LSTP requirement at 5.9 nm node in the case of (a) UL = 0 nm and (b) UL = 1 nm. (c) I_d – V_g curves for different effective mass. The inset sketch shows direct tunneling from source to drain, which degrades the SS for very small effective masses.

and a 2D channel [36]. The other solution is to employ high-mobility 2D semiconductors. The 1L tungsten diselenide (WSe₂) has been found to exhibit mobility as high as 200 cm²/V·s [12], [13], and thus, is more promising than MoS₂ for HP applications. On the other hand, it is found that improving the mobility of 1L device with 1 nm UL for LSTP, although helpful, is still not sufficient to meet the requirement, as shown in Fig. 10(b), which indicates that MoS₂, even in its perfect condition, is not able to satisfy LSTP application requirements at the 5.9 nm node. Therefore, other 2D semiconductors have to be explored.

3) *Role of Effective Mass:* For different 2D semiconductors, the primary difference for the FET application, beside the bandgap, which itself is irrelevant for the topic in this paper, as long as it is large enough ($\gg kT$) to suppress minority carrier leakage, is the carrier effective mass. Fig. 11 shows the effect of effective mass for different carrier mobilities, in the case of UL = 0 nm in (a), and UL = 1 nm in (b). Here, the effective mass is assumed to be roughly equal along different directions, which is valid for TMDs—the largest 2D semiconductor family known so far. It can be observed that without UL, varying effective mass, or equivalently using other 2D materials does not help. With the aid of 1 nm UL, a certain 1L 2D material of effective mass of $\sim 0.3 m_0$, can meet the 5.9 nm node LSTP requirement as long as its mobility can reach 190 cm²/V·s. It is interesting to notice that Fig. 11(a) and (b) shows an optimal region for effective mass, i.e., too large or too small effective masses both can degrade device performance. The reasoning is as follows. Large effective mass damps carrier velocity by

$$v = \frac{1}{\hbar} \frac{dE}{dk} = \frac{\hbar k}{m} \quad (4)$$

where \hbar is the reduced Planck's constant, E is the energy, k is the wave vector, and m is the effective mass. In other

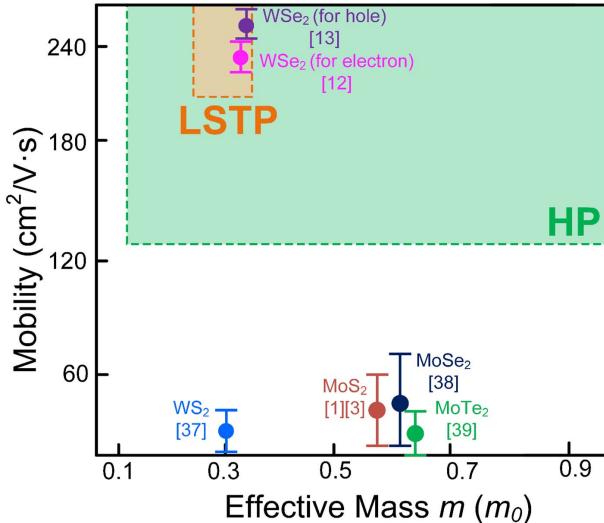


Fig. 12. Collected data for mobility (from experiments) and effective mass (based on first principle calculations) [14], [15] for various 2D semiconductors (1L–2L). Green block: required range of values for HP. Orange block: required range of values for LSTP.

words, smaller effective mass is desired to achieve higher carrier velocity, and hence I_{ON} . However, aggressively small effective mass leads to source-to-drain direct tunneling leakage [schematically shown in Fig. 11(c) (inset)], since the probability of carriers tunneling through a potential barrier, according to quantum mechanics, exponentially increases with the reduced carrier effective mass, i.e., $T \propto e^{-h\sqrt{m}}$, where h is a function of barrier width and height. Therefore, SS [see the subthreshold characteristics circled in Fig. 11(c)] and hence, I_{ON} are severely degraded. The use of 1 nm UL effectively delays the appearance of source-to-drain direct tunneling leakage with decreasing effective mass, and thus is able to derive more benefit from carrier velocity improvement, which is the reason that UL can help boost I_{ON} and meet the LSTP requirement, as shown in Fig. 11(b).

4) Benchmarking TMD Semiconductors: Fig. 12 collects currently available data, to the best of our knowledge, of the mobility (experiments) and effective mass (first-principle calculations) of 2D TMD semiconductors in [1], [3], [12]–[15], and [37]–[39]. It is found that beside the high carrier mobility, WSe₂ happens to own the suitable effective mass for the most challenging 5.9 nm node, i.e., WSe₂ is able to meet the requirement of all the nodes in the current road map, which may be a compelling reason for material and device scientists to invest more efforts on this material in the future. In contrast, MoS₂ needs extra efforts in improving its mobility and modifying its effective mass by advanced techniques, such as strain engineering [35] and using h-BN buffer layer at the dielectric/channel interface [40], [41]. An intrinsic energy-delay benchmark [26], [42], [43] for 1L–3L MoS₂ FETs and WSe₂ FETs is provided, as shown in Fig. 13. The in-production CMOS at 15 nm node (“node” here is not gate length, the actual gate length is much larger than 15 nm) [43], and theoretically predicted III–V tunnel FET (TFET) at $L_g = 15$ nm, and $V_{dd} = 0.4$ V [44] are also shown for comparison. It is found that 1L WSe₂ FET (with 1 nm UL for LSTP) can offer the lowest intrinsic delay

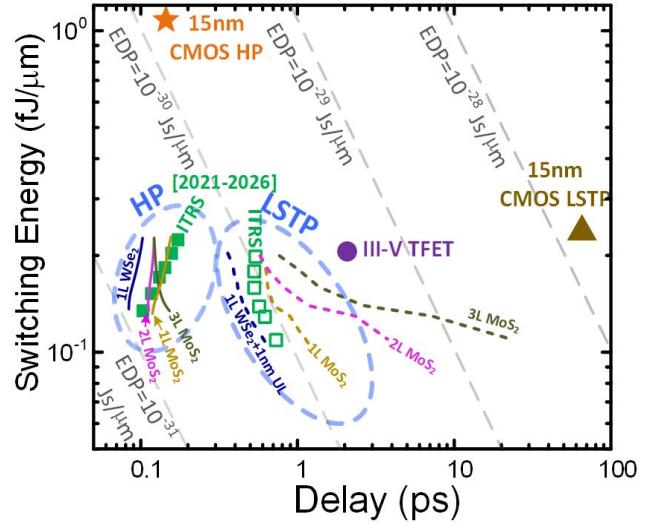


Fig. 13. Energy and delay benchmark of MoS₂ FETs and the proposed WSe₂ FETs for HP and LSTP. EDP: energy delay product. 15 nm CMOS are based on the state-of-the-art FinFET technology [26]. The III–V TFET is based on a theoretical prediction [44].

and energy-delay product (EDP), even lower than the ITRS requirement.

D. Possible Solutions for Sub-5 nm Nodes

Although WSe₂ has been found to be the right material for up to 5.9 nm node, it can only marginally meet the requirement, i.e., it is hard to apply this material beyond the current road map, i.e., for sub-5 nm nodes. Therefore, it would be insightful to explore possible solutions, by which there should be sufficient performance margin available at the 5.9 nm node, for their possible use in sub-5 nm nodes. Based on our extensive simulation study, using anisotropic 2D semiconductors with anisotropic effective mass are found to be a promising direction for HP applications.

1) Anisotropic 2D Materials: In order to investigate how much performance advantage over the WSe₂ device can be gained by using an anisotropic material which has different effective masses along (m_x) and perpendicular to (m_z) the transport direction, the carrier mobility of $200 \text{ cm}^2/\text{V}\cdot\text{s}$ and 1 nm UL are intentionally used for each material in the simulation. As can be found in Fig. 14, m_x displays similar behavior (an optimal value exists for both HP and LSTP), while m_z plays a different role in the HP (left) and the LSTP (right). HP prefers suitably low m_x ($\sim 0.15 m_0$) and high m_z , while LSTP prefers m_x of $\sim 0.3 m_0$, and is nearly independent of m_z . Qualitatively speaking, the dependence of I_{ON} on m_x is similar for HP and LSTP. When m_x is large, carrier velocity is low, which limits I_{ON} . When m_x is too small, direct source–drain (S–D) tunneling leakage occur, which degrades SS, thereby limiting I_{ON} . Quantitatively speaking, I_{ON} for HP degrades more with large m_x leading to low carrier velocity, while is less sensitive to small m_x and hence to S–D tunneling leakage, because the HP relies more on the superthreshold characteristics. In contrast, I_{ON} for LSTP degrades more with small m_x and hence with S–D tunneling leakage while is less sensitive to large m_x and hence to low carrier velocity, because the LSTP relies more on the subthreshold characteristics.

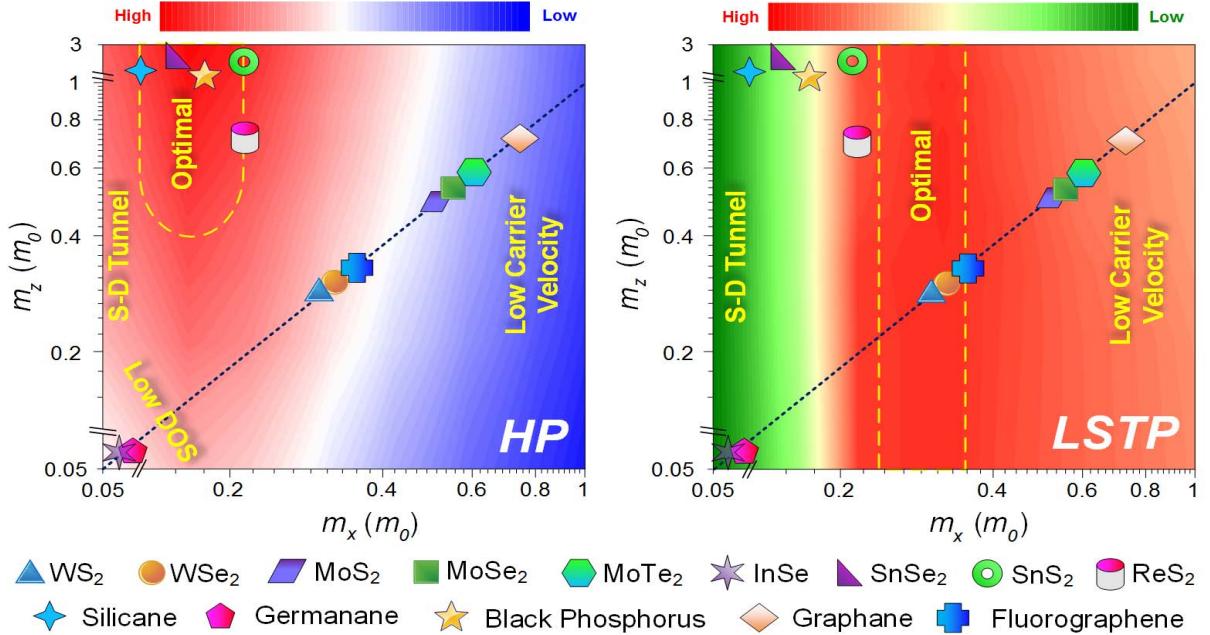


Fig. 14. I_{ON} (color contour) versus effective mass along (m_x) and perpendicular to the (m_z) transport direction for the HP (left) and the LSTP (right) at 5.9 nm node. Carrier mobility of $200 \text{ cm}^2/\text{V} \cdot \text{s}$ that is the minimum requirement for the mobility value of any 2D material that is targeted to outperform WSe₂, and 1 nm UL are intentionally used in the simulation in order to compare with the WSe₂ device. Some typical 2D semiconductors [14], [15], [18], [20], [46]–[49] are used for benchmarking. The dashed dark blue lines in both plots represent isotropic materials, i.e., $m_x = m_z$.

It is worthwhile to note that the curve with the mobility of $200 \text{ cm}^2/\text{V} \cdot \text{s}$ in Fig. 11(b) is the isotropic case (short-dashed dark blue line) in the right plot of Fig. 14, the color contour of which in turn verifies the phenomena in Fig. 11(b) that the slope at the left-hand side of the I_{ON} peak is much sharper than that at the right-hand side. It can be found that small m_z significantly degrades I_{ON} for HP, especially at small m_x . The reason is that m_z can noticeably affect the DOS of 2D material,

$$\text{DOS} = \frac{g_s g_v \sqrt{m_x m_z}}{2\pi \hbar^2} \quad (5)$$

where g_s and g_v are the spin and valley degeneracies, respectively. When m_x is also small, the DOS becomes too low to support adequate current drive. This effect has been reported in FETs based on III–V materials which are known for their small effective mass and low DOS, and has been named source starvation [45]. On the other hand, large m_z can increase DOS, and boost I_{ON} for HP. Therefore, suitable anisotropic materials can be very promising for HP application. The weak dependence of I_{ON} on m_z for LSTP results from the weak dependence of LSTP on the superthreshold characteristics, and hence on DOS.

Some typical 2D semiconductors [14], [15], [18], [20], [46] are benchmarked at 5.9 nm node in Fig. 14. Note that some 2D materials, such as graphene (monolayer and bilayer), germanene, and silicene, are not included because of their zero or ultrasmall bandgaps, or the difficulty to artificially open up a bandgap, which make them unsuitable for low-power VLSI applications. It is found that silicene, SnS₂, SnSe₂, ReS₂, and black phosphorus are within the optimal effective mass range for HP application, and have noticeable performance margin at the 5.9 nm node, as long as their mobility can reach $200 \text{ cm}^2/\text{V} \cdot \text{s}$, which is quite feasible because of their

smaller effective mass (with respect to that of WSe₂) along the transport direction. In contrast, the most promising candidate for the LSTP application remains to be WSe₂, as well as WS₂ and fluorographene whose effective masses are close to that of WSe₂. It is worthwhile to note that besides the intrinsically anisotropic materials, strain engineering can be employed to produce artificial anisotropic materials with desired properties, which could be a more flexible direction.

2) V_{dd} Barrier and Transport Mechanism Revolution: Although anisotropic materials are beneficial to the HP application, they do not help the LSTP. During the extensive simulation study, we identified the most stringent scaling constraint or performance limiter— V_{dd} . Fig. 15(a) shows the obtained I_{ON} from 1L MoS₂ FETs (having no special design, such as UL or mobility improvement) with and without V_{dd} scaling. It can be found that if V_{dd} is not scaled (fixed at 0.66 V for HP, and 0.65 V for LSTP) below 10 nm node, ITRS requirement can be easily met at all nodes in the current roadmap, and sufficient performance margin remains, which indicate that for sub-5 nm nodes, the constraint on V_{dd} can be suitably relaxed to achieve a balance between the power consumption and the performance. The other direction is to abandon the thermionic emission transport-based MOSFETs, and resort to sub- kT/q switches, such as tunneling field-effect transistors (TFETs) based on 2D materials [50], which can provide steeper (subthermionic) turn-ON characteristics ($SS < 60 \text{ mV/decade}$) and can potentially retain the same I_{ON} at reduced V_{dd} , as schematically illustrated in Fig. 15(b). It is worthwhile to note that sub- kT/q switches (based on bulk materials) with low turn-ON current does not help [see Fig. 15(b) (green dashed line)], which unfortunately happens to be the current situation for all experimentally reported TFETs. Employing 2D materials as the channel material of TFET can help alleviate this issue, because they possess

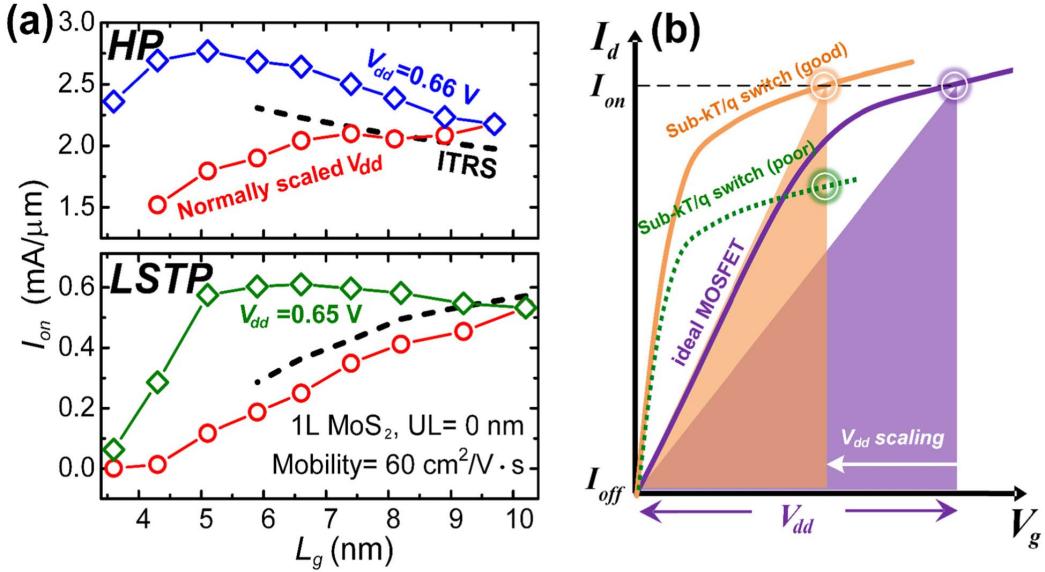


Fig. 15. (a) I_{ON} versus gate length for scaled and unscaled supply voltage V_{dd} . Both the HP and the LSTP requirements at all nodes in the current road map, even in some sub-5 nm nodes can be met (based on the trends of the black dash lines that are nearly straight). (b) Using sub- kT/q switches to conquer the V_{dd} barrier. The poor (good) sub- kT/q switch refers to low (high) turn-ON current level.

TABLE III
SUMMARY OF POSSIBLE MATERIAL/STRUCTURE/TECHNOLOGY CHOICES FOR SUB-10 nm HP AND LSTP VLSI APPLICATIONS. THE OPTIONS WITH ORANGE COLOR REPRESENT THE LESS PREFERRED ONES, WHICH NEED A LOT OF EFFORTS IN IMPROVING THE PROPERTIES OF MoS₂

| L_g | > 6.6 nm | 5 nm – 6.6 nm | < 5 nm |
|-------|--|--|--|
| HP | 2L MoS ₂ or other high mobility TMDs | <ul style="list-style-type: none"> ➤ 2L MoS₂ with 1nm UL & improve carrier mobility to > 138 cm²/V·s ➤ 1L or 2L WSe₂ | Anisotropic materials such as black phosphorus, SnSe ₂ , silicane, etc. |
| LSTP | <ul style="list-style-type: none"> ➤ 1L MoS₂ with 1 nm UL, & improve carrier mobility to > 190 cm²/V·s, & engineer the effective mass to be $\sim 0.3m_0$ ➤ 1L WSe₂ with 1nm UL | Sub-kT/q switch such as 2D tunnel FET | |

unique advantages compared with bulk materials for the TFET application. On one hand, their dangling bond-free surface can effectively suppress the trap assisted tunneling leakage and further improve the SS. On the other hand, their ultrathin body significantly enhances the gate control (electrostatics), and helps to reduce the tunnel barrier width, thereby increasing the tunneling probability and turn-ON current [50]. Additionally, judiciously selected 2D materials can be used to create heterojunctions with desired band offsets (or low tunnel barrier height) to allow ultralow voltage TFET operation. Therefore, 2D material-based TFETs can be very promising and can potentially lead to a paradigm shift in low-power electronics.

IV. CONCLUSION

The performance and scalability of emerging 2D semiconductor-based FETs are comprehensively evaluated for sub-10 nm nodes, through rigorous dissipative quantum transport simulations. It is found that the most widely studied MoS₂ is not intrinsically promising for sub-10 nm VLSI application. Extra efforts, including using an h-BN

buffer gate dielectric layer to improve its mobility, the UL structure to improve device electrostatics, and strain engineering to modify its effective mass, are needed to meet the ITRS requirement. On the other hand, WSe₂ intrinsically outperforms MoS₂ for sub-10 nm VLSI applications, because of its high mobility and suitable effective mass, which enables it, with the aid of UL structure, to meet all the requirements in the current VLSI technology road map. Beyond the current road map, i.e., for sub-5 nm nodes, anisotropic materials and sub- kT/q switch, such as 2D TFET, are identified as potential solutions for HP and LSTP applications, respectively. Table III summarizes the preferred materials/structure/technology for 2D FETs for sub-10 nm VLSI. Although this paper focused on the n-type device, the uncovered paths toward device scaling and design optimization are universal, which provides a straightforward reference to the design of p-type devices. Finally, while the 2D materials considered in this paper do not represent an exhaustive list, the methodology developed for benchmarking along with the device design strategies can be readily extended to other 2D semiconductors.

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