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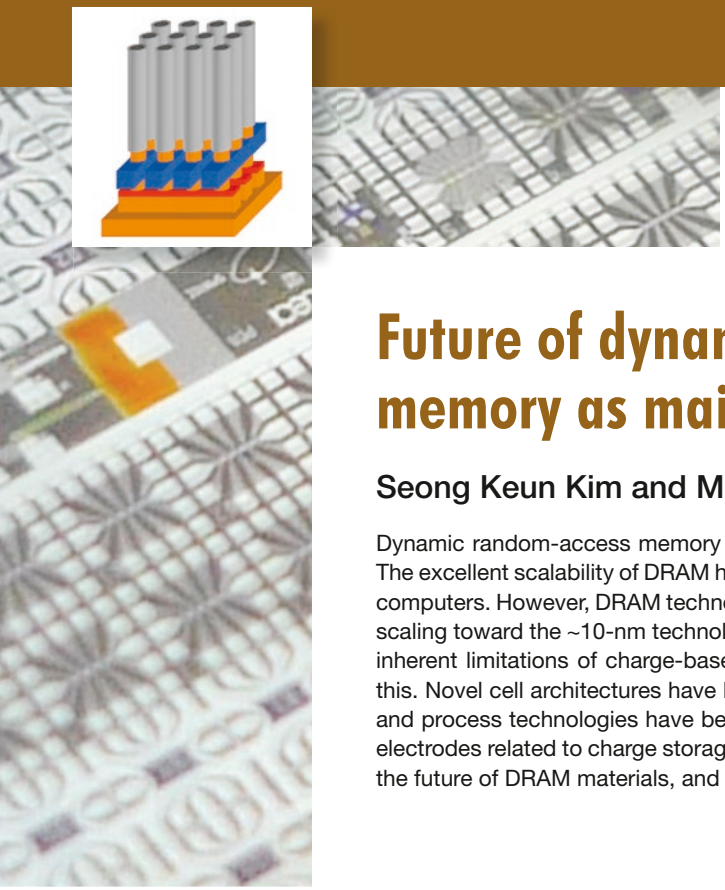

Future of dynamic random-access memory as main memory

Seong Keun Kim and Mihaela Popovici

Dynamic random-access memory (DRAM) is the main memory in most current computers. The excellent scalability of DRAM has significantly contributed to the development of modern computers. However, DRAM technology now faces critical challenges associated with further scaling toward the ~10-nm technology node. This scaling will likely end soon because of the inherent limitations of charge-based memory. Much effort has been dedicated to delaying this. Novel cell architectures have been designed to reduce the cell area, and new materials and process technologies have been extensively investigated, especially for dielectrics and electrodes related to charge storage. In this article, the current issues, recent progress in and the future of DRAM materials, and fabrication technologies are discussed.

Introduction

Dynamic random-access memory (DRAM) has served as the main memory in modern computers since it was introduced by Intel Corporation in 1972. DRAM is widely used in modern computers owing to characteristics such high-speed operation, large integration density, and excellent reliability.

A DRAM cell has a simple structure comprising one capacitor (1C) connected by one transistor (1T) (1T-1C) to the bit line (the line through which information is written to/read from the memory cell) (**Figure 1**a). The access transistor is connected to the word line and acts as a switch. The capacitor stores each bit of data as a negative or positive electrical charge. The memory state is read by sensing the stored charge on the capacitor via the bit line, which is set to $V_{cc}/2$, (V_{cc}: operating voltage of the chip) with the transistor closed. When the access transistor is on, the stored charge carriers flow into the bit line, which changes its potential. This voltage change is detected and amplified by the sense amplifier connected to the bit line.

During the past several decades, exponential growth in the number of memory cells per chip has occurred. Perpetual memory cell scaling has been the major strategy for realizing rapid increases in memory density.[1] DRAM is amenable to scaling because of its simple structure, and scaling of DRAM down to a ~100-nm technology node (specific manufacturing process and its design rule) is easily achieved with traditional materials such as Si-based dielectrics (SiO_2 and SiN_x) and electrodes (poly-Si). This excellent scalability of DRAM has led to its long-lasting success. Today, much effort is devoted to accelerating the scaling of DRAM cells further to the ~10-nm technology node[2] (Figure 1b).

DRAM is a charge-based RAM that requires a certain cell capacitance value (~10 fF/cell) to secure the minimum voltage difference detectable by the sense amplifier, regardless of cell size. The ever-shrinking dimension of the capacitor in DRAM cells will eventually result in failure to meet this cell capacitance requirement. Hence, advancing capacitor technology is essential for continued scaling of DRAM. The scaling of the DRAM cells also raises problems in the access transistor. Without major innovations in structure, materials, and processing, scaling of DRAM will end soon.

Transistor technology in DRAM

Unlike the transistor in performance-oriented logic devices, the access transistor in DRAM requires a high ON/OFF current ratio (~10^8) to prevent substantial loss of the charges stored in the capacitor and to write the data within a short time (less than a few tens of a nanosecond). As the DRAM cell shrinks, obtaining sufficient data retention time becomes more challenging. The increase in the channel doping concentration with scaling of the feature size results in increased electrical field and junction leakage current. A simple and effective way

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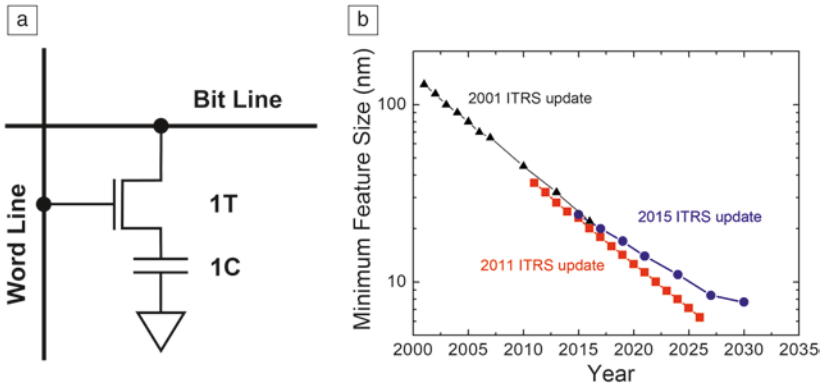

Figure 1. (a) Structure of a 1-transistor-1-capacitor (1T-1C) dynamic random-access memory (DRAM) cell. (b) Timing of DRAM technology nodes reported in the International Technology Roadmap for Semiconductors (ITRS).[1]

to overcome this detrimental short-channel effect is to increase the channel length. Three-dimensional (3D) structured transistors such as recess-channel-array transistors (RCATs) have been used to increase the effective channel length in this restricted dimension (**Figure 2**a).[3] Further increase in the channel length has been achieved by using modified RCAT structures such as sphere-shaped RCAT[4] and U-shaped RCAT[5] (Figure 2a). Below a technology node of ~50 nm, saddle-fin transistors, which combine fin-shaped field-effect transistor with a RCAT, have been utilized to obtain superior current-driving capability and sufficient data retention time.[6,7]

An 8 F^2 (where F is the minimum feature size) cell design architecture with a folded bit-line structure[8] has been traditionally used in DRAM because of reliable operations for the cell architecture. However, the demand for further scaling of the DRAM cell (< ~80-nm technology node) has resulted in conversion from 8 F^2 to 6 F^2 cell design architecture with an open bit line, because the 6 F^2 design provides a 25% improvement in DRAM cell area. However, the open bit-line architecture is vulnerable to array noise because of the high bit-line capacitance. A buried word line (Figure 2a), which is placed below the Si surface, is currently used to relieve this noise vulnerability.[9] A new 4 F^2 cell architecture—the most compact cell structure (Figure 2b) with a vertical pillar transistor—has also been proposed to facilitate further DRAM cell scaling.[10] The shift of cell architecture from 6 F^2 to 4 F^2 results in a 33% cell-area reduction. In the 4 F^2 cell design, the transistor and capacitor lie at every crosspoint of the word lines and bit lines. The vertical pillar transistor is placed on the buried bit line and beneath the storage node (Figure 2b). This cell design is highly favorable to lower the bit-line capacitance, due to the distinct arrangement of the buried bit line, aside from the capacitor. However, transiting from 6 F^2 to 4 F^2 DRAM cell design is still challenging. For further scaling of DRAM cells, severe technological challenges such as the floating body effect of the channel in the vertical transistor (the channel in the vertical transistor is isolated from the Si substrate), structural vulnerability of the pillar channel, and high resistance of the bit line remain.

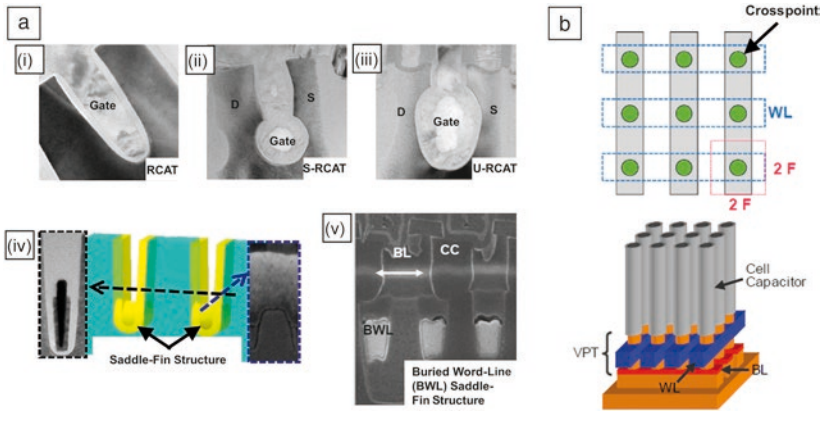

Figure 2. (a) Channel structure evolution of the cell transistor in dynamic random-access memory.[4,5,7,9] Transmission electron microscope (TEM) images of (i) RCAT, (ii) S-RCAT, and (iii) U-RCAT. (iv) (Middle) Schematic of a saddle-fin transistor with TEM cross-section images of the (left) *x*- and (right) *y*-axes of the transistor. (v) Cross-sectional image of a buried word line with a saddle-fin channel configuration. (b) (Upper) Layout of a 4 F^2 cell and (lower) schematic of a 4 F^2 cell with vertical pillar transistor.[10] Note: F, minimum feature size; RCAT, recess-channel-array transistor; S-RCAT, sphere-shaped RCAT; U-RCAT, U-shaped RCAT; D, drain; S, source; BL, bit line; CC, cell capacitor; WL, word line; VPT, vertical pillar transistor.

Capacitor technology in DRAM

For successful DRAM cell operation, the capacitor in the DRAM cell should meet two requirements—sufficient capacitance (~10 fF/cell) and ultralow leakage current ($J_g < 10^{-7}$ A/cm^2 at the operating voltage) irrespective of the cell size. The cell capacitance is expressed by:

$$C = \varepsilon_0 k \frac{A}{t_{phys}}, \quad (1)$$

where C, ε_0, k, A, and t_{phys} are the capacitance, vacuum permittivity, dielectric constant, effective capacitor area, and the physical thickness of the dielectric layer, respectively. Scaling of the DRAM cell has continuously reduced the area allocated to the capacitor in the cell, such that a 3D structured capacitor is used to obtain the necessary capacitance in the limited area, as shown in **Figure 3**a.[11] The aspect ratio of the capacitor has sharply increased and will reach ~100 shortly because of the aggressive scaling of DRAM. However, further increase in the aspect ratio is impossible because of the structural vulnerability of the storage node.

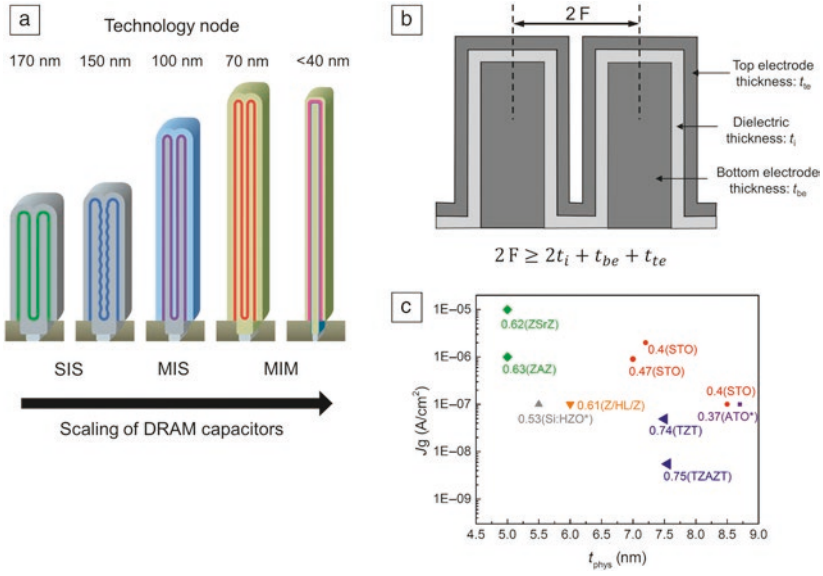

Figure 3. (a) Summary of dynamic random-access memory (DRAM) capacitor technology evolution.[11] (b) Schematic of pillar-type capacitors. (c) J_g at ±1 V as a function t_{phys} and *EOT* (nm) values for $SrTiO_3$ (denoted STO) (●),[17,48] and nanolaminates: $TiO_2/ZrO_2/TiO_2$ (denoted TZT) and $TiO_2/ZrO_2/Al_2O_3/ZrO_2/TiO_2$ (denoted (TZAZT) (◀),[49] ZrO_2/HfLaO/ZrO_2 (denoted Z/HL/Z)(▼)[50] and ZrO_2/SrO(or Al_2O_3)/ZrO_2 (ZSrZ or ZAZ) (◆).[20] In the case of ATO(■)[41] and Si:HZO(▲)[51] (Si doped $Zr_{60}Hf_{40}$ oxide), J_g is reported at 0.8 V. ZrO_2-based dielectrics remain the most promising path toward the envisaged *EOT*-J_g values at ≤5 nm t_{phys}. Note: SIS, silicon–insulator–silicon; MIS, metal–insulator–silicon; MIM, metal–insulator–metal; ATO, Al-doped TiO_2; J_g, leakage current; t_{phys}, physical thickness of the dielectric layer; *EOT*, equivalent oxide thickness; F, minimum feature size.

Thinning of the dielectric layer is also not an eventual solution to acquire large capacitance as the electric field applied to the dielectric increases with decreasing t_{phys}, which leads to a significant rise in the J_g.

Therefore, a higher-*k* material must be used as the dielectric in the DRAM capacitor. The t_{phys} value can be increased to some extent owing to the high-*k* value, reducing the effective electric field at the operating voltage. The figure of merit used by DRAM capacitor technology is the electrical performance of the dielectric material as compared to SiO_2, known as the equivalent oxide thickness (*EOT*). The *EOT* of the dielectric is given by:

$$EOT = \frac{3.9 \times t_{phys}}{k}, \quad (2)$$

where 3.9 is the dielectric constant of SiO_2. In the last decade, extensive investigations have focused on identifying high-*k* dielectrics in conjunction with specific metal electrodes to reduce the *EOT* value.[11–20]

DRAM capacitor technology is more seriously challenged than ever. Sub-20-nm DRAM technology nodes require a low *EOT* value of <0.5 nm, which is difficult to achieve. A significant challenge is the limit in t_{phys} of the dielectric and electrode layers. For >40-nm technology nodes, the lateral size of the capacitor is incomparably larger than the t_{phys} of the layers. This large technology node enables the use of cylindrical capacitors to maximize the effective capacitor area. For sub-20-nm technology nodes, however, the cylindrical structure is no longer valid and pillar capacitors are utilized because of their small feature size (F < 20–40 nm) (Figure 3a). The t_{phys} of the dielectric is stringently limited below ~5 nm, even in the pillar structure, because the sum of 2 × t_{phys}, width of the bottom electrode, and the thickness of the top electrode should not exceed 2 × F (Figure 3b). A new high-*k* material for future DRAM capacitors should achieve both ultralow J_g (10^{-7} A/cm² at the operating voltage) and a low *EOT* of <0.5 nm at a low thickness of <5 nm.

Dielectrics in DRAM capacitors

The dielectric layer should be conformally formed over the 3D capacitor structure. A better step coverage is necessary at a lower t_{phys}, because the electric field at a thinner layer can be significantly influenced by even a tiny difference in the t_{phys}. Atomic layer deposition (ALD), known to achieve exceptional step coverage, is appropriate for the growth of the dielectric layer over the 3D capacitor. In addition, ALD can grow high-quality films at a relatively low temperature. Consequently, the ALD technique has been extensively used for studies on the dielectric in DRAM capacitors.

DRAM capacitor technology has relied on the ZrO_2 dielectric for a decade as it enabled attainment of the 25-nm technology node. The trilayer structure of tetragonal (or cubic ZrO_2 ($k \approx 40$))/amorphous Al_2O_3 ($k \approx 9$)/tetragonal (or cubic ZrO_2), called ZAZ, in combination with TiN electrodes has replaced HfO_2 for the capacitors required for the ≤45-nm technology node.[21] Nevertheless, it is generally agreed that a J_g of 10^{-7} A/cm² at ±1 V cannot be maintained with the ZAZ nanolaminate stack for a sub-20-nm technology node with smaller surface areas that involves reducing t_{phys} of the dielectric.[2]

Robertson[22] showed that the *k* of oxides tends to vary inversely with the bandgap, which limits the choice of high-*k* oxides to several candidates comprising TiO_2 and $SrTiO_3$. Their bandgap is rather small (3.2–3.3 eV); however, their *k* values are more than 100. Although the allowable cation nonstoichiometry range of bulk $SrTiO_3$ is narrow and off-stoichiometric $SrTiO_3$ thin films usually show decreased *k* value, its perovskite structure could be maintained in a reasonable range of Sr:Ti ratios around stoichiometric $SrTiO_3$.[14,23] Significant efforts have been devoted to the development of $SrTiO_3$[14,16,17,23–33] and TiO_2[12,13,18,34,35] by ALD. High-*k* values of $SrTiO_3$ while preserving low J_g could be achieved by controlling the stoichiometry (Sr enrichment)[16,17] or the grain size.[27,30]

TiO_2 crystallizes as anatase ($k \approx 40$) or rutile ($k \approx 80$) phases. Rutile, a high-temperature phase,[36] is incompatible

with the thermal budget required in the DRAM fabrication process (<600°C). However, when grown on RuO_2 conductive oxide, rutile TiO_2 phase with similar lattice parameters crystallizes at deposition temperatures (i.e., 250°C) owing to the template effect displayed by the substrate,[12,13,37,38] thus reducing both the *EOT* and J_g.[12,15,34] Nevertheless, the scalability of t_{phys} is limited to 10–12 nm. Doping TiO_2 with Al[11,39–42] could further reduce J_g, leading to further reduction in t_{phys} to ~7 nm.[39,41]

A doping approach could also be considered for other dielectrics (e.g., HfO_2 and ZrO_2). Dopants with lower electronegativities and larger ionic radii than those corresponding to the host oxide led to higher-*k* and a reduction of J_g for HfO_2[43–45] and ZrO_2.[46,47] Higher symmetry phases are formed via doping (such as tetragonal or cubic) leading to larger *k*, while the lower J_g was attributed to the shift of the charge states of the oxygen vacancies into the conduction bands.[47]

As previously described, continued downscaling of DRAM technology toward the sub-20-nm technology node will require a low t_{phys} of ≤5 nm. At such a low thickness, other characteristics of the capacitors become important, including electrode and dielectric surface roughness, lattice mismatch, and chemical compatibility of electrode/dielectric. A summary of the lowest $EOT - J_g - t_{phys}$ at ±1 V for ALD dielectrics is given in Figure 3c.[17,20,41,48–51] This shows that the nanolaminates' approach combining a high bandgap with a high-*k* dielectric leads to the lowest J_g when thinning the dielectric. However, for $t_{phys} \leq 5$ nm, the nanolaminate approach is less likely to be an option because of intermixing of the layers under the thermal budget applied to the capacitor.

Comprehensive *ab initio* calculations of the bandgap and *k*[52] (namely the generalized gradient approximation for bandgap and local density approximation for *k*) showed that cubic BeO can display the highest-*k* (~300) and bandgap values (>9 eV). However, the cubic rock-salt structure of BeO is a high-pressure phase; therefore, stabilization under ambient conditions is required. Efforts are being devoted to depositing a high-bandgap BeO by ALD;[53] however, no high-*k* material has yet been achieved.

Electrodes in DRAM capacitor

Further reduction in J_g can also be attained by electrode engineering. The electrode in a DRAM capacitor should have a high work function and a sharp interface between the electrode and dielectric for better dielectric performance. TiN, grown by ALD using $TiCl_4$ and NH_3, currently functions as the electrode in DRAM capacitors. However, the work function of TiN is insufficient to suppress J_g at the thin dielectric thickness required in the ~10-nm technology node. Therefore, much effort has also been devoted to developing new electrodes, including noble metal and conducting oxide electrodes. Among noble metals, ruthenium (Ru) is considered the most promising for DRAM capacitor electrodes. Ru is favorable for suppressing J_g because of its relatively high work function (~4.8 eV), and the ease with which Ru can be dry etched is also advantageous for patterning the electrodes. The use of Ru as the electrode has shown possibilities of lowering J_g.[54–56] Forming a continuous and smooth Ru layer on oxides at a low Ru thickness of <5 nm is difficult because of its high surface energy. Morphological issues such as blisters, which often occur on ALD Ru on oxides, must also be addressed for electrode application of Ru.[57]

Conducting oxides such as RuO_2 and $SrRuO_3$ have also attracted attention as potential electrodes. The work function of RuO_2 and $SrRuO_3$ is even higher than that of Ru, which is favorable for low J_g. In particular, the structural coherency with promising high-*k* materials (e.g., rutile TiO_2/RuO_2[13,58,59] and $SrTiO_3/SrRuO_3$[60,61]) provides concurrent decreases in *EOT* and J_g. However, these conducting oxides have not yet been practically used in DRAM capacitors. Those Ru-containing oxides are easily reduced during the back-end process, because of the weak bonding between ruthenium and oxygen. Ta-doped SnO_2 has recently been suggested as a reduction-resistant oxide electrode for DRAM capacitors.[62] Capacitors composed of rutile TiO_2/Ta-doped SnO_2 stack showed both excellent dielectric properties and thermal stability in experiments.

Summary and outlook

DRAM is the representative memory used in modern computers, but it appears to be facing serious challenges for further scaling toward the ~10-nm technology node. Much effort has been dedicated to prolonging its scaling. Structural modification of cell transistors has been attempted to suppress J_g and lower the bit-line capacitance. Transition of the cell architecture to 4 F^2 has also been suggested for further DRAM scaling. To satisfy the stringent requirements of capacitors in ~10-nm technology nodes, new higher-*k* dielectrics and electrodes have been extensively investigated. Although high-*k* oxides such as TiO_2 and $SrTiO_3$ show potential for further scaling of DRAM, their large J_g has to be resolved at a low thickness of <5 nm. A new dielectric material with both large bandgap (over ~5 eV) and large *k* (>50) should be designed for the ~10-nm technology node. Otherwise, downscaling of DRAM might end at approximately the 15-nm technology node.

Although the scaling of DRAM will eventually end, DRAM might maintain its status as the main memory for a long time. The market for infrastructure such as servers, storage, and networking continues to grow rapidly. Bandwidth is the major challenge of DRAM for those applications. Although die stacking with conventional wire bonding has limited data-transfer rates, the emergence of high-bandwidth memory (HBM) through-silicon-via technology shows great promise with much improved data rates and reduced power consumption. Die stacking of DRAM in the form of HBM could be the future of this long-standing main memory, following the end of DRAM scaling.

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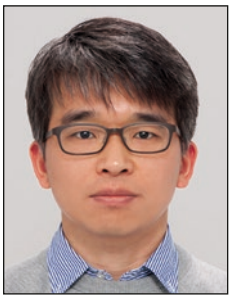

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