

Hardware/Software co-design with ADC-Less In-memory Computing Hardware for Spiking Neural Networks

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Abstract—Spiking Neural Networks (SNNs) are bio-plausible models that hold great potential for realizing energy-efficient implementations of sequential tasks on resource-constrained edge devices. However, commercial edge platforms based on standard GPUs are not optimized to deploy SNNs, resulting in high energy and latency. While analog In-Memory Computing (IMC) platforms can serve as energy-efficient inference engines, they are accursed by the immense energy, latency, and area requirements of high-precision ADCs (HP-ADC), overshadowing the benefits of in-memory computations. We propose a hardware/software co-design methodology to deploy SNNs into an ADC-Less IMC architecture using sense-amplifiers as 1-bit ADCs replacing conventional HP-ADCs and alleviating the above issues. Our proposed framework incurs minimal accuracy degradation by performing hardware-aware training and is able to scale beyond simple image classification tasks to more complex sequential regression tasks. Experiments on complex tasks of optical flow estimation and gesture recognition show that progressively increasing the hardware awareness during SNN training allows the model to adapt and learn the errors due to the non-idealities associated with ADC-Less IMC. Also, the proposed ADC-Less IMC offers significant energy and latency improvements, $2 - 7 \times$ and $8.9 - 24.6 \times$, respectively, depending on the SNN model and the workload, compared to HP-ADC IMC.

Index Terms—ADC-Less, In-memory Computing, Spiking Neural Networks, HW/SW co-design.

1 INTRODUCTION

PROGRESS in deep learning has allowed outstanding results in many cognitive tasks, albeit at the cost of increased model size and complexity [1], [2]. Although such models are suitable for cloud-based systems with vast computational resources, they are not ideal for real-time edge applications, like autonomous drone navigation, where both low energy consumption and latency are crucial. In recent years, Spiking Neural Networks (SNNs) have emerged as bio-plausible alternative to standard deep learning leading to energy-efficient models for sequential tasks. Their intrinsic features, such as inherent recurrence via membrane potential accumulation, sparsity, binary activations, event-based and spatio-temporal processing make them suitable for edge implementations. A considerable amount of work has been done on training deep SNNs for image classification tasks, achieving accuracy comparable to those obtained by conventional Artificial Neural Networks (ANNs) [3], [4], [5]. While image classification only demands spatial processing, SNNs also offer temporal processing capabilities, thanks to the inherent recurrence due to their membrane potential that serves as a memory. Recent research has shown that SNNs can handle sequential tasks with performance at par with complex Gated Recurrent Unit (GRU) and Long Short-Term Memory (LSTM) based models with much lesser

parameters [6], [7], [8]. We believe that sequential tasks, such as gesture recognition and event-based optical flow estimation are examples where all features of SNNs can be exploited to achieve better efficiency than the corresponding ANN implementations [9], [10].

SNN deployment into existing commercial GPU-based edge hardware platforms are highly inefficient. This originates from present day Graphical Processing Units (GPUs) lacking the ability to seamlessly process binary, sparse, and spatio-temporal inputs [11]. This has triggered the interest in domain-specific accelerators that can fully extract the benefits of SNNs [7], [12], [13]. Among the alternatives, In-Memory Computing (IMC) architectures turn out to be promising inference engines for deploying SNN models at a lower energy overhead and latency. This is possible because IMC architectures perform matrix-vector multiplications (MVM) within the memory crossbar arrays with a very high efficiency [14], [15]. Nevertheless, in conventional IMC architectures, the efficiency of MVMs is overshadowed by the high energy consumption of peripheral circuits used as interfaces between the analog and digital portions of the system. Specifically, High-Precision ADCs (HP-ADC) consume more than 60% of the total system energy and occupy more than 81% of the chip area, representing the major bottleneck in IMC architectures [14], [15], [16].

There have been several proposals to overcome the limitations imposed by HP-ADCs in IMC architectures. Some have focused on reducing ADC precision while compensating for accuracy degradation by changing IMC structures and splitting MVM operands [17], [18]. Later works focused on quantization-aware approaches to further reduce

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the ADC precision down to 1-bit [19], [20], [21]. Most of the above approaches focused on hardware optimization, either through performing fully analog operations or optimizing the design of ADCs [22], [23] and focused only on ANNs for image classification tasks on simple datasets like MNIST and CIFAR10. In this work, we propose a hardware/software co-design methodology to deploy SNNs into an ADC-Less IMC architecture by replacing HP-ADCs with sense-amplifiers as 1-bit ADCs (ADC-Less). We employ 1-bit partial sum quantization for the sense amplifiers and propose a three-step hardware-aware training methodology to recover performance degradation.

We performed experiments on image classification datasets such as CIFAR10 and CIFAR100 and on more complex vision tasks such as gesture recognition on the DVS128 gesture dataset [24], and optical flow estimation on the MVSEC dataset [25]. Our models demonstrate competitive application accuracy for all the tasks while achieving significant energy and latency improvements compared to HP-ADC IMC architectures and commercial GPU-based platforms, respectively.

The main contributions of the work can be summarized as follows.

- An ADC-Less in-memory computing architecture for spiking neural networks with very low latency and energy consumption.
- An end-to-end hardware-aware training methodology for SNNs that compensates for the proposed architecture's quantization error (weights and binary partial sums).
- Experiments validating that the proposed HW/SW co-design method is suitable for deploying spiking neural networks for tasks beyond image classification, such as optical flow estimation and gesture recognition.
- Generalization of the proposed scheme for different network architectures, such as plain CNNs, ResNets, and U-Net architectures.

2 BACKGROUND

To bring energy-efficient machine intelligence to the edge, it is imperative that we effectively co-design the network and hardware architectures. In this section, we describe the SNN dynamics and the IMC hardware used to implement corresponding SNNs.

2.1 Spiking Neural Networks

Among all the spiking models, the leaky-integrate-and-fire (LIF) neuron model is one of the simplest ones that retain the main features of biological neurons with binary activation (spikes). The LIF model can be described as follows:

$$U_{mem}[t] = \lambda U_{mem}[t-1] + \sum_j W_j X_j[t] - R[t-1] \quad (1)$$

$$A_s[t] = \Theta(U_{mem}[t] - V_{th}) \quad (2)$$

$$R[t] = \begin{cases} \lambda U_{mem}[t] A_s[t] & , \text{hard reset} \\ V_{th} A_s[t] & , \text{soft reset} \end{cases} \quad (3)$$

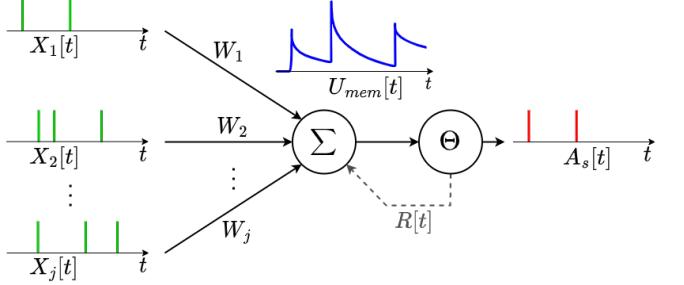


Fig. 1. Dynamics of a LIF spiking neuron where the membrane potential, U_{mem} , integrates the incoming spikes, X_j , modulated by the weights, W_j , and leaks with a time constant, λ . When U_{mem} reaches a threshold, V_{th} , the neuron fires generating an output spike, A_s . After the neuron fires, the membrane potential is reset.

Where Θ is the Heaviside function, and $R[t]$ is a reset mechanism triggered when the neuron fires. For $R[t]$, there are two options: a hard reset and a soft reset. The former sets $U_{mem}[t]$ to zero, while the latter reduces $U_{mem}[t]$ by a value equal to V_{th} .

A visual representation of the spiking neural dynamics is shown in Fig. 1. The membrane potential accumulates inputs over time, where the inputs, $X_j[t]$, are multi-time-step binary spikes. The inherent recurrence of spiking models is due to membrane potential, U_{mem} , the hidden state evolving over time that can be described as short-term memory. Similarly, the leak parameter, λ , introduces a forgetting mechanism, similar in function to that of a "forget gate" in an LSTM model [8]. These features enable SNNs to efficiently handle sequential tasks.

2.2 Crossbar-based In-memory Computing

In-memory computing (IMC) can be used to perform analog matrix-vector multiplication (MVM) operations with high energy efficiency. The memory elements can be placed in a crossbar array, as shown in Fig. 2. This configuration takes advantage of Kirchhoff's law to perform multiplication and accumulation (MAC) operations. The voltage (V_i) on the input rows, also called wordlines, is multiplied by the conductances (G_{ij}) of the memory elements and accumulated on the current output ($I_1 = \sum G_{i1} V_1$) of each column, called bitline. This operation resembles the MAC operations performed by a neural network (NN), where the voltages are the NN's inputs, conductances are the weights of the NN, and the bitline current corresponds to the MVM operation output. For a SNN, the inputs are multi-time-step binary spikes (1/0). SNN execution on IMC hardware involves MVM operation between the weight matrix and the binary input vector repeated for each time-step. During each time step, MVM operation output is accumulated with the membrane potential and passed on to the neuron unit for application of activation function (LIF).

In order to map an SNN model into an IMC crossbar, the model parameters need to be quantized. Hence, the weights must have a finite resolution: number of bits per weight (nbW). The number of memory cells used to represent the weights is determined by the bit-slicing weight resolution (sbW), which is equal to the bit-cell resolution of the memory elements (note, memory elements can be multi-bit mem-

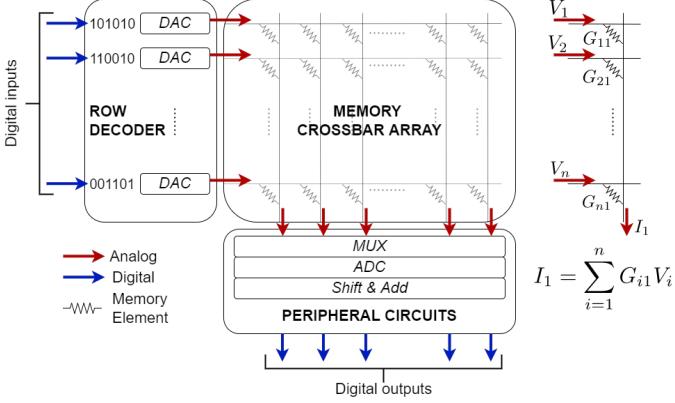


Fig. 2. General scheme of a conventional crossbar-based analog MVM accelerator, showing the peripheral circuits.

ories such as ReRAMs or PCRAMs, or single-bit such as SRAMs). Hence, the number of memory elements used per weight value is nbw/sbw . The binary input activations in SNNs are applied through a 1-bit digital-to-analog converter (DAC). At a particular timestep, multiple wordline are activated for matrix vector multiplication, which manifests itself as a current developed over the bitline. The bitline current is passed through a multiplexer (MUX) connected to an analog-digital converter (ADC) which converts the analog current into a digital value. The multiplexer allows multiple bitlines to share the same ADC since it is impractical to have one high-precision ADC per bitline due to its large area. Ideally, the ADC requires a precision equal to $\log_2(N_{WL}) + sbw - 1$ where N_{WL} is the number of wordlines used - typically equal to the crossbar size ($xbar$). Finally, the digitized values are shifted and added according to their MSB and LSB (most and least significant bits) positions. The number of shifted operations is proportional to (nbw/sbw) .

For a deep SNN, the size of layer weights is too large to be mapped into a single crossbar. Hence, it has to be split into multiple crossbar arrays, with each array producing a partial-sum (PS) that is accumulated to get the final activation value for the layer. Here, the ADC's resolution determines the accuracy of the PS. Therefore, a high-precision ADC (HP-ADC) is required. However, HP-ADCs are expensive, both in terms of the chip area, and energy consumption [14], [16]. Therefore, to optimize area, the ADC units have to be shared among multiple columns of the crossbar, which adds extra latency to the total operation of the crossbars. It is clear that the cost of the ADCs overshadow the potential benefits of employing crossbars to perform fast and energy-efficient MVMs. [15], [26].

In the above sections, we discussed a general crossbar-based IMC, independent of the memory technology. Note, however, both CMOS and non-volatile technologies can be used as memory elements for the crossbar array. For the rest of the paper, we employ ReRAM as an example technology to show the effectiveness of our approach.

3 RELATED WORKS

Past works such as [14], [15], [16], [17], [18], [19], [20], [21], [22], [26] identify ADCs as the principal bottleneck towards

fully leveraging the energy efficiency of crossbar-based IMC architectures. In [17], the authors proposed an offline methodology to manually adjust the weight distribution of different crossbars to achieve a 1-bit partial sum using a thresholding operation, which is then merged to generate a 1-bit output to be fed into the next layer. They were able to eliminate both ADC and DAC modules without a significant accuracy drop. However, their methodology was impractical for deeper networks, as the method's complexity and errors increase as the network becomes larger.

The authors in [18] proposed an input-splitting scheme to represent a large neural network as multiple smaller models. This allowed for a reduction of the ADC precision from 8-bits to 4-bits without a significant accuracy drop. However, as shown in [15], a 4-bit ADC still consumes too much energy and area compared to crossbar arrays.

Authors in [19] proposed an iterative quantization-aware training method to partially overcome some of the hardware limitations imposed by the ReRAM-based IMC accelerators. The method involves quantizing the inputs and weights to a fixed resolution and then retraining the model considering the features of the crossbar architecture, and finally introducing the effects of the ADC resolution in the partial sum. Based on this approach [19] reduces the precision of the ADC while the neural model partially compensates for the loss of accuracy. However, for ADC resolution below 4-bit, this method suffers from severe accuracy degradation.

On the other hand, authors in [20] explored quantization-aware training on binary ResNets targeting IMC architectures with low ADC precision. Their approach resulted in small accuracy drop when using 1-bit ADCs when merging the partial sum followed by a batch normalization layer. Nevertheless their approach was limited to binary ResNet architectures, which are still challenging to train with high accuracy. On a similar line, researchers in [21] proposed a hardware-software co-design approach to eliminate the ADC modules by using only the sense-amplifier (SA) modules as 1-bit ADC and mitigate the accuracy loss using a quantization-aware training. However, this method introduced additional parameters to scale the binary partial-sum to increase the representation ability of the partial sums. Also, [22] proposed a fully analog IMC macro to compute MVM without using ADCs by encoding the inputs as pulse-width modulated (PWM) signals. The main constraint being that the ANN models were limited by the crossbar size and were restricted to only 2-bit weights. Note, it required contiguous layers to be mapped into contiguous arrays in hardware, limiting the chip architecture.

All the works discussed above were intended for only ANN models and were evaluated on image classification tasks for datasets like MNIST and CIFAR10. Our work aims to extend the application to SNN models and scale to complex sequential regression tasks while being energy efficient.

4 ADC-LESS IMC ARCHITECTURE

In this section, we describe the proposed ADC-Less IMC architecture which does not suffer from the performance bottleneck posed by ADCs in conventional IMC hardware

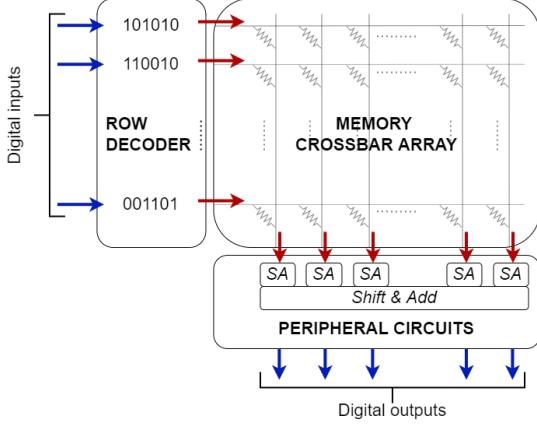


Fig. 3. Proposed scheme of the ADC-Less crossbar-based analog MVM for spiking neural networks.

design. The general scheme of the ADC-Less IMC architecture is shown in Fig. 3. In contrast to conventional IMC (Fig. 2), our ADC-Less IMC uses sense amplifier (SA) circuits at each bitline instead of a large high-precision ADC.

4.1 Binary partial sum quantization

As described in Section 2.2, the bitline current of the crossbars represent the Partial Sum (PS) of an MVM operation. The PS is digitized by using an ADC, and the resolution of the ADC determines the dynamic range of PS (PS quantization). For an SNN, mapped into a crossbar using binary memory cells ($sb_w = 1$), the ideal dynamic range required for the PS is equal to $\log_2(N_{WL})$. However, for the ADC-Less IMC, we use SA as 1-bit ADC, which produces binary PS. This drastic reduction in the PS quantization is compensated by adapting a quantization aware training of SNN, as discussed later in Section 5.

4.2 Weight mapping

We evaluate two schemes to map positive and negative 4-bit weights into binary memory-cell arrays.

The first mapping scheme is shown in Fig. 4a, where both positive and negative weights are mapped into the same column using two rows. The positive weights are mapped into the first row using an unsigned integer representation, while the second row is set to a high resistive state (Roff). Similarly, the negative weights are mapped into the second row using an unsigned integer representation, while the first row is set to Roff. This strategy allows positive weights to charge the bitlines (BL) while negative ones to discharge them. For this mapping, the access to each row requires a pass transistor controlled by the binary input spikes.

On the other hand, the second mapping scheme, shown in Fig. 4b, uses different columns for positive and negative weights. The weights are mapped into one row using two consecutive 4-bit columns; the positive values are mapped into the first column, while the successive columns are set to Roff. Similarly, the negative values are mapped in the second column, while the first is set to Roff. In contrast to the first mapping scheme, the crossbar's wordlines can be accessed without additional circuitry.

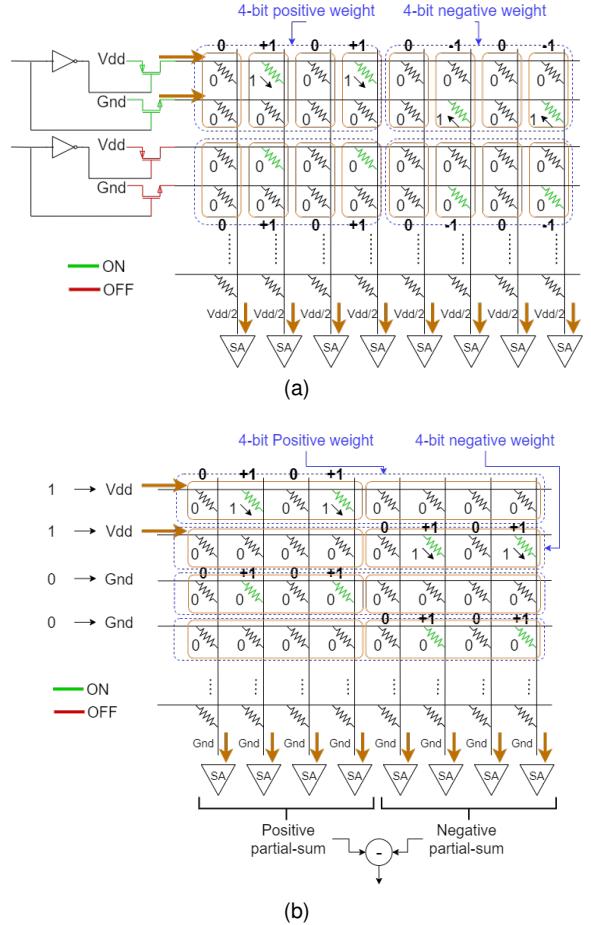


Fig. 4. Two proposed weight mapping schemes (a) positive and negative weights sharing the same column with weights mapped in two rows, and (b) positive and negative weights in different columns with weights mapped in two columns.

The first mapping scheme quantizes the partial sum into ± 1 values for each column. In contrast, the second mapping scheme quantizes the partial sum for the positive and negative columns into 0 and 1 values that must be subtracted.

4.3 Digital LIF Neuron Module

In addition to the ADC-Less IMC described in the previous section, we designed a digital module to perform the neural dynamics of the LIF model described in Section 2.1. Each LIF module implements an individual neuron that accumulates the partial sum of multiple crossbars to a membrane potential (U_{mem}), storing it in a register, as described in (1). In parallel, the additional circuits in the module monitor if the value of U_{mem} is close to the threshold value (V_{th}) to fire an output spike, (2), or start the reset mechanism, (3). The module is implemented so that each time step of the LIF model corresponds to one clock cycle of the proposed architecture.

4.4 SNN inference with ADC-Less IMC

During inference, the first layer of an SNN model receives an input sequence of frames, whose length (time-steps) depends on the workload (5 for optical flow, 10 for image

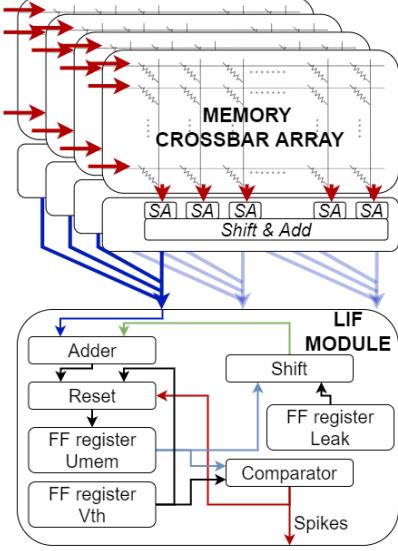


Fig. 5. Multiple crossbars producing a partial-sum, and the Digital LIF neuron module for accumulation and spike generation.

classification, and 20 for gesture recognition). The output of this layer is a sequence of binary spikes with the same number of time-steps that pass through the rest of the model. In the following layers, the spikes are applied to the wordlines of the crossbars in a sequential manner, one spike at a time. After the bitline current output is digitized according to the selected mapping scheme, described in Section 4.2, the binary partial sum is shifted and accumulated appropriately. The partial sums from multiple crossbar arrays are added together and accumulated into the U_{mem} register, as described in Section 4.3. Finally, the LIF module produces an output sequence of binary activation spikes for the next layer.

5 HARDWARE-AWARE TRAINING

The proposed ADC-Less architecture imposes some hardware constraints such as weight quantization (4-bit, $nb_w = 4$), memory cell resolution (1-bit per cell, $sb_w = 1$), and partial sum quantization (1-bit). These features lead to a deviation from the ideal full-precision operation producing significant accuracy loss when a spiking model is deployed naively into the proposed architecture.

Thus, we propose a three-step hardware-aware training to compensate for the deviation from an ideal inference. The three-step method is shown in Fig. 6, where the models are trained consecutively, increasing the hardware awareness in each step. First, the method involves full-precision training using ANN-to-SNN conversion [4] or surrogate gradients [27] for the spiking models. In the second step, the model is re-trained using quantization-aware training with uniform 4-bit quantization. Finally, in the third step, the denominated “ADC-Less training” fine-tunes the quantized model by exposing it to the weight mapping scheme, the memory cell resolution, and the binary partial-sum quantization.

5.1 Full Precision Training

The first step of the proposed hardware-aware method begins with training a full-precision SNN model that would

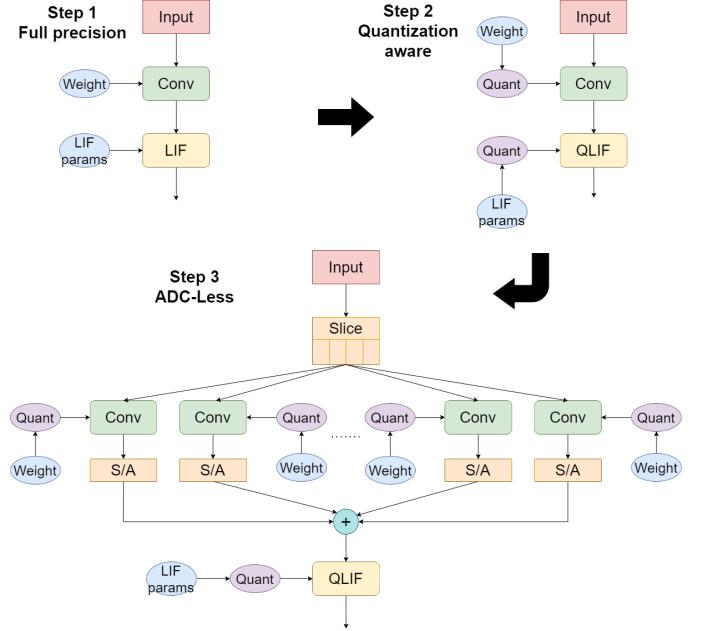


Fig. 6. The hardware-aware training methodology proposed is based on three consecutive training steps where the model resulting from the previous step is used as initialization for the next one.

be used as model initialization for the next step. For this purpose, we used two training approaches.

The first approach is based on ANN-to-SNN conversion followed by fine-tuning of the leak and threshold parameters as proposed in [4], which has proven to be effective in training deep SNNs for image classification tasks with just a few time-steps. During the ANN-to-SNN conversion phase, the weights are copied to the SNN model. At the same time, the threshold parameters (V_{th}) are set to the maximum activation value achieved during forward pass at each layer. This ensures that the spikes propagate through the entire mode without vanishing. Then, the leak (λ) and V_{th} parameters are fine-tuned to achieve better accuracy.

The second approach uses surrogate gradients [27] to train the model from scratch. One advantage of this approach is that it can be used for image classification and more complex sequential tasks, such as gesture recognition and optical flow estimation, where ANN-to-SNN conversion is unsuitable. The surrogate gradient method approximates the derivative of the Heaviside function used by the LIF model during the backward pass of the training.

5.2 Quantization-aware Training

During this step, we quantize the weights, LIF neuron membrane potential, the neuron threshold, and the leak to integer values to match hardware precision during inference. The model is initialized from the previous step and we perform quantization aware training to fine tune the model to integer only data structures. Our quantization scheme is designed to operate with SNNs, and it is based on [28]. The weights of convolutional and linear layers are symmetrically quantized to 4-bits, so the weights (W) are separated into quantized weights (W_q) and a scale factor (S_W), as shown in Fig. 7.

The main difference from [28] is that we take advantage of the binary spikes to avoid an additional quantization of

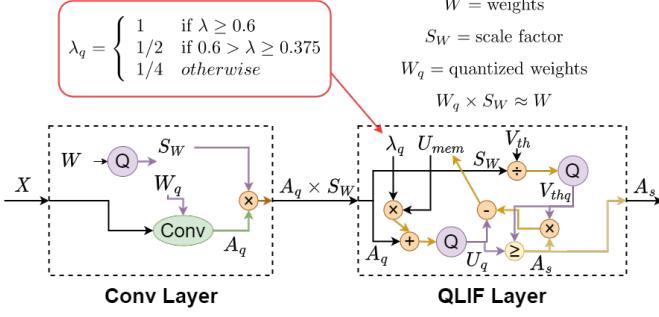


Fig. 7. Quantization scheme for convolutional and LIF layers.

activations. This reduces additional computations and error associated with activation quantization. Moreover, in [28], the weights and activation of one layer are scaled based on its local parameters and the scale factors of previous layers. In contrast, we scale weights using only local parameters of that layer, so each layer is independently quantized.

As part of the quantization-aware training, the neural dynamics of the LIF model were quantized to match precisely with the operation of the LIF module described in Section 4.3. Parameters, such as membrane potential and threshold, were scaled using the S_W of the previous layer and quantized with 12 bits. In contrast, the leak parameter was quantized to powers of 2 (2^{-n}), with $n \in [0, 2]$, so that it could be implemented as a shift operation in hardware. The quantization process is shown in Fig. 7.

To avoid zero gradients produced by quantization operations, we use surrogate gradients to approximate the full precision gradient during the backward pass, in the same way as [28].

5.3 ADC-Less Training

After the quantization-aware training, the model was fine-tuned, considering the weight mapping scheme (nbW weight bit resolution and sbW bit slicing), the crossbar array size ($xbar$), and the partial-sum quantization.

Here, the conventional convolution operation (Conv), used in the quantization scheme shown in Fig. 7, was replaced with the ADC-Less convolution described in Fig. 8. This new convolution was implemented by binarizing the weights and splitting the input channel dimension of the kernel into a certain number of groups computed according to the $xbar$ and kernel sizes. The split kernel is used to perform a grouped convolution over the spike inputs (X), to obtain PSs. The PSs are then quantized according to the weight mapping scheme, producing binary PS that are then shifted and added properly. Finally, the PSs are accumulated into the final activation (A_q) which goes to the input of the QLIF layer to perform the spiking dynamics.

We also use surrogate gradients to avoid the vanishing gradient problem due to the kernel slicing and binary partial sum. The gradient is masked with the binary bits mapped into the crossbar arrays for the slicing. And for the binary partial sum, the gradient is approximated by $g(x) = \frac{1}{1+\alpha x^2}$.

6 SNN MODELS

This section describes four SNN models used in our experiments (two for image classification, one for gesture

Input: $W_q, X, xbar, nbW = 4, sbW = 1$

Output: A_q

```

1:  $in\_ch \leftarrow W_q.shape()[1]$  {input channels}
2:  $k_H, k_W \leftarrow W_q.shape()[2 :]$  {kernel size}
3:  $n\_groups \leftarrow ceil(\frac{in\_ch \times k_H \times k_W}{xbar})$ 
4: while  $in\_ch \% n\_groups == 0$  do
5:    $n\_groups \leftarrow n\_groups + 1$ 
6: end while
7:  $W_{pos-q,nbW} \leftarrow \text{binarize}(\text{relu}(W_q), nbW, sbW)$ 
8:  $W_{neg-q,nbW} \leftarrow \text{binarize}(\text{relu}(-W_q), nbW, sbW)$ 
   {If using the first mapping scheme}
9:  $out\_acc \leftarrow 0$ 
10:  $W_{q,nbW} \leftarrow W_{pos-q,nbW} - W_{neg-q,nbW}$ 
11: for  $i$  in range( $0, nbW/sbW$ ) do
12:    $w \leftarrow \text{cat}(\text{chunk}(W_{pos-q,i}, n\_groups, dim = 1))$ 
13:    $out \leftarrow \text{conv}(w, X, groups = n\_groups)$ 
14:    $out \leftarrow \text{adc\_less\_act}(out)$  {±1 values}
15:    $out\_acc \leftarrow out\_acc + 2^i \times out$ 
16: end for
17:  $A_{acc} \leftarrow out\_acc$ 
   {End of first mapping scheme}
   {If using the second mapping scheme}
18:  $out\_pos \leftarrow 0$ 
19: for  $i$  in range( $0, nbW/sbW$ ) do
20:    $w \leftarrow \text{cat}(\text{chunk}(W_{pos-q,i}, n\_groups, dim = 1))$ 
21:    $out \leftarrow \text{conv}(w, X, groups = n\_groups)$ 
22:    $out \leftarrow \text{adc\_less\_act}(out)$  {0, 1 values}
23:    $out\_pos \leftarrow out\_pos + 2^i \times out$ 
24: end for
25:  $out\_neg \leftarrow 0$ 
26: for  $i$  in range( $0, nbW/sbW$ ) do
27:    $w \leftarrow \text{cat}(\text{chunk}(W_{neg-q,i}, n\_groups, dim = 1))$ 
28:    $out \leftarrow \text{conv}(w, X, groups = n\_groups)$ 
29:    $out \leftarrow \text{adc\_less\_act}(out)$  {0, 1 values}
30:    $out\_neg \leftarrow out\_neg + 2^i \times out$ 
31: end for
32:  $A_{acc} \leftarrow out\_pos - out\_neg$ 
   {End of second mapping scheme}
33:  $A_{acc,g} \leftarrow \text{chunk}(A_{acc}, n\_groups, dim = 1)$ 
34:  $A_q \leftarrow 0$ 
35: for  $j$  in range( $0, n\_groups$ ) do
36:    $A_q \leftarrow A_q + A_{acc,j}$ 
37: end for
38: return  $A_q$ 

```

Fig. 8. Pseudo-code for ADC-Less convolution operation.

recognition, and one for optical flow).

As discussed earlier, this work exploits the binary activations in SNNs. For this reason, our SNN models were carefully designed to preserve the spikes at all layers during both training and inference stages. For instance, all the models use max pooling instead of average pooling since the latter destroys spikes. We modify the dropout layers to avoid the scaling factor used during training; initialize them at the beginning of a sequence, and keep them frozen until the end. The most crucial change was made to the residual layers used in three of the four SNN models. A regular residual block, as shown in Fig. 9a, merges the outputs from the direct path and skip-connection by adding both signals

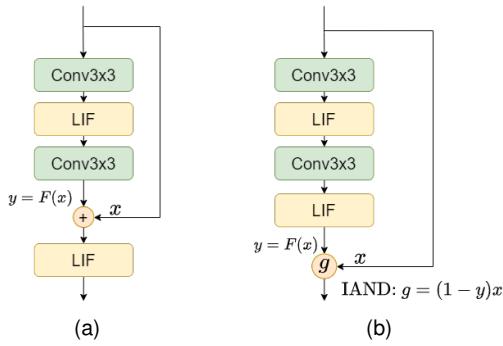


Fig. 9. Residual blocks for SNN: (a) regular residual block, and (b) IAND spike-element-wise (SEW) block.

$(x + y)$, and then recovers the spikes by using a LIF layer. This kind of block works well for full precision models using ANN-to-SNN conversion methods [4]. However, it is not compatible with our quantization-aware training scheme that aims to perform only integer-integer computations. For this reason, we adopt the IAND Spike-Element-Wise (SEW) block proposed in [5] that merges x and y signals by using a binary IAND ($g = (1 - y)x$) logical operation (Fig. 9b). This logical operation can be implemented much more efficiently on hardware compared to an adder by using just two logic gates. In addition, the SEW block has been proven to be suitable for training deep models with surrogate gradients [5].

6.1 VGG16 and ResNet20

For image classification, we use spiking VGG16 and ResNet20 models. In order to ensure that all the layers receive only binary activations, we made minor changes to both architectures. For both models, we use only max pooling layers instead of average pooling to preserve the integrity of the spikes. Moreover, for the ResNet20, we use the SEW residual block shown in Fig. 9b, to ensure that all the inputs are binary.

For quantization, we use 8-bit weights for the first and last layer with HP-ADC and 4-bits weights for the other layers with ADC-Less.

6.2 DVSNet

For gesture recognition, we designed a model called DVS-Net based on the IAND SEW blocks described earlier. The input layer is a Conv3x3 with 32 output channels, followed by five SEW blocks with 32 input channels, where each block uses a MaxPool2x2 layer at the output. The output spikes of the convolutional layers are accumulated and flattened to be classified by a final Linear128x11 layer.

For quantization, we use 4-bit weight for all the layers. The first and last layers use HP-ADC, and the other layers use ADC-Less.

6.3 Fully-spiking FlowNet (FSFN) model

For optical flow estimation, we implemented a fully-spiking model based on the hybrid SNN-ANN Spike-FlowNet [9] model. We denote our model as Fully-Spiking FlowNet

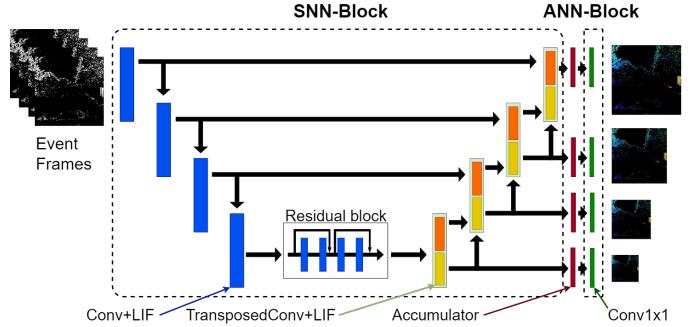


Fig. 10. Fully-Spiking FlowNet (FSFN) encoder-decoder architecture. Both encoder and decoder are spiking layers, and only the last layer used for the final estimation of the optical flow is composed of Conv1x1 layers. During the training, outputs of all four levels are used to compute loss and guide the training, but only the output with the highest resolution is used during inference time.

(FSFN). FSFN has some minor changes with respect to the original Spike-FlowNet architecture in terms of kernel size, channels, and input sizes. These changes ensure that all layers receive only binary inputs. Since optical flow is an analog quantity, we maintain the last layer as an analog Conv1x1 layer (ANN block). This layer receives the accumulated outputs produced by the SNN block as inputs, as shown in Fig. 10.

Four Conv1x1 layers compound the ANN-block with 32 channel inputs and two channel outputs. This block produces outputs at different scales that are helpful to guide the model during training, as they connect the global loss with the first layers allowing learning coarse and fine flow at multiple scales. However, only the output layer with the highest resolution is used during the inference stage.

For quantization, we use the following configuration: 8-bit weights for the first layer with HP-ADC, 4-bits weights for the rest of the SNN-Block with ADC-Less, and full precision Conv1X1 layers for the ANN-Block. We use full precision in the ANN-Block because the optical flow prediction is a continuous value requiring high precision.

7 EXPERIMENTAL RESULTS

7.1 Computational evaluation on different tasks

In this section, we evaluate the hardware-aware training discussed in Section 5 for multiple tasks such as image classification, gesture recognition, and optical flow estimation. In all the cases, we compare the ADC-Less model to a quantized model using HP-ADCs. All models were selected using cross-validation with a three-partition dataset (train, validation, and test sets).

7.1.1 Experiments on Image Classification

Although image classification is not the most suitable computer vision task for SNNs, it helps to set a baseline for comparing our work with other proposals focused on ANNs. As discussed in Section 3, most previous works tested their proposed schemes on MNIST and CIFAR10. However, the MNIST dataset is a simple image classification task, so we only focus on CIFAR10 dataset and extend our results to CIFAR100 dataset. For both datasets, we use the following

TABLE 1
Test accuracy of spiking models for image classification on CIFAR10 and CIFAR100

Metrics	FP	HP-ADC	ADC-Less		
			32	64	128
CIFAR10 (VGG16)					
Acc@1	88.89	91.93	90.70	90.44	89.52
Gap	-	-	-1.23	-1.49	-2.41
CIFAR10 (ResNet20)					
Acc@1	89.97	90.12	88.96	88.46	87.70
Gap	-	-	-1.16	-1.66	-2.42
CIFAR100 (VGG16)					
Acc@1	66.39	68.71	68.48	67.11	66.93
Gap	-	-	-0.23	-1.6	-1.78

distribution: 50k images for training, 5k for validation, and 5k for testing.

Here, we evaluate the hardware-aware training on the two SNN models discussed in Section 6.1. The full-precision (FP) VGG16 was trained based on an ANN-SNN conversion + fine-tuning scheme [4] with 5 time-steps, while FP ResNet20 was trained from scratch using surrogate gradients with 10 time-steps.

After the FP training, we proceed with the quantization-aware training followed by the ADC-Less training. In both cases, the models were trained using 10 time-steps. The accuracy values obtained for the test set are shown in Table 1. We can see that quantization-aware training improves the accuracy of the models in all cases because quantization has a regularization effect that supports SNN learning. Then, for the ADC-Less aware training, we used the second mapping scheme, shown in Fig. 4b.

Table 1 shows that the accuracy drop for both ADC-Less models (VGG16 and ResNet20) on CIFAR10 is around 1.16 – 2.42% compared to the HP-ADC, depending on the size of the crossbar array. This range is slightly higher than the accuracy drops reported in similar works focused on ANNs [20], [21]. The accuracy drop is a natural effect of using spiking models for static tasks. Note, we report accuracy values obtained for the test set in a cross-validation scheme, while previous works only reported accuracy on the validation set. Similarly, for CIFAR100, VGG16 shows a drop in accuracy in the range of 0.23 – 1.78% depending on the crossbar size. In all the cases, the ADC-Less training can minimize the accuracy drop achieving comparable results to the HP-ADC models.

7.1.2 Experiments on Gesture Recognition

As discussed in Section 2.1, SNNs are able to handle spatio-temporal data, such as those produced by event-based cameras. Event-based cameras detect log-scale brightness changes asynchronously and independently on each pixel-array element, producing positive and negative binary impulse trains for the corresponding pixel [29]. This results in binary, sparse, and high-temporal resolution representations, features that make them a good fit for SNNs.

Here, we test DVSNet, described in Section 6, for gesture recognition on the DVS128 Gesture dataset [24]. This dataset contains event data recorded from 29 subjects performing 11

TABLE 2
Test accuracy of DVSNet for gesture recognition on DVS128 Gesture dataset

Metrics	FP	HP-ADC	ADC-Less		
			32	64	128
Acc@1	94.56	94.95	95.15	93.40	91.85
Gap	-	-	+0.2	-1.55	-3.1

hand gestures in 3 different lighting conditions. The data is augmented by slicing the original sequences into time windows of 1.5 seconds without overlapping. Then, event frames are generated by accumulating the events during windows of 75 ms (20 time-steps per sequence) and finally downsamples to a 64 × 64 size. This preprocessing results in 4k sequences for training, 500 for validation, and 500 for testing.

We train our DVSNet model from scratch using surrogate gradients following the proposed three-step hardware-aware training. For the quantization-aware training, we use a 4-bit weight quantization for all the layers. Then, for the ADC-Less training, we use the second weight mapping scheme discussed in Section 5.3 since it encourages sparsity. Similar to the previous section, we evaluate the ADC-Less training with three crossbar array sizes, 32, 64, and 128.

The accuracy values measured on the test set are shown in Table 2. It is worth noting that the ADC-Less model with a crossbar size of 32 is slightly better than the HP-ADC model. It is because of the high sparsity in the intermediate layer activations that result in just a few wordlines being activated at the same time. On the other hand, when increasing the xbar size to 64 and 128 there is an accuracy drop of 1.55% and 3.1%, respectively.

These results so far show that the hardware-aware training proposed can also be used for sequential classification tasks with no significant accuracy loss.

7.1.3 Experiments on Optical Flow Estimation

Optical flow is a computer vision task that aims to estimate the apparent movement of an object (pixel) in a sequence of images. Early works on this task were based on inputs from frame-based cameras. However, these approaches suffered in high-speed motion and challenging lighting conditions while also incurring high energy and latency. We utilize inputs from a low-power asynchronous event-based camera that does not suffer from the above limitations. Recent works adopting an event-based approach to estimate optical flow, demonstrate their importance in terms of maintaining accuracy while being efficient at the same time [9], [30], [31].

For example, [9] showed that combining SNN and ANN layers in a hybrid encoder-decoder architecture (Spike-FlowNet) could achieve a significant improvement in the computational efficiency of the model while achieving a better performance than comparable ANN implementations (EV-FlowNet) [30]. Nevertheless, all previous works focused only on full precision implementations without exploring the potential losses due to hardware constraints.

Here, we train our FSFN model, shown in Fig. 10, on the Multi-Vehicle Stereo Event Camera (MVSEC) dataset [25] following the hardware-aware training methodology dis-

TABLE 3
Comparison of the AEE metric on MVSEC [25] dataset [AEE lower is better]

Models	Quant	Type	Outdoor_day1 AEE	Indoor_flying1 AEE	Indoor_flying2 AEE	Indoor_flying3 AEE
FSFN _{FP} (Ours)	No	Spiking	0.51	0.82	1.21	1.07
FSFN _{HP-ADC} (Ours)	Yes	Spiking	0.48	0.85	1.29	1.13
FSFN _{ADC-Less 32} (Ours)	Yes	Spiking	0.65	0.91	1.41	1.18
FSFN _{ADC-Less 64} (Ours)	Yes	Spiking	0.65	0.88	1.39	1.18
FSFN _{ADC-Less 128} (Ours)	Yes	Spiking	0.65	0.94	1.54	1.30
Spike-FlowNet [9]	No	Hybrid	0.47	0.84	1.28	1.11
EV-FlowNet [30]	No	Analog	0.49	1.03	1.72	1.53
Zhu et al. [31]	No	Analog	0.32	0.58	1.02	0.87
Zero prediction	-	-	1.08	1.29	2.13	1.88

cussed in Section 5. For this purpose, we integrate our training methodology into the self-supervised pipeline training proposed in [9]. Similar to previous works, we train our models on the *outdoor_day2* sequence of the MVSEC dataset and evaluate on the *outdoor_day1* and *indoor_flying1,2,3* sequences.

The quantitative results are shown in Table 3, where we report the Average End-point Error (AEE) metric compared with previous works. Here, the full precision FSFN (FSFN_{FP}) gets better AEE performance than Spike-FlowNet and EV-FlowNet models, which have a similar number of parameters and training pipelines. The quantized FSFN model with HP-ADC (FSFN_{HP-ADC}) shows performance comparable to FSFN_{FP}. This shows that our quantization-aware training can recover most of the performance of the full-precision models. For ADC-Less training, we use the first mapping method discussed in Section 5.3 because optical flow requires less sparsity in the intermediate layers. From Table 3, it can be seen that the performance of our three ADC-Less models (32, 64, and 128) is superior to [30], and only slightly worse than [9]. Note that the ADC-Less model trained with an xbar size of 64 performs slightly better than the one using 32. The main reason behind these results that do not follow an increasing trend is the batch size used during the training. The model with xbar size of 64 allows using a larger batch size, which helps with the convergence of the training.

In addition, Fig. 11 shows the masked optical flow produced by our models compared with the Spike-FlowNet and the ground truth sample in the *outdoor_day1* sequence. As expected, the ADC-Less model produces a noisier estimation, but in general, it captures the apparent movement of different objects with a reasonable performance. The quantitative and qualitative results show that our ADC-Less aware training scheme can be extended to complex spatio-temporal regression problems, like optical flow, and work well with self-supervised learning schemes.

7.2 Hardware Performance

In this section, we estimate energy and latency improvements of the ADC-Less IMC architecture described in Section 4 with respect to a conventional IMC architecture with HP-ADCs. For optical flow estimation (Section 7.1.3), we additionally compare the ADC-Less IMC with the results

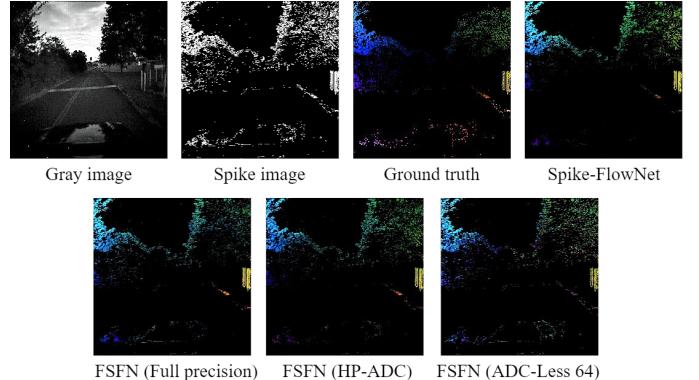


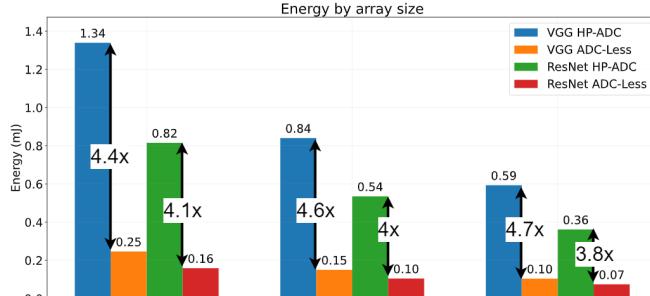
Fig. 11. Masked optical flow evaluation and comparison with Spike-FlowNet. The sample is taken from *outdoor_day1* sequence, and the masked optical flow is the optical flow only in the pixels where there was an event, that is, using the spike image as the mask of the dense flow.

obtained for the FSFN running on an NVIDIA Jetson TX2 board.

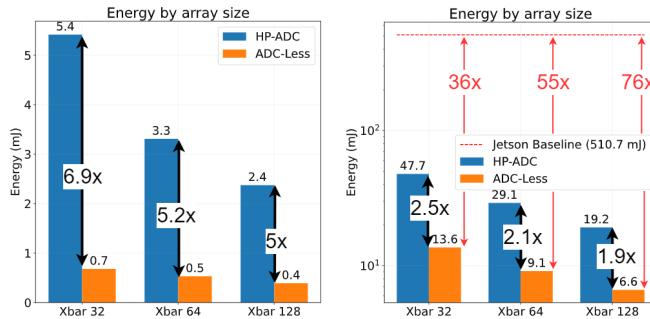
To obtain the energy and latency estimations, we use the DNN+NeuroSim V1.3 [26] simulator. For the simulation, 1-bit ReRAM for bit-cells, Ron/Roff ratio of 150, Flash ADCs, and 65 nm for the technology node was used.

For the ADC-Less architectures, we use a 1-bit ADC connected to each column similar to the sense amplifiers shown in Fig. 3. This is feasible because of the small area required by 1-bit ADC. In contrast, we use an 8-to-1 multiplexer to connect the HP-ADC, that is, 8 columns bitlines share the same ADC, due to the fact that HP-ADC requires much more area, being unrealistic to use one per column [15], [26]. For all the simulations, the resolution of the HP-ADC is set to 5-bit.

Since the NeuroSim simulator is not designed for spiking models, we designed and synthesized the digital LIF neuron (described in Section 4.3) using ModelSim and Cadence RTL compiler with the TSMC 65nm PDK. The metrics obtained for an individual LIF neuron are 1448 μm^2 of area, 1.202 mW of dynamic power, and 57.6 nW of leakage power. Then we appropriately scale this module's area, energy, and latency values to add them to the results from each layer of the model under analysis.



(a) Image classification (VGG16 and ResNet20)



(b) Gesture recognition (DVSNet)

(c) Optical flow (FSFN)

Fig. 12. Energy consumption comparison of the ADC-Less and HP-ADC IMC architectures with different crossbar sizes, running different SNN models for different computer vision tasks.

7.2.1 Energy Improvements

First, we analyze energy improvements for optical flow estimation. The improvements are computed as

$$\text{improvement} = \frac{(\text{HP-ADC} - \text{ADC-Less})}{\text{ADC-Less}}$$

Fig. 12c shows that the ADC-Less architecture consumes $1.9 - 2.5 \times$ lower energy than the same architecture with HP-ADC. As expected, when the crossbar array size increases, the energy consumed per inference is reduced, and the gap between the ADC-Less and HP-ADC reduces, but the ADC-Less architecture still remains energy-efficient.

Since our main motivation is to enable optical flow estimation suitable for edge inference in real-time, we compare our results with the NVIDIA Jetson TX2 platform, an embedded system largely used to deploy DL models at the edge. We observe that the Jetson platform consumes 510.7 mJ per inference of the FSFN model, making our ADC-Less architecture $36 - 76 \times$ more energy-efficient, as depicted in Fig. 12c.

Similar results are obtained for gesture recognition ($5 - 6.9 \times$ lower energy consumption) and image classification ($3.8 - 4.7 \times$ lower energy consumption) tasks, as shown in Fig. 12b and Fig. 12a respectively.

These results show that our proposed ADC-Less architecture is suitable as a low-energy inference engine for edge applications, allowing a direct trade-off between energy and accuracy by choosing the crossbar array size.

7.2.2 Latency Improvements

To estimate latency, we consider all the operations during a forward pass. The simulations were performed under

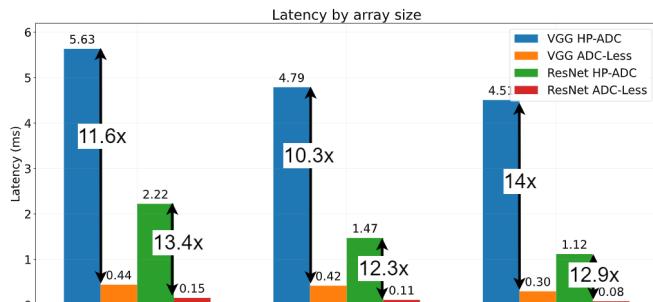
a synchronous operation mode, thus the clock period is determined by the compute-sense cycle. This is measured as the critical path from the input to the memory crossbar arrays till the ADC output generating the partial sum. The latency is determined by the total number of cycles needed for processing. Given this configuration, the clock period for the ADC-Less architectures is around 1.1 ns while the HP-ADC clock period is around 11.9 ns . For all the cases, we report the latency under the assumption that it is possible to implement pipelined processing.

For image classification, the ADC-Less presents latency improvement over the HP-ADC architecture of $10.3 - 14 \times$, as shown in Fig. 13a. Similarly, gesture recognition experiments present latency improvements of $15.9 - 24.6 \times$. In both cases, when the array size increase, the latency decrease.

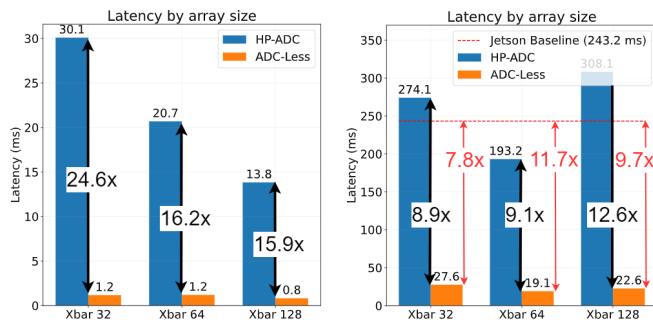
Similar to the previous section, for the optical flow estimation task, we compare the latency values of the ADC-Less architecture with the Jetson TX2 platform and the HP-ADC. When the FSFN model is deployed on the Jetson platform, we obtain a high latency of 243.2 ms , which is far from the usual real-time latency (33 ms or 30 FPS). In contrast, as can be seen in Fig. 13c, the ADC-Less architecture has a $7.8 - 11.7 \times$ latency improvement, which potentially enables real-time inference using FSFN. Similarly, the ADC-Less has an $8.9 - 12.6 \times$ latency improvement over the HP-ADC architecture. One important observation is that when the array size goes from 64 to 128, in Fig. 13c, the latency increases instead of decreasing as was expected. This phenomenon happens because when the array size increase, the model can be mapped using less number of crossbar arrays. This means that fewer tiles are required in the simulator, which goes from 64 tiles for the 64 array size to 16 tiles for the 128 array size. This reduction in the number of tiles produces a bottleneck that increases the latency, which did not happen for other cases, as shown in Fig. 13 because the models are smaller than FSFN.

8 CONCLUSION

Spiking Neural Networks are suitable for performing complex sequential tasks by using their membrane potential as short-term memory. Note, however, most commercial hardware accelerators (GPU-based) are not optimized for such networks. While crossbar-based IMC architectures can be energy-efficient, the usage of expensive HP-ADC is a major obstacle. Unilaterally reducing the ADC precision (and its associated cost) results in significant degradation in the model's performance. To recover the performance we developed hardware aware training that enables IMC architectures with ADC precision as low as 1-bit. The proposed approach shows significant energy and latency improvements, $2 - 7 \times$ and $8.9 - 24.6 \times$ respectively, with respect to HP-ADC IMC architectures with comparable accuracy. Moreover, in contrast to previous works, our methodology naturally extends the range of applications beyond simple image classification tasks to more challenging sequential tasks such as optical flow estimation and gesture recognition.



(a) Image classification (VGG16 and ResNet20)



(b) Gesture recognition (DVSNet)

(c) Optical flow (FSFN)

Fig. 13. Latency comparison of the ADC-Less and HP-ADC IMC architectures with different crossbar sizes, running different SNN models for different computer vision tasks.

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