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LETTER

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A subthermionic tunnel field-effect transistor with an atomically thin channel

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The fast growth of information technology has been sustained by continuous scaling down of the silicon-based metal–oxide field-effect transistor. However, such technology faces two major challenges to further scaling. First, the device electrostatics (the ability of the transistor's gate electrode to control its channel potential) are degraded when the channel length is decreased, using conventional bulk materials such as silicon as the channel. Recently, two-dimensional semiconducting materials[1–7] have emerged as promising candidates to replace silicon, as they can maintain excellent device electrostatics even at much reduced channel lengths. The second, more severe, challenge is that the supply voltage can no longer be scaled down by the same factor as the transistor dimensions because of the fundamental thermionic limitation of the steepness of turn-on characteristics, or subthreshold swing[8,9]. To enable scaling to continue without a power penalty, a different transistor mechanism is required to obtain subthermionic subthreshold swing, such as band-to-band tunnelling[10–16]. Here we demonstrate band-to-band tunnel field-effect transistors (tunnel-FETs), based on a two-dimensional semiconductor, that exhibit steep turn-on; subthreshold swing is a minimum of 3.9 millivolts per decade and an average of 31.1 millivolts per decade for four decades of drain current at room temperature. By using highly doped germanium as the source and atomically thin molybdenum disulfide as the channel, a vertical heterostructure is built with excellent electrostatics, a strain-free heterointerface, a low tunnelling barrier, and a large tunnelling area. Our atomically thin and layered semiconducting-channel tunnel-FET (ATLAS-TFET) is the only planar architecture tunnel-FET to achieve subthermionic subthreshold swing over four decades of drain current, as recommended in ref. 17, and is also the only tunnel-FET (in any architecture) to achieve this at a low power-supply voltage of 0.1 volts. Our device is at present the thinnest-channel subthermionic transistor, and has the potential to open up new avenues for ultra-dense and low-power integrated circuits, as well as for ultra-sensitive biosensors and gas sensors[18–21].

Two-dimensional (2D) semiconducting materials derived from transition metal dichalcogenides (TMDs) are highly promising as channel material for FETs, specifically for mitigating the degradation of device electrostatics (Supplementary Information S1), and hence have attracted much attention recently[1–7]. Their ultra-thin structure and pristine interfaces can lead to excellent electrostatics, and at the same time their planar nature facilitates easy fabrication compared to one-dimensional structures (such as nanowires and nanotubes) that can also provide excellent electrostatics but are far less fabrication-friendly.

Even if excellent electrostatics could be achieved with atomically thin TMDs, the most severe challenge for metal–oxide–semiconductor field-effect transistors (MOSFETs) still remains, which is the increase in power density due to the inability to scale down the supply voltage. This arises from the fundamental thermionic limitation of the subthreshold swing (SS) of $2.3k_BT/q$ (or 60 mV per decade at room temperature) in conventional FETs (CFETs, Supplementary Information S2); here k_B is Boltzmann's constant, T is temperature and q is the elementary charge. (SS is the inverse of the subthreshold slope and is given by $SS = (d\log_{10}I_{DS}/dV_{GS})^{-1}$, where I_{DS} is the drain-to-source current, and V_{GS} the gate-to-source voltage.) Thus, just using 2D semiconducting-channel materials only partially addresses the scaling issue—use of novel device technology based on 2D materials is necessary for simultaneous achievement of efficient electrostatics as well as novel carrier transport mechanisms, in order to achieve SS values below 60 mV per decade and thereby combat power density increase and enable scaling to continue in future. Apart from digital electronics, achievement of a device based on 2D semiconducting-channel material and with subthermionic SS would be highly desirable for next-generation ultra-sensitive, low-power and fast biosensors and gas sensors. Here we demonstrate planar transistors based on a 2D semiconducting material (bilayer molybdenum disulfide, MoS_2), which overcomes the fundamental limitation on SS of CFETs, and offers a minimum SS of 3.9 mV per decade and an average SS of 31.1 mV per decade for more than four decades of drain current at room temperature. This is achieved by using a fundamentally different transport mechanism in the form of quantum mechanical band-to-band tunnelling (BTBT)[22,23].

Tunnel-FETs (TFETs) using BTBT[10–16] are promising candidates for the achievement of subthermionic SS. In spite of the high level of interest in TFETs with 2D channel materials, and experimental work[24,25] in this direction using electrostatic doping techniques, there has not until now been a successful experimental demonstration of a TFET—or of any transistor based on a 2D material with subthermionic SS. Moreover, use of electrostatic doping requires an extra gate electrode for functioning and hence, is not energy-efficient. Here we build a unique vertical TFET with subthermionic SS by engineering the substrate, portions of which are configured as a highly doped semiconductor source and other portions of which are etched and filled with a dielectric for hosting the drain and gate metal contacts, while ultra-thin 2D TMD forms the channel (Fig. 1a). This TFET structure offers several unique advantages. First, the use of a 2D TMD material as the channel produces not only excellent electrostatics but also a small tunnelling distance or tunnelling barrier width (which is determined by the channel thickness), as needed to increase the BTBT current. We note that using a 3D material as the source does not hamper device electrostatics, as it is the channel region that needs to be modulated by the gate and it is atomically thin in our case. Second, combining 3D and 2D materials opens up unprecedented opportunities for designing custom-built heterostructures. We have chosen germanium (Ge) as the 3D material because it has a relatively low electron affinity (EA) and bandgap compared to the other commonly used group IV and III-V semiconductors, while MoS_2 is chosen as the 2D material since it has a relatively high EA compared to the other commonly explored TMDs. Thus, Ge-MoS_2 forms a staggered heterojunction (Fig. 1b), with a small band overlap at the interface, leading to low tunnelling barrier height, which is necessary for increasing the BTBT

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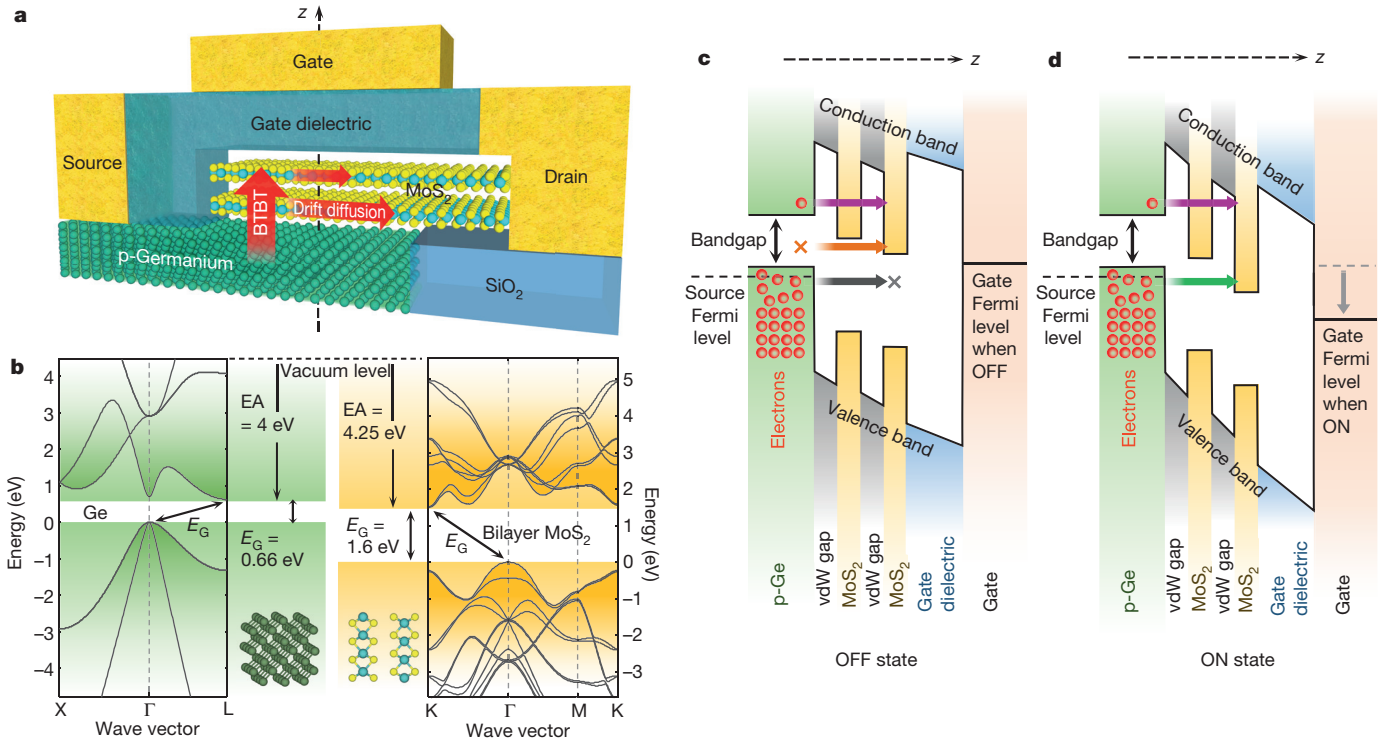

Figure 1 | Schematic and working principle of the ATLAS-TFET. **a**, Schematic diagram illustrating the cross-sectional view of the ATLAS-TFET with ultra-thin bilayer MoS_2 (1.3 nm) as the channel and degenerately doped p-type Ge as the source. Path for electron transport is shown by the red arrows, which run vertically (indicating band-to-band-tunnelling, BTBT) from the Ge source to the MoS_2 and then laterally through the MoS_2 layers (via drift diffusion) to the drain. As the Ge is highly doped, the tunnelling barrier height is mainly determined by the effective band overlap between Ge and MoS_2 while the tunnelling width is determined by the MoS_2 thickness (including the van der Waals gap). **b**, Band alignment of Ge and bilayer MoS_2 showing their electron affinities (EA) and bandgaps (E_G) and, thus, illustrating the formation of a staggered vertical heterojunction. Insets in the middle show the crystal structures of both materials, while the bandstructures are shown on the left and right sides. **c**, **d**, Band diagrams along the vertical dashed line in **a** are shown in both OFF (**c**) and ON (**d**) states. The white regions represent the forbidden gaps (zero density of states, DOS). While the effective bandgap of bilayer MoS_2 is illustrated in **b**, here the bands for the two layers are shown separately with the van der Waals (vdW) gap between them for better visual interpretation of current flow. Note that the drain contact is located perpendicular to the plane of the figure and is not shown. In the OFF state, electrons from the valence band of Ge cannot transport to MoS_2 owing to the non-availability of DOS in MoS_2 (horizontal black arrow and cross sign). At higher energies, empty DOS is available in MoS_2, but no DOS is available in Ge, again forbidding electron flow (horizontal orange arrow and cross sign). With a further increase in energy reaching above the conduction band of Ge, DOS is available in both Ge and MoS_2. However, the number of electrons available in the conduction band of the Ge source is negligible owing to the exponential decrease in electron concentration with increase in energy above the Fermi level according to the Boltzmann distribution. Thus, very few electrons can flow to the MoS_2 (horizontal purple arrow), leading to a very low OFF-state current. With an increase in gate voltage (**d**), the conduction band of MoS_2 at the dielectric interface is lowered below the valence band of the Ge source, and electrons start to flow (horizontal green arrow), resulting in an abrupt (subthermionic) increase in BTBT current.

current. Third, the heterojunction is formed with van der Waals bonds and thus has strain-free interfaces. Fourth, although methodologies for obtaining stable (and high) doping in TMDs are very challenging and still under investigation, 3D materials already enjoy well developed doping technologies that have been used in this work to form a highly doped source. This enables the creation of an ultra-sharp doping profile and hence, a high electric field at the source–channel interface, because there is a negligible chance of diffusion of dopant atoms across the heterojunction owing to the presence of a van der Waals gap. Last, because MoS_2 is placed on top of Ge forming a vertical source–channel junction, BTBT can take place across the entire area of MoS_2–Ge overlap, which leads to a higher current in the ON state than in the case of line overlap obtained in lateral junctions.

Although we are using the term tunnel-FET in a general way, our device is specifically a band-to-band tunnel-FET, involving transition of carriers from the valence band (of Ge) to the conduction band (of MoS_2). Although 'tunnelling-transistors' using heterostructures of 2D materials have been reported[26,27], they did not involve BTBT and hence, cannot lead to devices with SS below 60 mV per decade, because of the fundamental inability of a single carrier tunnelling barrier to provide this (Supplementary Information S3).

Our ATLAS-TFET provides several beneficial attributes relative to other subthermionic transistors. The use of bilayer MoS_2, which is only 1.3 nm thick, leads to a very thin channel transistor with subthermionic SS, which can lead to opportunities for ultra-dense and low-power electronic applications. We have achieved this on a planar platform, which is easily manufacturable compared to 1D structures such as nanowires and nanotubes. It is noteworthy that the International Technology Roadmap for Semiconductors (ITRS) has prescribed the attainment of average SS lower than 60 mV per decade over four decades of current. The only experimental TFET so far reported in the literature to have obtained this metric was produced by Tomioka *et al.*[28], who used a 1D (nanowire) based structure. The ATLAS-TFET is the first TFET demonstrated in planar architecture to satisfy this ITRS prescription, and is the only one to achieve it in any architecture at an ultra-low drain–source voltage V_{DS} of 0.1 V, which is highly desirable for the lowering of supply voltage and hence, power dissipation.

Figure 1c and d demonstrates the operation of the ATLAS-TFET using band diagrams obtained along the vertical dashed line in Fig. 1a, in both the OFF (Fig. 1c) and the ON (Fig. 1d) state. Our device is an n-type transistor, in which positive voltage is applied to the drain electrode (with respect to the source electrode) contacting the MoS_2 layers, which in turn contact the highly p-doped Ge source. Hence, electrons tend to move from the Ge to the MoS_2 and this electron transport can be modulated by the gate to turn the device ON or OFF. In the OFF state, only electrons above the conduction band of

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Ge can transport to MoS_2 (purple arrow), leading to ultra-low current due to the scarcity of available electrons at high energies above the Fermi level. At lower energies, no electrons can flow owing to the non-availability of density of states (DOS) in the Ge source (orange arrow) or in the MoS_2 channel (black arrow). Hence, the OFF current is very low. As the gate voltage is increased, the conduction band of MoS_2 is lowered below the valence band of the Ge source (ON state), and hence filled DOS in the source gets aligned with empty DOS in the channel, leading to an abrupt increase in electron flow (green arrow) and hence, current, which can lead to subthermionic SS. Electrons, after tunnelling from the Ge source to the MoS_2, are 'sucked in' laterally by the drain contact, as shown by the red arrows in Fig. 1a. Note that bilayer MoS_2 is used instead of a monolayer. Although bilayer MoS_2 is 0.65 nm thicker than monolayer MoS_2, the former still offers excellent electrostatics and an ultra-low tunnelling barrier width; at the same time, it has a smaller bandgap[4], higher DOS and is more robust to surface scattering[29].

For fabricating the ATLAS-TFET, we first prepare the engineered substrate. We start with a degenerately p-doped Ge wafer and etch ~300-nm-deep trenches in it, followed by the filling up of the trenches with SiO_2 dielectric and subsequent planarization. Next, formation of 20 nm/50 nm Ni/Au source contact to Ge, as well as cross marks and numberings (to assist electron-beam lithography in subsequent steps), are carried out in a single step. The engineered substrate with the source contact pads and markings is shown in Fig. 2a. To enable scalable technology, MoS_2 is synthesized using the chemical vapour deposition (CVD) process (details in Supplementary Information S4) and transferred onto the engineered substrate (Fig. 2b), followed by etching of MoS_2 except in regions where we plan to make the devices (Fig. 2c). Subsequently, the drain contact to MoS_2 is defined using electron-beam lithography followed by metallization with 20 nm/50 nm Y/Au (Fig. 2d). The TMD technology is still undergoing development, and formation of scaled and high-quality gate dielectrics remains a challenge. Hence we form the gate capacitor of the TFET, not from a conventional high-k dielectric, but from a solid polymer electrolyte, consisting of poly(ethylene oxide) and lithium perchlorate ($LiClO_4$), which can lead to high gate capacitance due to the formation of an electrical double layer[30]. With advances in TMD technology and the achievement of high-quality scalable gate dielectric materials, a conventional gating method using high-k gate dielectrics could be integrated into the ATLAS-TFET. Details of the processing steps are given in Supplementary Information S5.

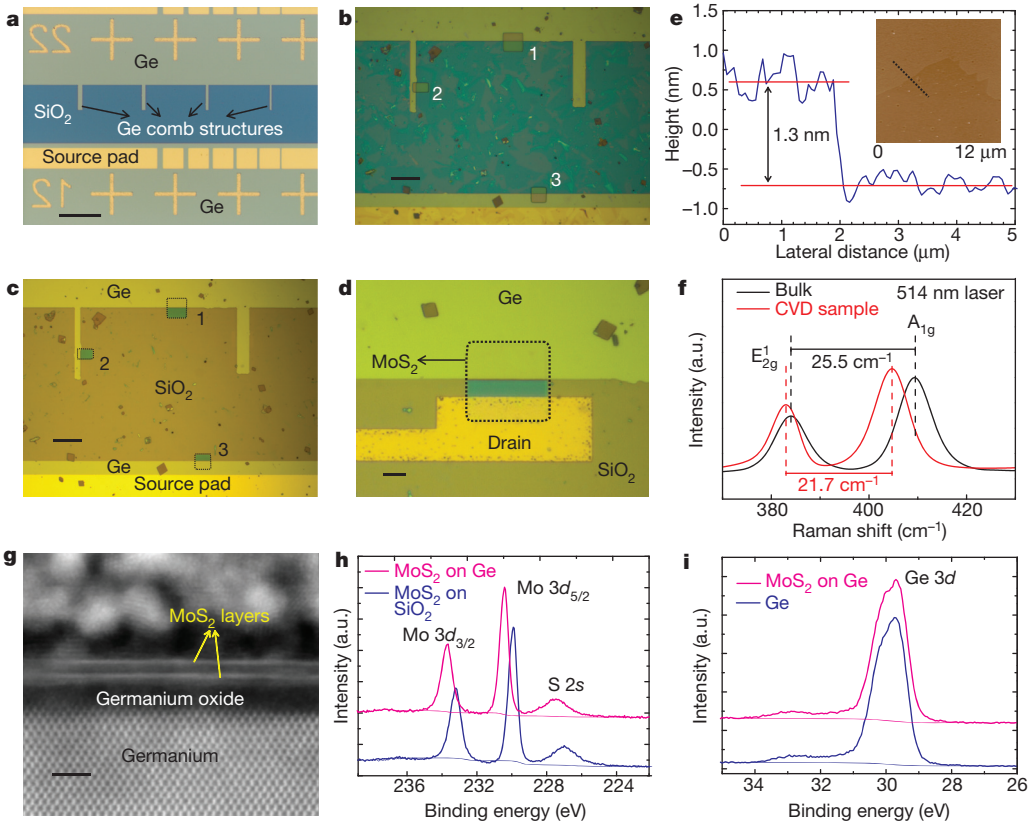

Figure 2 | Fabrication of an ATLAS-TFET and characterization results. **a**, Engineered substrate consisting of alternate layers of Ge and SiO_2 along with Ge comb structures. The Ge comb structures increase the probability of achieving 'necessary overlap regions', which means that part of the MoS_2 flake overlaps the Ge while the other part overlaps the SiO_2 and thus combs are important, especially if the flakes are small. Metal source pads as well as markings required to assist electron-beam lithography are also shown. Scale bar, 100 µm. **b**, Engineered substrate with the CVD synthesized MoS_2 transferred onto it. Regions marked 1, 2 and 3 in the image show three different ways in which 'necessary overlap regions' can be obtained. Scale bar, 25 µm. **c**, After etching the MoS_2 from all other regions except those marked 1, 2 and 3. Scale bar, 25 µm. **d**, After drain formation using electron-beam lithography for the region marked 1 in **b** and **c**. Scale bar, 5 µm. More details on device fabrication can be found in Supplementary Information S5. **e**, Atomic force microscopy performed on bilayer MoS_2 confirming that the thickness is 1.3 nm. The height profile is plotted along the dotted line shown in the inset. **f**, Raman spectroscopy (using a 514 nm laser) of the CVD bilayer sample (red curve), showing the E^1_{2g} peak at 383.0 cm^{-1} and the A_{1g} peak at 404.7 cm^{-1}, which confirms that the sample is indeed bilayer MoS_2. Comparison is also shown with spectrum of bulk MoS_2 (black curve) for reference. **g**, Cross-sectional TEM image of bilayer MoS_2 on Ge. Scale bar, 2 nm. **h**, Comparison of Mo 3*d* core level doublet ($3d_{3/2}$ and $3d_{5/2}$) of MoS_2 on SiO_2 with that of MoS_2 on Ge, showing a 480 meV shift towards higher binding energy in the latter case. This is due to band bending in MoS_2 because of the presence of positive charges in it when placed on Ge. The sulfur 2*s* core level also shows a similar shift in binding energy. **i**, Comparison of the Ge 3*d* core level for Ge alone and for Ge with MoS_2 on it, showing negligible difference between the two, indicating an absence of band bending in Ge due to its high doping level. The deconvolution of the Ge 3*d* level is not shown here for clarity, and is illustrated in Supplementary Information S6.

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The MoS_2 sample is characterized using atomic force microscopy and Raman spectroscopy, as shown in Fig. 2e and f, respectively. A transmission electron microscope (TEM) image of the cross-section of bilayer MoS_2 on Ge is presented in Fig. 2g, which clearly reveals the two MoS_2 layers, the Ge crystal and the presence of a thin layer of native germanium oxide. X-ray photoelectron spectroscopy (XPS) was performed to investigate the electronic structure of the Ge-MoS_2 heterostructure. As is evident from Fig. 2h, the Mo 3*d* core level in the heterostructure shifts towards higher binding energies by about 480 meV compared to that of pristine MoS_2. The sulfur 2*s* levels also shift by the same amount. This shift is due to band bending in MoS_2 in the heterostructure owing to the presence of positive charges. No shift in the Ge core levels is observed, which is consistent with the fact that band bending in Ge is almost negligible owing to its high doping (Fig. 2i). Details of the XPS results are presented in Supplementary Information S6.

The electrical characterization of the device is first performed in a two-terminal configuration, just using the source and drain contacts, without any polymer gate (Fig. 3a). We find that the device essentially behaves like a p–n junction (Fig. 3b). Note that no rectification is observed and a large current is obtained even under the reverse bias condition because of the high BTBT current due to the ultra-thin tunnelling barrier. The trend towards negative differential resistance, as shown by the circled region in the forward bias characteristics in Fig. 3b, confirms the existence of BTBT (Supplementary Information S7). BTBT is further confirmed through temperature-dependent measurements, as shown in Supplementary Information S8. Next, the transistor analysed is measured in a three-terminal configuration using the source, drain and gate (Fig. 4a). Figure 4b shows the transfer (I_{DS}–V_{GS}) characteristics of the device for different V_{DS} starting from a drain voltage as low as 0.1–1 V. It is observed that for all the drain voltages, the ATLAS-TFET can overcome the fundamental limitations on SS (60 mV per decade at room temperature) in MOSFETs, and SS values below 60 mV per decade are obtained over about four decades of current. We note that although the low SS occurs at a negative gate voltage, it can be adjusted by changing the work function of the gate metal. Also, the achievement of sub-60 mV per decade at room temperature using our ATLAS-TFET is repeatable, and the hysteresis in the transfer characteristics is negligible, as shown in Supplementary Information S10 and S11, respectively. The output characteristics are shown in Supplementary Information S12.

To compare the performance of our ATLAS-TFET with a CFET, a CFET is fabricated using the same MoS_2 thickness and measured under similar conditions (Supplementary Information S13). The SS of the ATLAS-TFET and the CFET is plotted in Fig. 4c. The lowest SS achieved for the CFET is 60 mV per decade, whereas for the ATLAS-TFET, not only is a minimum SS as low as 3.9 mV per decade obtained, but excellent average SS values (in mV per decade) of 5.5, 12.8, 22 and 31.1 are obtained over 1, 2, 3 and 4 decades of current, respectively. (These average values of SS have been derived using equation (s3) in Supplementary Information S3, and the data points within the range of drain currents from around 10^{-13} A to 10^{-12}(/10^{-11}/10^{-10}/10^{-9}) A are used for obtaining the average over 1(/2/3/4) decades of current.) In Fig. 4c, the noisy data points have been eliminated and thus the average of the point SS values of ATLAS-TFET plotted in that figure leads to a similar average SS over four decades, as obtained above. The performance of the ATLAS-TFET is also compared to that of other experimental TFETs with subthermionic SS reported in the literature (Supplementary Information S14). In addition to the superior SS of the ATLAS-TFET (compared to that of all other TFETs with subthermionic SS), the current obtained at a low V_{DS} of 0.1 V is more than two orders of magnitude larger than that obtained in ref. 28 (which is the only other TFET to have obtained subthermionic SS over four decades of drain current, although at higher V_{DS}) for the same V_{DS}. The current in the ATLAS-TFET could be further improved by removing the interfacial germanium oxide layer, which adds extra tunnelling resistance to the device as explained in Supplementary Information S15. Intrinsically, the ATLAS-TFET is promising for obtaining a high ON current because of the larger area for tunnelling (compared to the case of line overlap obtained in lateral junctions) as well as the small tunnelling barrier width, which is determined by the channel thickness (Supplementary Information S16). Higher ON current could improve the gate-to-source capacitance, while the gate-to-drain capacitance could be reduced by introducing an underlap region (Supplementary Information S17). The ATLAS-TFET is also advantageous compared to 1D TFETs, as discussed in Supplementary Information S18. Finally, to ensure that the performance of the ATLAS-TFET was not due to any substrate effects from Ge, we fabricated and characterized a CFET having identical channel (bilayer MoS_2) and gate dielectric (polymer complex) materials, and where p-Ge acts mainly as the substrate and not as the source because the source metal is directly connected to the

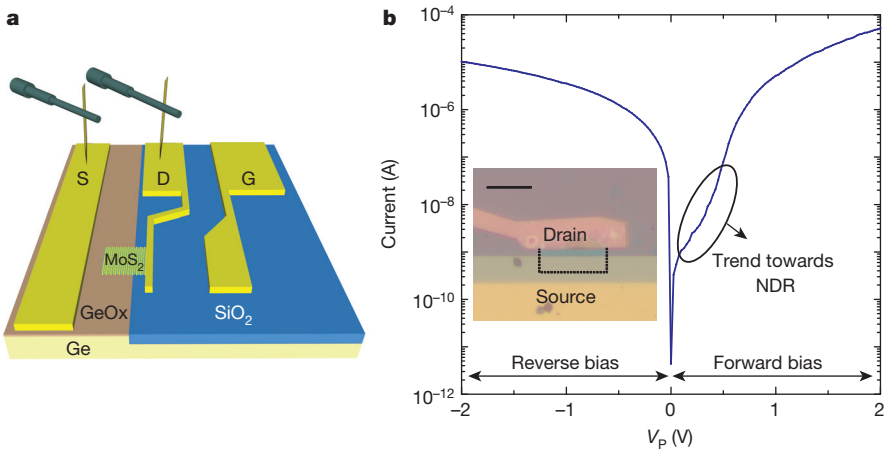

Figure 3 | Room-temperature electrical characteristics of an ATLAS-TFET in diode configuration. **a**, Schematic diagram showing the probing configuration for measurement of the characteristics of the p–n junction diode formed by highly p-doped Ge and naturally n-doped MoS_2. The presence of a thin layer of germanium oxide (GeOx) is also shown. Note that, although there is a layer of germanium oxide between the source contact and the Ge, we have still achieved ohmic contact to Ge, owing to the ultra-thin nature of the oxide. **b**, Current as a function of applied bias (V_P) on Ge while the contact to MoS_2 is grounded. The p–n junction characteristics are shown in both forward and reverse bias conditions. The circled region in the forward biased characteristics shows a trend towards negative differential resistance (NDR), confirming band-to-band-tunnelling (BTBT) current (as explained in Supplementary Information S7). The measured device is shown in the inset (scale bar, 10 μm). The length and width of the device are 5.1 μm and 15 μm, respectively, and the area of overlap of MoS_2 and Ge is 54.6 μm^2.

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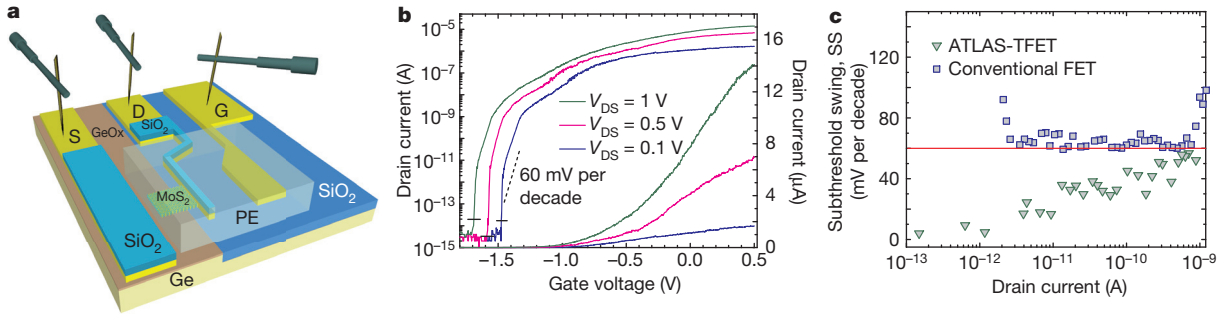

Figure 4 | Room-temperature electrical characteristics of an ATLAS-TFET. **a**, Schematic diagram showing the probing configuration for measurement of the characteristics of the ATLAS-TFET. The source and drain electrodes are covered with SiO_2 to prevent these electrodes from influencing the polymer electrolyte as well as to reduce leakage between these electrodes and the gate. **b**, Drain current as a function of gate voltage for three different drain voltages of 0.1 V, 0.5 V and 1 V. The 'cross point', where the drain current become similar to the gate leakage current (gate leakage characteristics are shown in Supplementary Information S9), is shown by a short black dash on each curve for a particular V_{DS} (note logarithmic scale). Below these cross points, current from the gate flows into the source and drain terminals and contaminates the source–drain current. In our case, current from the gate goes mainly to the source owing to the higher overlap between Ge and the polymer complex gate. The cross points occur at or below 3×10^{-14} A for all the V_{DS} values plotted. We derived SS over the current range above 10^{-13} A (specifically 10^{-13}–10^{-9} A), which is well above the cross points and hence the SS is not contaminated by the gate leakage. The dashed black line indicates a slope of 60 mV per decade. Although SS may appear steeper than 60 mV per decade only for $V_{DS} = 0.5$ V, in the current range between 2 pA and 1 nA, it is also below 60 mV per decade for V_{DS} values of 0.1 V and 1 V. The average SS in the current range between 2 pA and 1 nA for a V_{DS} of 0.1 V and 1 V is 52.6 mV per decade and 46.4 mV per decade, respectively. The device measured is the same as in Fig. 3b. The shift in the curves to the left with increasing V_{DS} is due to the higher drain capacitance, which is a general feature of all TFETs (Supplementary Information S12). Note the two sets of drain current curves in **b**, one on a log scale (left set of curves and *y* axis) and the other on a linear scale (right set of curves and *y* axis). **c**, SS as a function of drain current for an ATLAS-TFET (green triangles) as well as a conventional MOSFET (blue squares) at $V_{DS} = 0.5$ V. The red line demarcates the fundamental lower limit of SS of conventional FETs.

MoS_2; this CFET exhibited an SS of >60 mV per decade, as expected (Supplementary Information S19).

Our ATLAS-TFET can potentially address both the scalability and energy-efficiency requirements of nanoscale FETs, and can guide development of next-generation ultra-low-power integrated electronics and ultra-sensitive sensors.

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Author Contributions K.B. initiated, planned and led the research. D.S. designed and fabricated the devices, collected and analysed the data, with input from X.X., W.L., W.C. and J.K. X.X. and W.L. performed Raman analysis. W.C. collected and analysed data on previously demonstrated tunnel-FET devices. Y.G. and P.M.A. synthesized large-area bilayered MoS_2 samples. S.K. performed TEM analysis. D.S. and K.B. wrote the main Letter and the Supplementary Information with input from all other authors.

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