DESIGNING A DIGITAL CLOCK

Group Members

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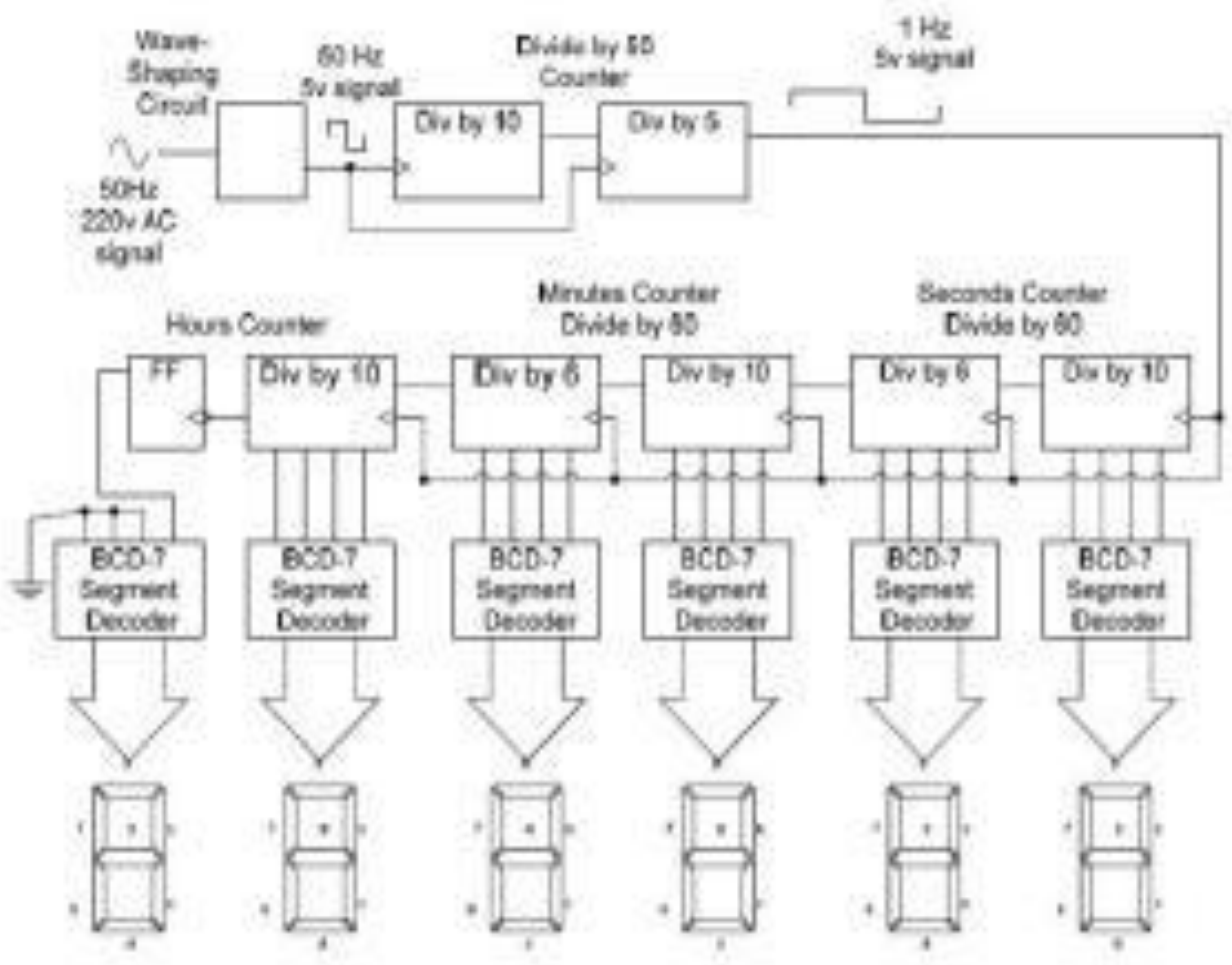
DESIGN OF THE DIGITAL CLOCK

_Here, we make a digital clock to count time using seven segment decoders, T flip flops and some gates. And we use six separate seven segment displays to display seconds, minutes and hours of a day. The design of the circuit is following.

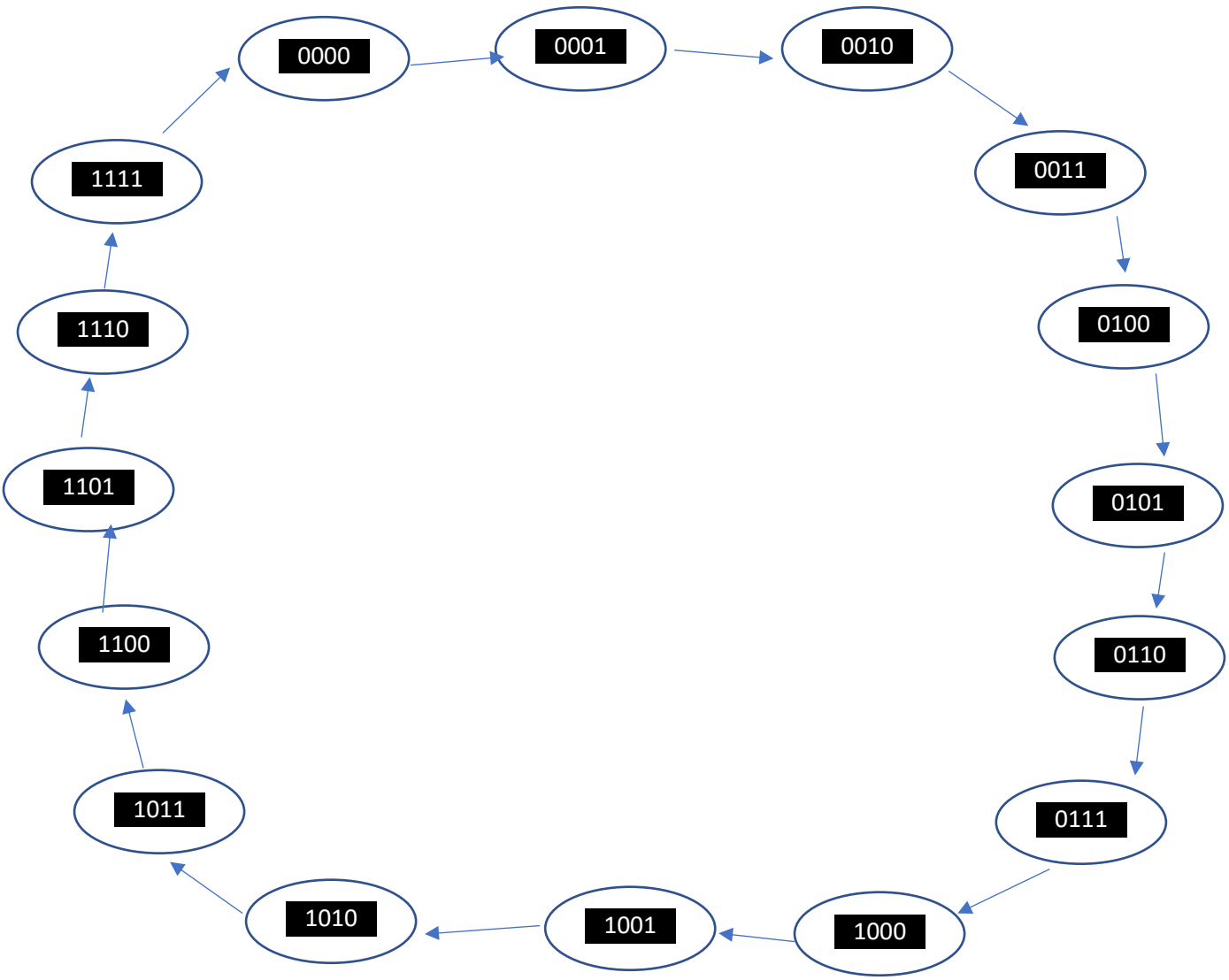


Design the circuit diagram for the clock

This is 12 hours digital clock. Therefore, we have to use two seven segment display for each one part such as for hours count, minutes count and seconds count. An each part time goes from 1 to 12. So in that case 4-bit synchronous counter is used in designing the clock.

1. Number of bits-4
2. Number of states-16 states (2^4 states)
3. Number of outputs- 4 outputs (Q_1,Q_2,Q_3,Q_4)

State diagram



Characteristic table

Current State				Next State							
Q_A	Q_B	Q_C	Q_D	Q_A^+	Q_B^+	Q_C^+	Q_D^+	D_A	D_B	D_C	D_D
X	X	X	X	0	0	0	0	0	0	0	0
X	X	X	X	Q_A	Q_B	Q_C	Q_D	Q_A	Q_B	Q_C	Q_D
X	X	X	X	Q_A	Q_B	Q_C	Q_D	Q_A	Q_B	Q_C	Q_D
X	X	X	X	Q_A	Q_B	Q_C	Q_D	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	0	1	1	0	0
1	1	0	0	1	1	0	1	1	1	0	1
1	1	0	1	1	1	1	0	1	1	1	0
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0	0

Excitation table for D flip flop

Q	Q+	D
0	0	0
0	1	1
1	0	0
1	1	1

K-Maps

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	1	1	1	1
10	1	1	0	1

$A(t+1) = BCD + AD^1 + AC^1$

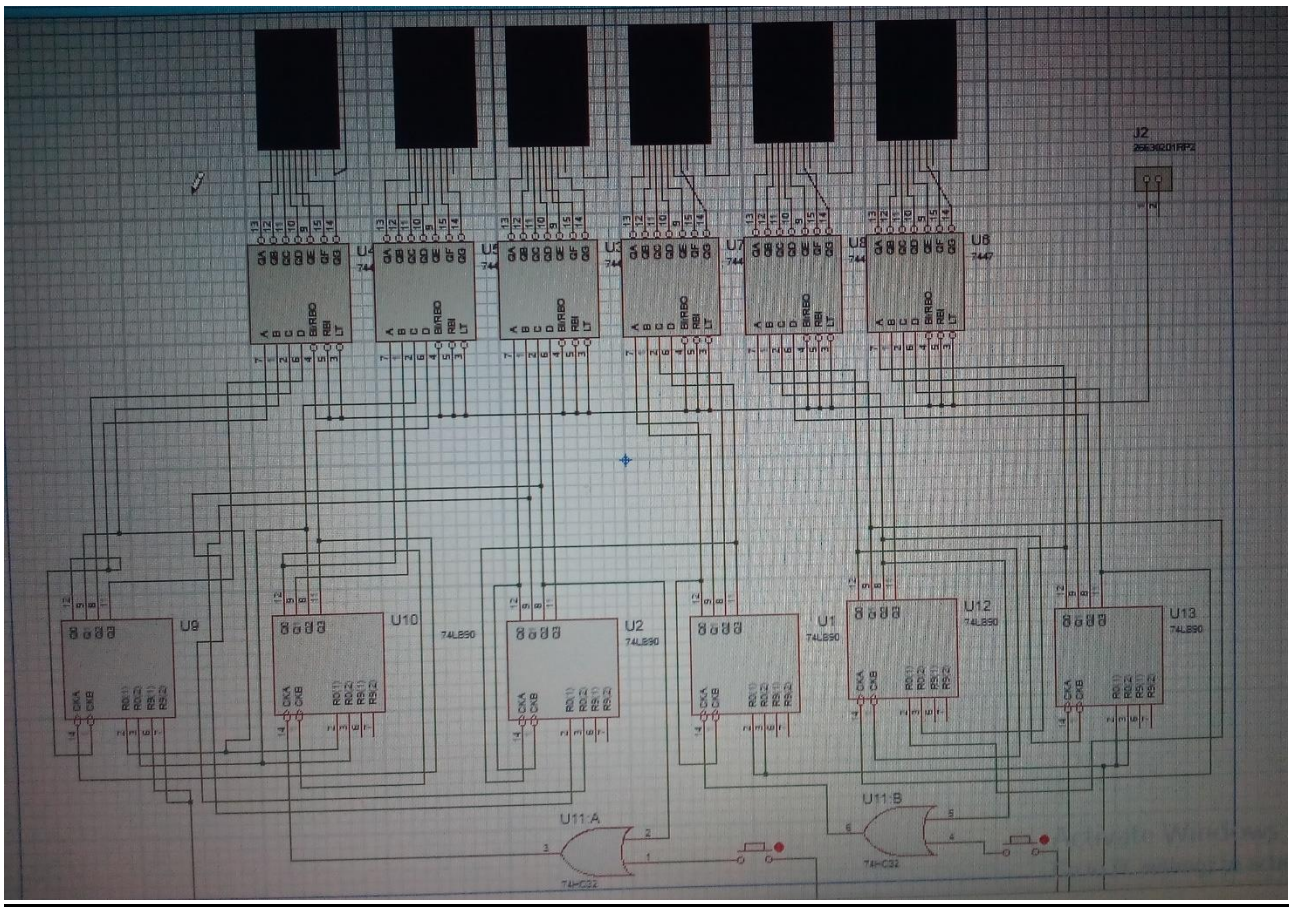
AB \ CD	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	1	1	0	1
10	0	0	1	0

$B(t+1) = B^1CD + BD^1 + BC^1$

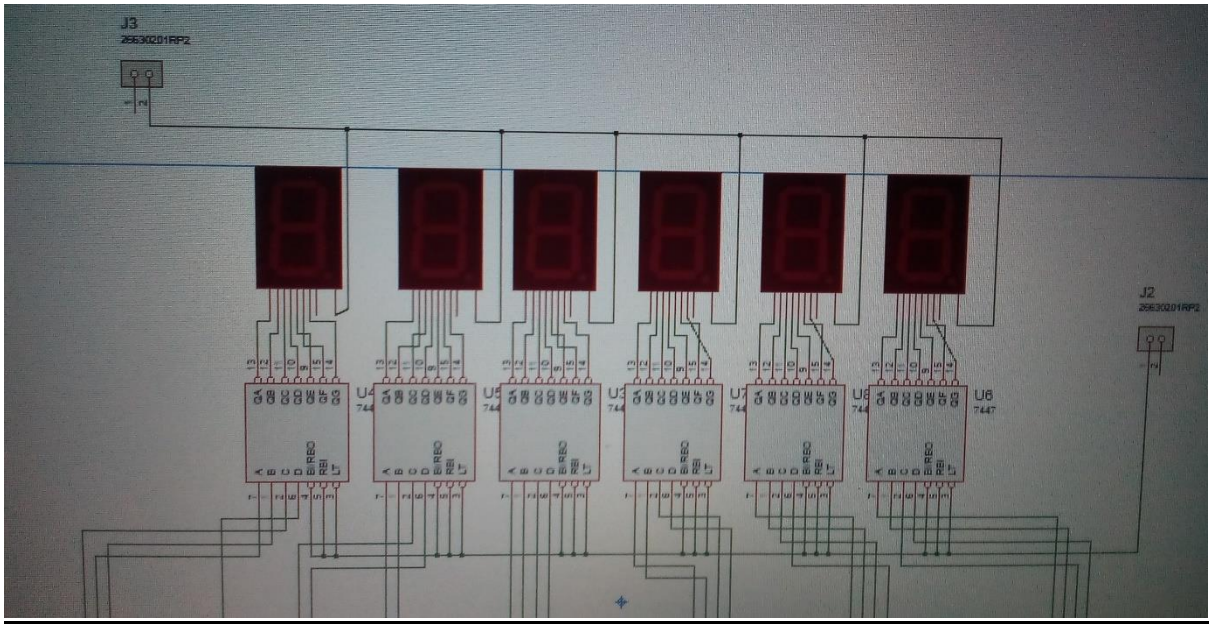
AB \ CD	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$C(t+1) = CD^1 + C^1 D$

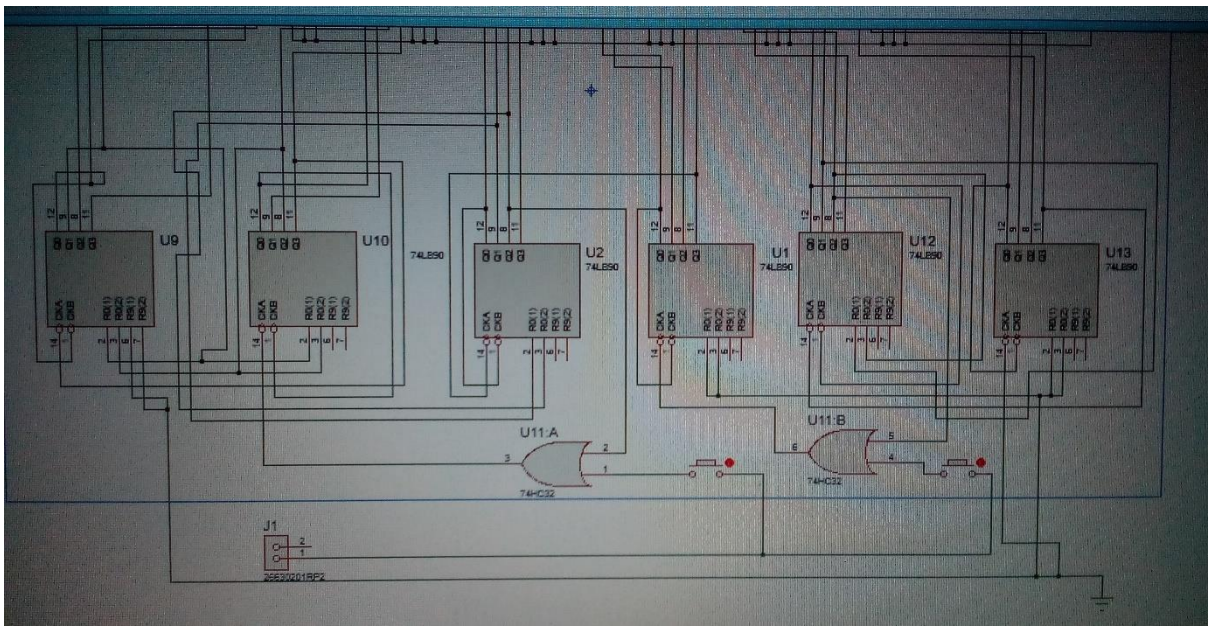
Shematic capture of the circuit



Seven segment dispalys



How decorders connect with the circuit



PCB design for the design