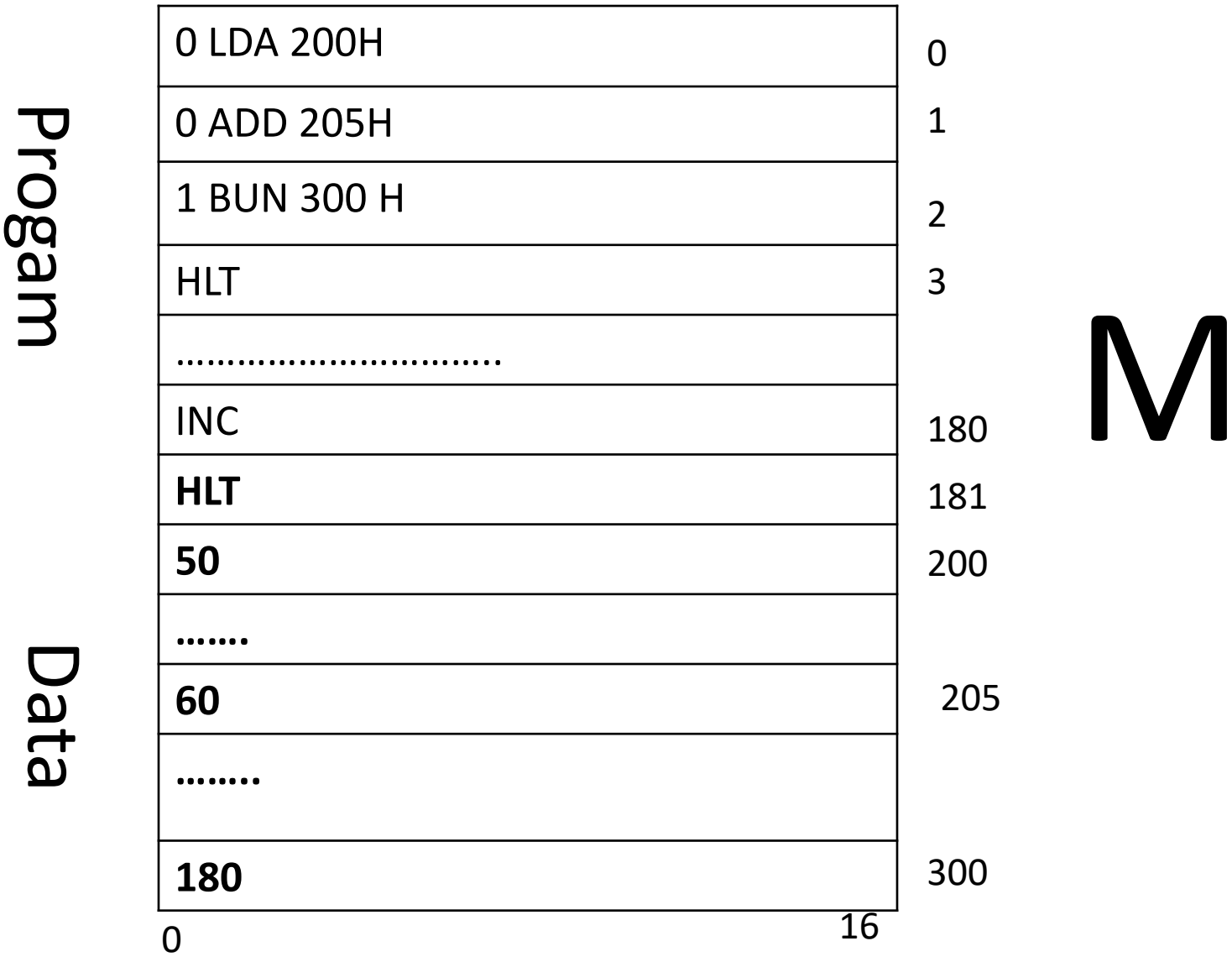
Fetch Decode and Execute cycle

Instruction Cycle

Assume a Memory Unit contains following program



- Question: Illustrate how each instruction is processed by a CPU?

Solution

- Each instruction is passed through Fetch decode and execute cycle which is collectively known as instruction cycle.

Contd…

- Let the program counter points the instruction located at location 0 of memory unit.
- During Fetch and decode cycle we know that

T0: AR← PC

So at T0 cycle AR will have

T0: AR← 0

Contd…

- At T1 cycle the RTL is

  T1 : IR$\leftarrow$ M[AR] , PC $\leftarrow$ PC+1

  So,

  T1: IR $\leftarrow$ M[0] , PC $\leftarrow$ 0+1=1

  At this stage Instruction register will have content pointed out by memory location 0.

  T1: IR $\leftarrow$ 0 LDA 200H , PC $\leftarrow$ 1

  Next cycle is all about decoding the instruction and finding out the effective address of an operand if it is Memory reference instruction else remaining bits will be used as the type of either RRI or IOI.

Decode cycle

T2 : I ← IR (15), D0……D7 ← IR (14 13 12), AR ← (11…….0)

So at this cycle (T2),

I flip flop will have 0 as an input, Decoder D2 will be active because IR (14 13 12) will have bit pattern $(0\ 1\ 0)_2$ and AR will have 200H value.

The system will know this as MRI as soon as D2 is active. Direct memory access because I flip flop have 0 as an input. The remaining 12 bits in AR will be used to find out the effective address of the operand. In this case AR will have 200H.

Execution cycle

- Next step is to fetch the effective address for MRI so it will go to execution cycle.
- So for LDA instruction, execution cycle will be

D2T4: DR ← M[AR]

= D2T4: DR ← M[200H]

= D2T4: DR ← 50 (as an decimal value)

Execution cycle

- Final step for 0 LDA 200 H is to copy the content of location 200H to Accumulator.

$$D2T5: AC \leftarrow DR, SC \leftarrow 0$$

$$= D2T5: AC \leftarrow 50, SC \leftarrow 0$$

So, Accumulator will have value 50 and sequence counter (SC) will be set to 0. That means the system has completed instruction cycle for content located at M [0].

- This process will continue until we reach end of the program HLT [Stop the program]. Even the Halt instruction should go through instruction cycle to terminate a program. Program runs sequentially until conditional or unconditional branching is encountered.

Instruction cycle for next instuction

- Next instruction to be processed is memory location 1 because program counter points to location 1.
- so Fetch and decode cycle will be

  T0: AR← PC

  So at T0 cycle AR will have

  T0: AR← 1

- At T1 cycle the RTL is

  T1 : IR$\leftarrow$ M[AR] , PC $\leftarrow$ PC+1

  So,

  T1: IR $\leftarrow$ M[1] , PC $\leftarrow$ 1+1 = 2

  At this stage Instruction register will have content pointed out by memory location 0.

  T1: IR $\leftarrow$ 0 ADD 205H , PC $\leftarrow$ 2

Decode cycle

T2 : I ← IR (15), D0……D7 ← IR (14 13 12), AR ← (11…….0)

So at this cycle (T2),

I flip flop will have 0 as an input, Decoder D1 will be active because IR (14 13 12) will have bit pattern $(0\ 0\ 1)_2$ and AR will have 205H value.

The system will know this as MRI as soon as D1 is active. Direct memory access because I flip flop have 0 as an input. The remaining 12 bits in AR will be used to find out the effective address of the operand. In this case AR will have 205H.

Execution cycle

- Next step is to fetch the effective address for MRI so it will go to execution cycle.
- So for ADD instruction, execution cycle will be

D_1T_4: DR $\leftarrow$ M[AR]

= D_1T_4: DR $\leftarrow$ M[205H]

= D_1T_4: DR $\leftarrow$ 60 (as an decimal value)

Execution cycle

- Final step for 0 ADD 205 H is to copy the content of location 205H to Accumulator.

$$D_1T_5: AC \leftarrow AC + DR, SC \leftarrow 0$$

$$= D_1T_5: AC \leftarrow 50 + 60, SC \leftarrow 0$$

So, Accumulator will have value 110 and sequence counter (SC) will be set to 0. That means the system has completed instruction cycle for content located at M [1].

- Similarly we can interpret for 1 BUN 300 instruction. But it will cause unconditional branch so program will be diverted to memory location 300 which is indirect address as it is 1 BUN 300.

For INC operation

- All RRI or IOI based instructions are executed in T3 cycle. Before that INC should also go through fetch and decode cycle. Decoder D7 will be active and we know that this is RRI.

r = $D_7 I'T_3$ => Register Reference Instruction

r: SC $\leftarrow$ 0

<u>INC</u>

rB5: AC $\leftarrow$ AC + 1

Similar is the case for Halt operation [RRI]