Kathmandu University
School of Engineering
Department of Computer Science & Engineering
BACHELOR LEVEL PROGRAM

Name of the Course: Pankaj Raj Dawadi
Duration of Course Delivery:

Course Delivery Details:

Date	Time (from-to)	Total hours	Topics covered or activity	Remarks
Week1		4	Logic Gates Boolean Algebra Map Specification Combinational Circuits Flip-Flops Sequential Circuits Design of a counter, State Diagram, State Table, Excitation table	
			Combinational Circuits Flip-Flops Sequential Circuits Design of a counter, State Diagram, State Table, Excitation table	**End of Chapter 1**
Week 2		4	Register Encoder, Decoder, MUX, DMUX	
			Memory Components RAM, ROM Integrated Circuits	**End of Chapter 2**
Week 3		4	Data Types Complements Fixed Point Representations Floating Point Representations	
			Other Binary Codes, grey code, alphanumeric code, 8421,2421, Hamming Code Error Detection Codes	**End of Chapter 3**
Week 4 Week 5		6	Register Transfer Language Register Transfer Bus and Memory Transfers	
			Shift Micro operations Arithmetic Logic Shift Unit Arithmetic Micro operations	**End of Chapter 4**

			Logic Micro operations	
Week 5 Week 6 Week 7		10 Hours	Instruction Codes Computer Registers Computer Instructions Timing and Control	**]**
			Instruction Cycle Memory Reference Instructions Input-Output and Interrupt	
			Complete Computer Description Design of Basic Computer Design of Accumulator Logic	**End of Chapter 5**
Week 8 Week 9		6	Introduction General Register Organization Stack Organization	
			Instruction Formats Addressing Modes Data Transfer and Manipulation	
			Program Control Reduced Instruction Set Computer	**End of Chapter 6**
Week 10 Week 11 Week 12		6	Fixed Point Arithmetic Operation Addition of Signed Magnitude Data Addition of 2's Complement Data Subtraction of Signed Magnitude Data Subtraction of 2's Complement Data	
			Multiplication of Signed Magnitude Data Array Multiplier	
			Booth Algorithm Division Algorithm of Signed Magnitude Representation	End of Chapter 7
Week 13		4	Peripheral Devices Input-Output Interface Asynchronous Data Transfer	
			Modes of Transfer Priority Interrupt Direct Memory Access Input-Output Processor Serial Communication	End of Chapter 8

Mini Project		10 hours	Discussion on Design of a simple processing unit	6 hours allocated for discussion 4 hours allocated for evaluation [Project Presentation + Viva + Project Demonstration]
	Total	Direct Contact Indirect contact	**44 Hours** **10 Hours**	