Mini project 3: Sine Wave

Ishan Porwal

The goal of this project was to use the OSS CAD suite to design a digital circuit to produce a sinusoidal waveform through a 10-bit R-2R ladder digital-to-analog converter (DAC). Given the symmetrical characteristics of sine waves, the main challenge was to generate the waveform while minimizing the amount of memory used. The original look-up table provided had 512 values representing a full cycle, but for this implementation, it was reduced to only the first 128 values, or the first quarter of the cycle. The remaining three-quarters were recreated using the symmetry mentioned above. The circuit was implemented using SystemVerilog and simulated using Icarus Verilog to verify functionality before flashing to hardware.

The circuit created uses a 9-bit counter *sample_idx* to keep track of the current sample from the look-up table for the cycle. This counter is incremented on every clock cycle and automatically reset after reaching the end of a full cycle (511 samples). *quarter_mem* was used to store the 128 values of 10-bit data (decimal values ranging from 512 to 1023) from the look-up table. Based on *sample_idx*'s value, the DAC output value can be calculated, and thus, all four sections of the complete sine wave cycle can be reconstructed. Initially, the output is rising from 512 to 1023 in decimal, which can be handled by directly accessing *quarter_mem[sample_idx]*. The second quarter-cycle is formed by mirroring the values of the first quarter-cycle in reverse order. The third quarter-cycle is generated by subtracting the values of the first quarter from 1024, creating an inverted version. The fourth quarter-cycle is derived by mirroring the third quarter-cycle in reverse order. Finally, this computed 10-bit DAC output (*dac_out*) is assigned to the individual output logic signals corresponding to the DAC's 10-bit input.

The testbench is created to verify that the waveform generation initializes the circuit, generates a clock signal, and simulates for more than one complete cycle (10,000 time units). The clock signal toggles every 40 ns, which is close enough to the 12 MHz clock frequency on board for this application.

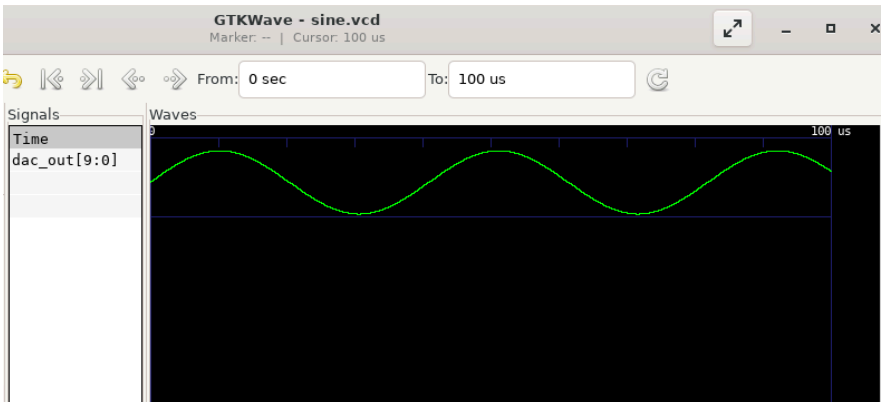

Figure 1. Screengrab of gtkwave plot showing more than 1 cycle simulation of sine wave as a function of time

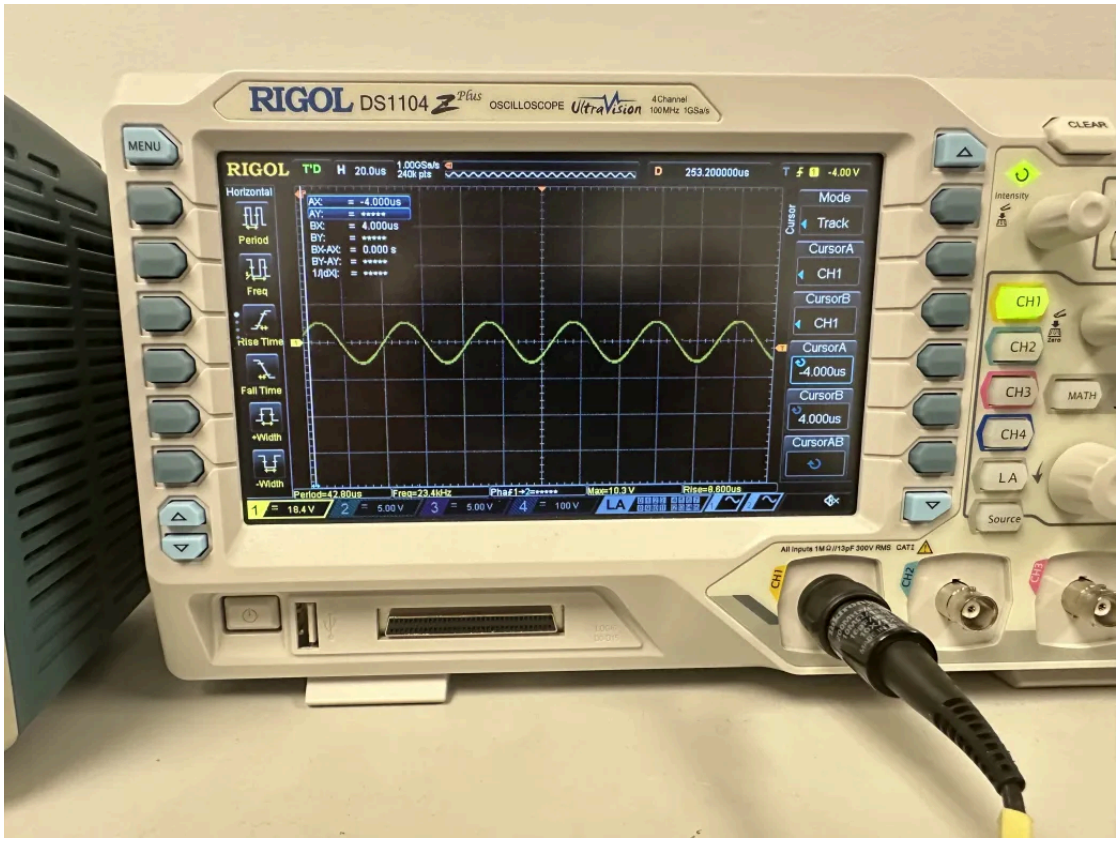

Figure 2. Measured voltage waveform produced by the circuit using an oscilloscope