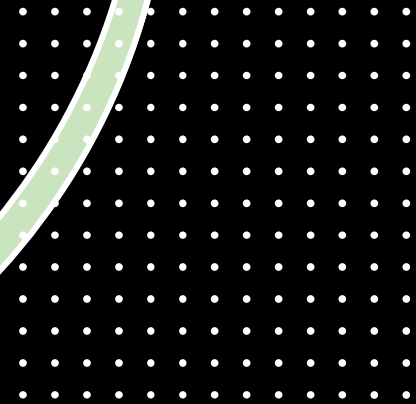
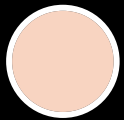
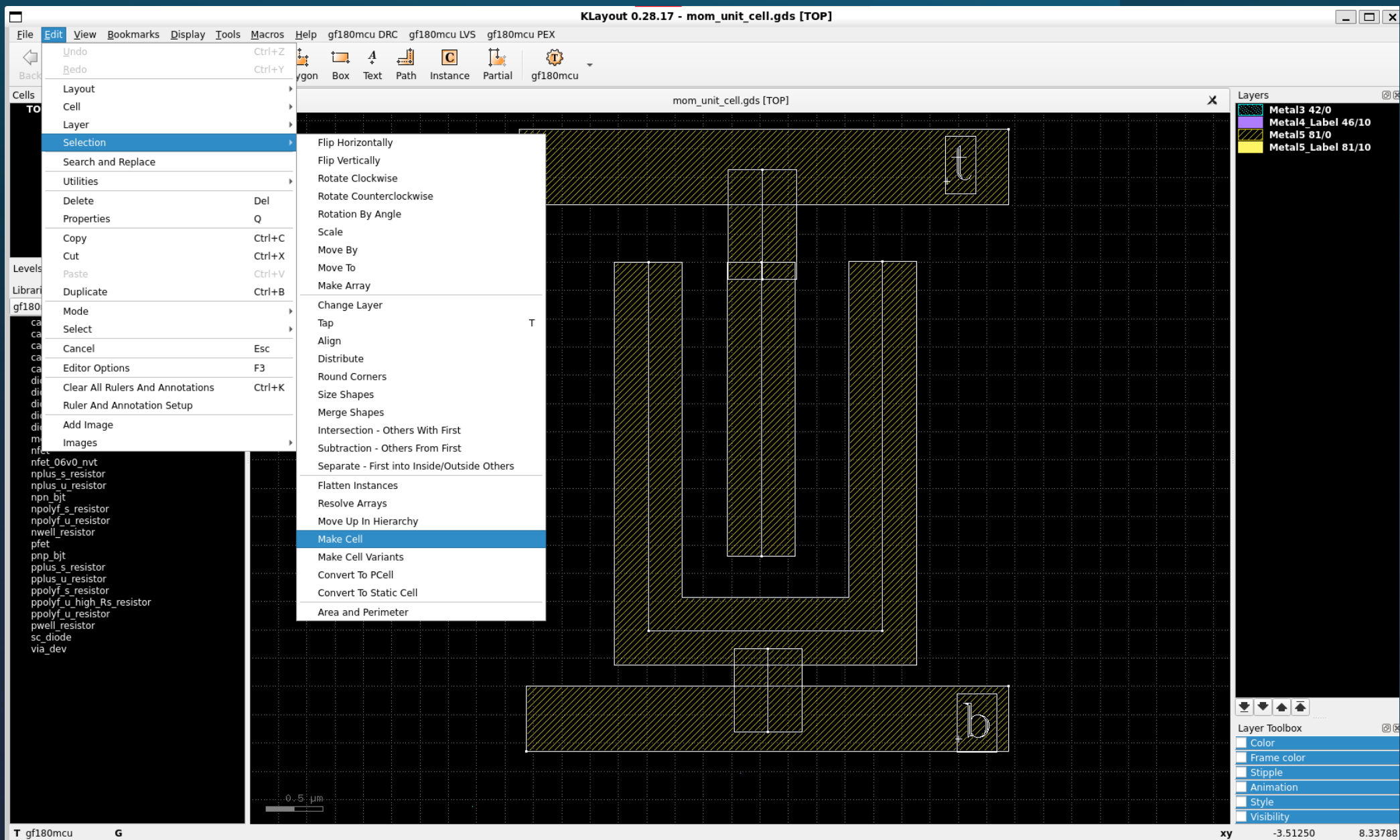


Cell化とArray配置

Cell化







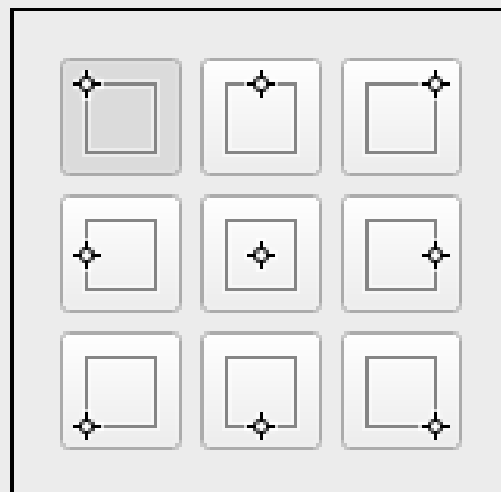
Make Cell



Name of cell to make from selected shapes and instances:

MOM_UNIT

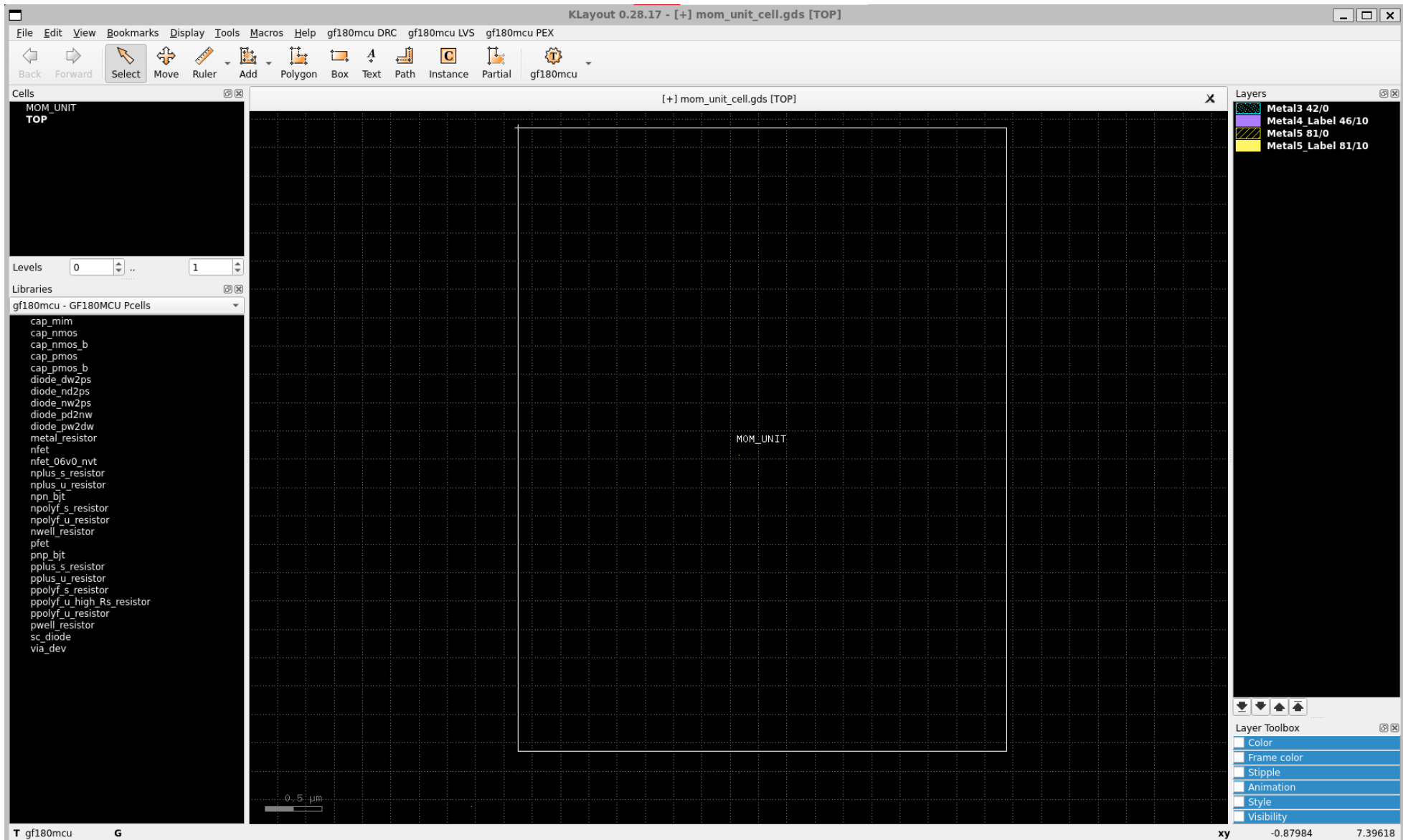
☒ Put origin relative to cell's bounding box at ...

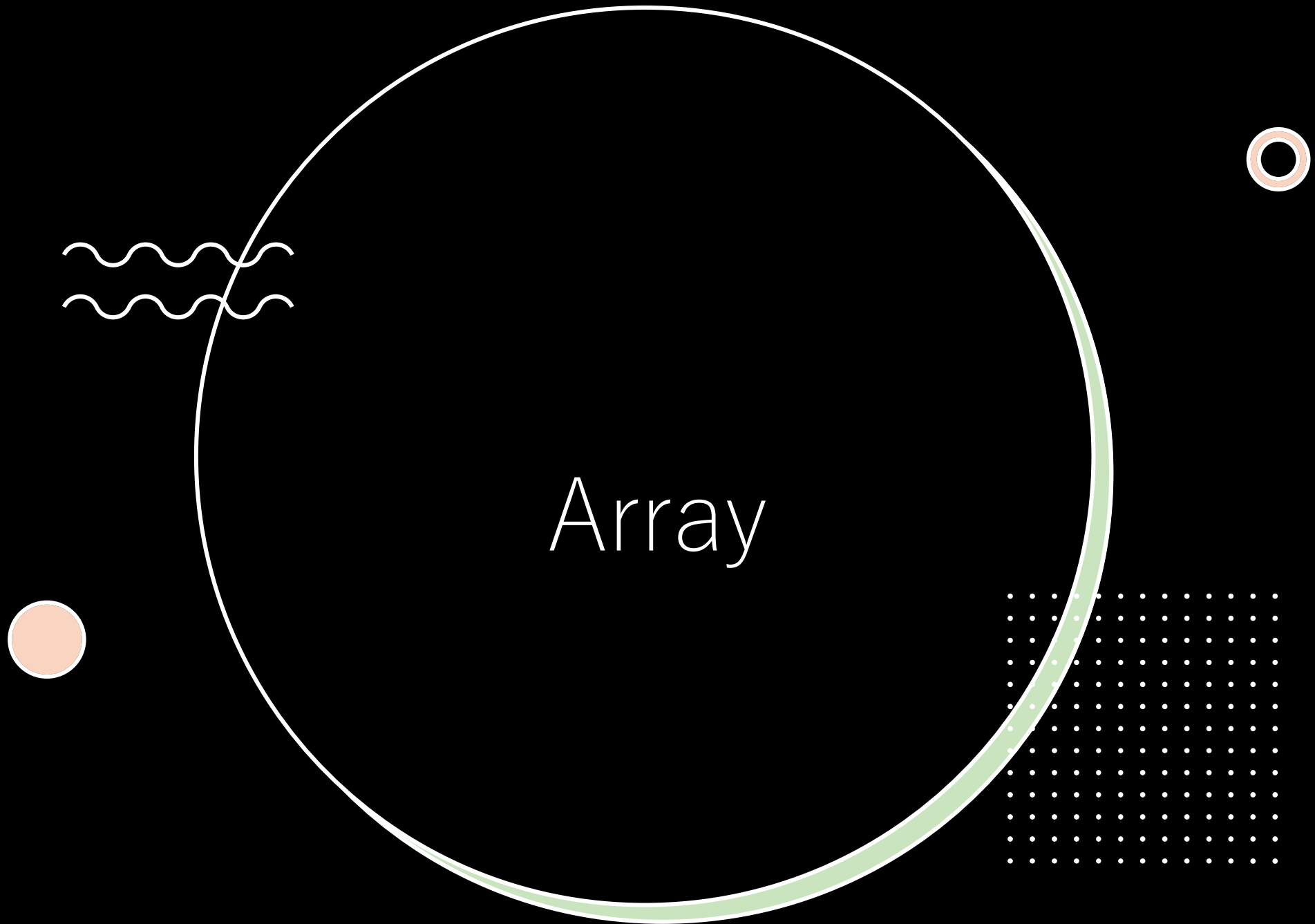


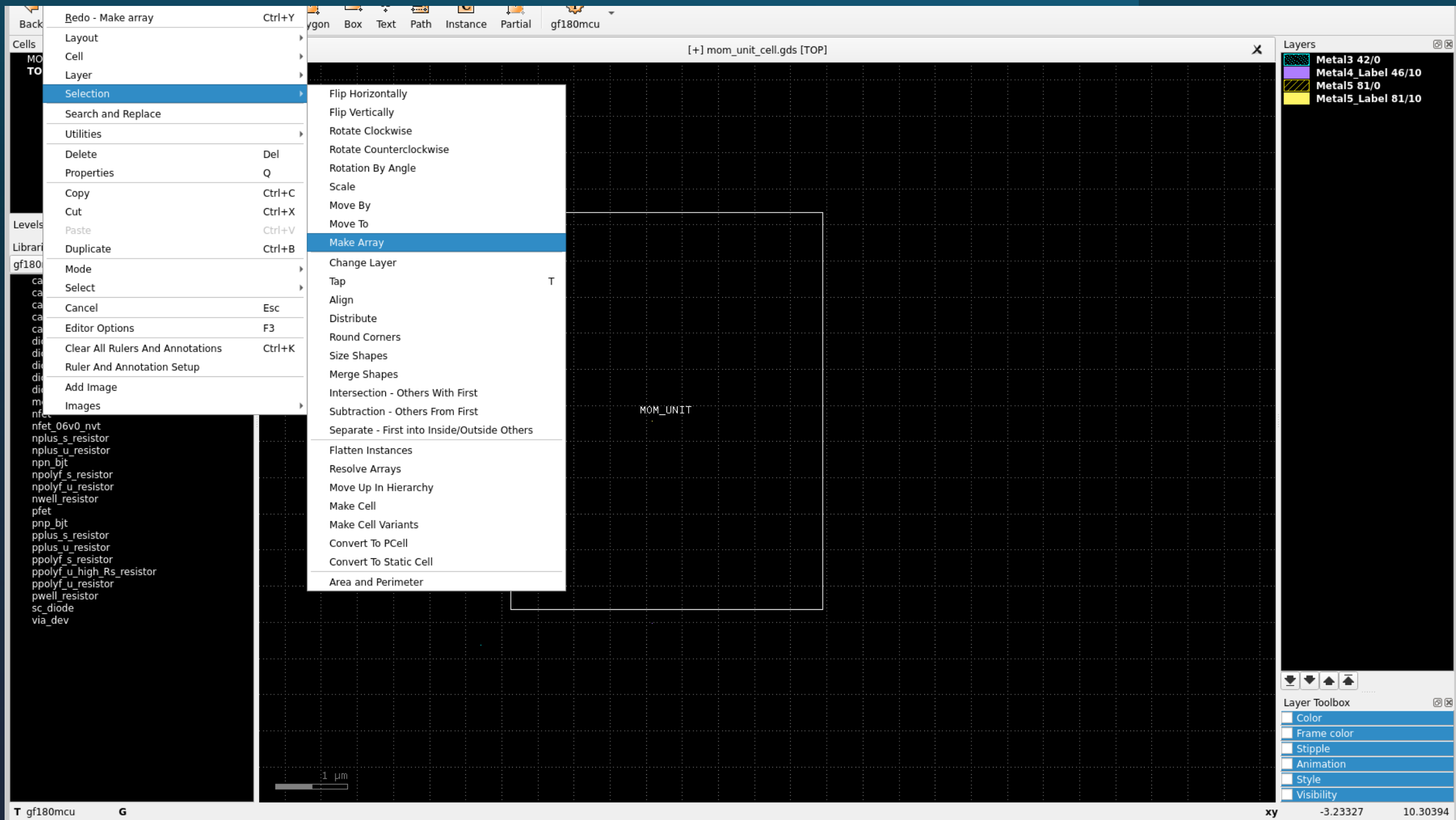
OK



Cancel









Make Array



The selection will be copied row * columns times. Each copy will be displaced by a vector given by the row vector times the row index and the column vector times the column index.

Rows And Columns

Rows/Columns	rows =	<input type="text" value="1"/>	columns =	<input type="text" value="10"/>
Row vector (x,y)	x =	<input type="text" value="0.00000"/>	y =	<input type="text" value="1.00000"/>
Column vector (x,y)	x =	<input type="text" value="4.00000"/>	y =	<input type="text" value="0.00000"/>

Warning: undo is available for this function only for small arrays (less than 1000 instances)



OK



Cancel

KLayout 0.28.17 - [+] mom_unit_cell.gds [TOP]

File Edit View Bookmarks Display Tools Macros Help gf180mcu DRC gf180mcu LVS gf180mcu PEX

Back Forward

Select

Move

Ruler

Add

Polygon

Box

Text

Path

Instance

Partial

gf180mcu

Cells

MOM_UNIT
TOP

Levels 0 .. 1

Libraries

gf180mcu - GF180MCU Pcells

cap_mim
cap_nmos
cap_nmos_b
cap_pmos
cap_pmos_b
diode_dw2ps
diode_nd2ps
diode_nw2ps
diode_pd2nw
diode_pw2dw
metal_resistor
nfet
nfet_06v0_nvt
nplus_s_resistor
nplus_u_resistor
npn_bjt
npolyf_s_resistor
npolyf_u_resistor
nwell_resistor
pfet
pnp_bjt
pplus_s_resistor
pplus_u_resistor
ppolyf_s_resistor
ppolyf_u_high_Rs_resistor
ppolyf_u_resistor
pwell_resistor
sc_diode
via_dev

[+] mom_unit_cell.gds [TOP]

5 μm

Layers

Metal3 42/0
Metal4_Label 46/10
Metal5 81/0
Metal5_Label 81/10

Layer Toolbox

☐ Color
☐ Frame color
☐ Stipple
☐ Animation
☐ Style
☐ Visibility

T gf180mcu G selected: instance("MOM_UNIT" r0 *1 -275,1735) in TOP@1 xy 21.47236 1.86716

KLayout 0.28.17 - [+] mom_unit_cell.gds [TOP]

File Edit View Bookmarks Display Tools Macros Help gf180mcu DRC gf180mcu LVS gf180mcu PEX

Back Forward Select Move Ruler Add Polygon Box Text Path Instance Partial gf180mcu

Cells

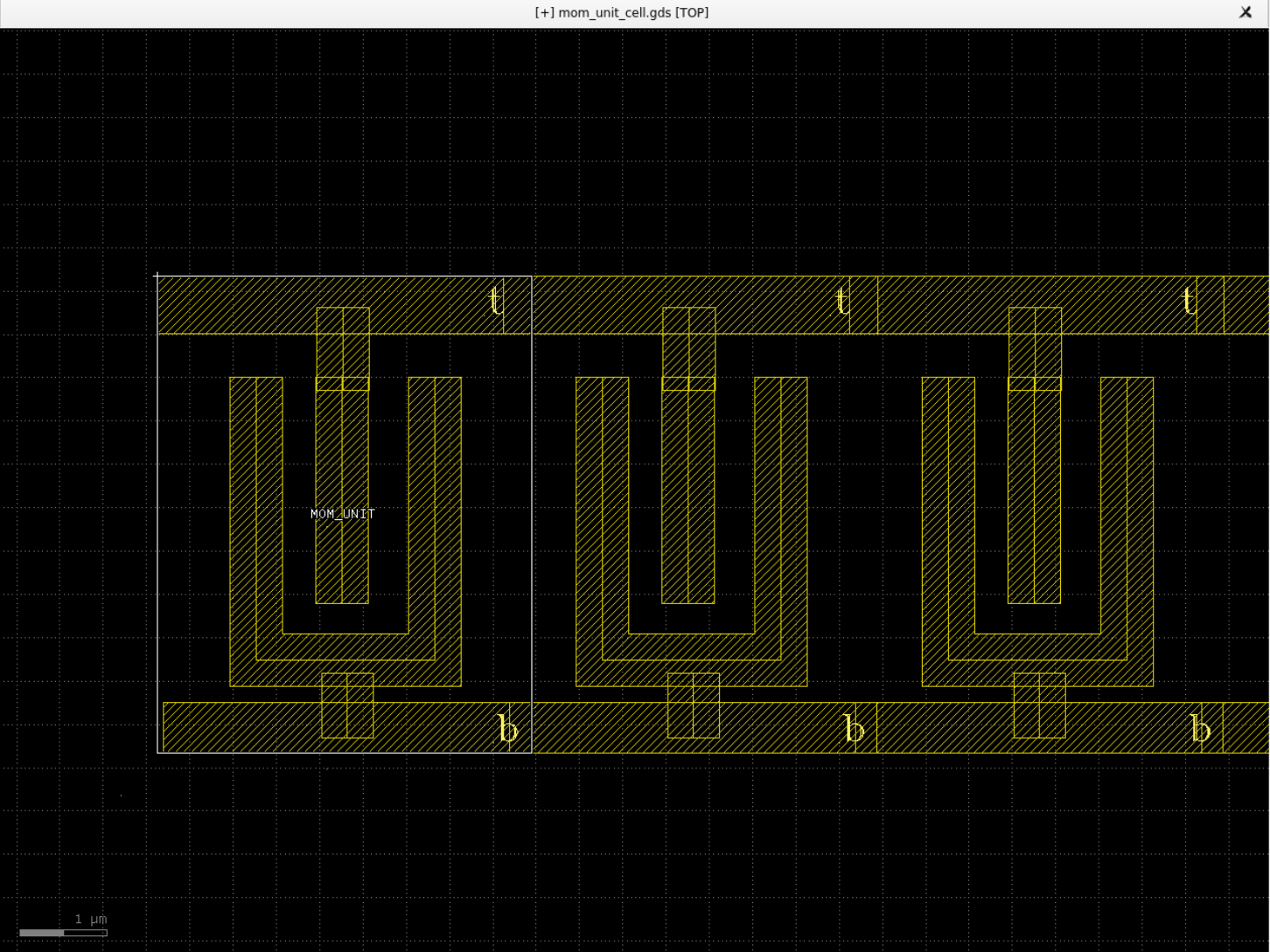
MOM_UNIT TOP

Levels 0 .. 2

Libraries gf180mcu - GF180MCU Pcells

cap_mim
cap_nmos
cap_nmos_b
cap_pmos
cap_pmos_b
diode_dw2ps
diode_nd2ps
diode_nw2ps
diode_pd2nw
diode_pw2dw
metal_resistor
nfet
nfet_06v0_nvt
nplus_s_resistor
nplus_u_resistor
nprn_bjt
npolyf_s_resistor
npolyf_u_resistor
nwell_resistor
pfet
pnp_bjt
pplus_s_resistor
pplus_u_resistor
ppolyf_s_resistor
ppolyf_u_high_Rs_resistor
ppolyf_u_resistor
pwell_resistor
sc_diode
via_dev

[+] mom_unit_cell.gds [TOP]



The image shows a GDS layout of a MOM_UNIT cell. The layout consists of three identical units arranged horizontally. Each unit is a rectangular block with a central vertical strip. The top and bottom horizontal strips are labeled 't' and 'b' respectively. The central vertical strip is labeled 'MOM_UNIT'. The layout is drawn on a grid. A scale bar at the bottom left indicates 1 μm.

Layers

Metal3 42/0
Metal4 Label 46/10
Metal5 81/0
Metal5_Label 81/10

Layer Toolbox

☐ Color
☐ Frame color
☐ Stipple
☐ Animation
☐ Style
☐ Visibility

T gf180mcu G selected: instance("MOM_UNIT" r0 *1 -275.1735) in TOP@1 xy 7.06228 4.66157