

# Introduction to the ISHI-KAI

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ISHI-KAI

<https://ishi-kai.org/>

Mail: [info@ishi-kai.org](mailto:info@ishi-kai.org)

# Agenda

- About the ISHI-KAI
- Activities of the ISHI-KAI

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- About the ISHI-KAI
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# What is the ISHI-KAI?



- The name was inspired by the society community (KAI is the society community in Japanese) that deals with open (democratised) ISHI (ISHI is stone in Japanese) = Silicon = Semiconductor (ASIC/LSI/IC) and connects various fields.

Community to support beginners  
(those outside the semiconductor industry)  
who want to make semiconductors.



- The policy for future activities is to revolutionise the semiconductor (ASIC/LSI/IC) field by involving people from other fields, and we will organise events such as hands-on seminars for very beginners for other fields and study groups with dense content for experts, and we will form teams to organise OpenMPW shuttles and globalChipathon challenges and participation in events such as the Maker Faire, so please do get in touch.

## Making 'I have made it'

To create a "Make: Movement (open hardware)" level big wave in open source semiconductors.

- Companies that started up in Make: Era
  - From software companies and others with no connection to hardware, something like an 'in-house Make:Development Department' was set up and derived from it.
    - 'Where have you acquired your knowledge?'
      - Open hardware communities in the Make:
    - 'A coherent number of technicians were created'
      - Any company can now do business involving hardware.
    - 'Make it work as a business'
      - 'Intermediaries with knowledge of both the industry and business of the party wishing to enter and the semiconductor industry' are needed.



# Grand Design of ISHI-KAI

I want to develop new sectors but don't know how to do it

## Chip in with Everyone's Experience!

Want to convert to ASIC (LSI) but have no information

### Current state of the ASIC (LSI) industry (stagnation)

- Cannot Share because of NDAs.
- Cutting Edge Requires Big Money
  - Young people are not coming in.

### Current situation in other industries (sense of limitation)

- Demand for high speed, compactness and power saving
  - Limitations with generic chips + software

### Significance of the community

- Re-use of results possible; Do it With Others mentality
- Advantages of Japan: geographical location makes it physically easy to get together and hold study groups and camps.

Everything is open!

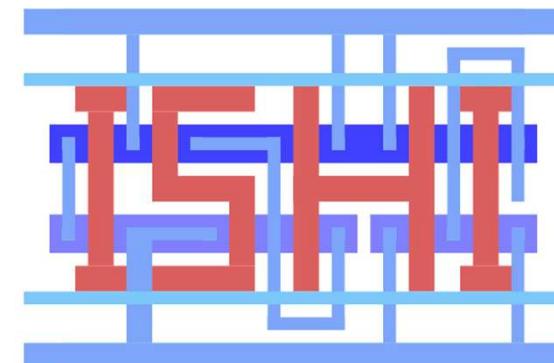
### Significance of ISHI-KAI

- Expectations for unprecedented research and development through the integration of knowledge from other (multi)disciplines

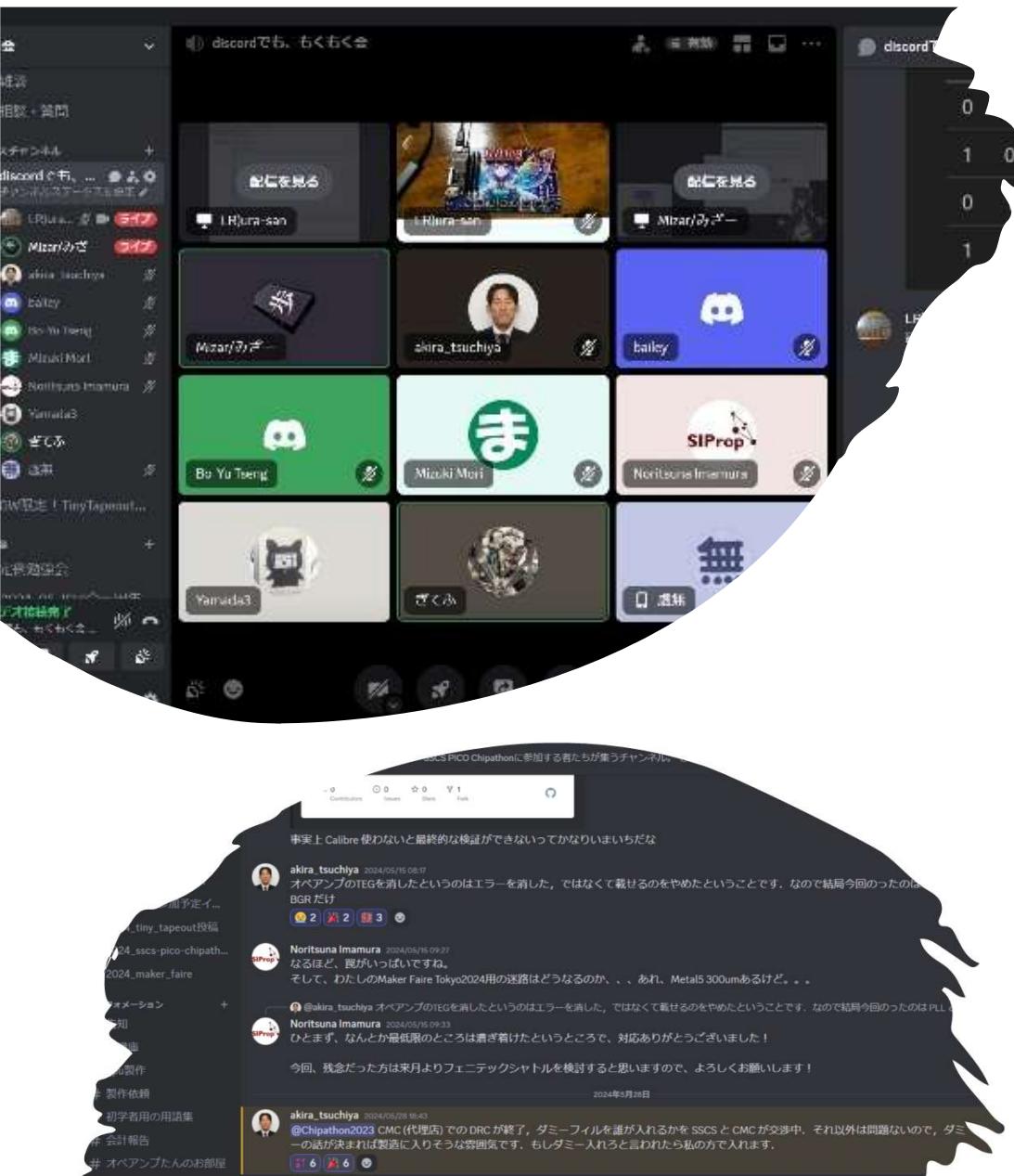
# Information on the ISHI-KAI

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- Number of members
  - 350 or more
- Homepage
  - <https://ishi-kai.org/>
- Active on Discord
  - <https://discord.gg/RwAWF5mZSR>
- Event announcements (e.g., workshops)
  - <https://ishikai.connpass.com/>
  - About 20-50 people attend at any given time



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- Activities of the ISHI-KAI
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# Location: Discord

- Base of operations on the Internet
  - Using Discord, a chat application
  - Equivalent to an office in a typical organization
- Main Activities
  - Discussion by each channel on the theme
  - Regular Mokumoku-kai using video chat
    - Mokumoku-kai: Meetings where everyone gathers in one place to develop their own themes in silence.



## First Event

- ISHI-KAI was established with the First Hands-On Seminar held on May 7, 2023.
  - 13 members



## Regular Events

- One of the activities for external
- Once or twice a month, we hold study sessions and hands-on seminars for beginners by inviting guest lecturers on the theme.

〒155-0031 東京都世田谷区北沢2丁目3-3 第二友和ビル

**ISHI**

2024/08/24 (土) 21:00~ 7/10  
2024年夏休み特別イベント「TinyTapeoutハンズオン」勉強会  
Noritsuna Imamura  
(場所未定)

**ISHI**

2024/08/11 (日) 13:00~ 47/71  
2024年08月イベント：初めての半導体設計・製造体験 for ISHI OpenMPW  
Noritsuna Imamura 他  
東京都渋谷区道玄坂1丁目2番3号 渋谷クラス

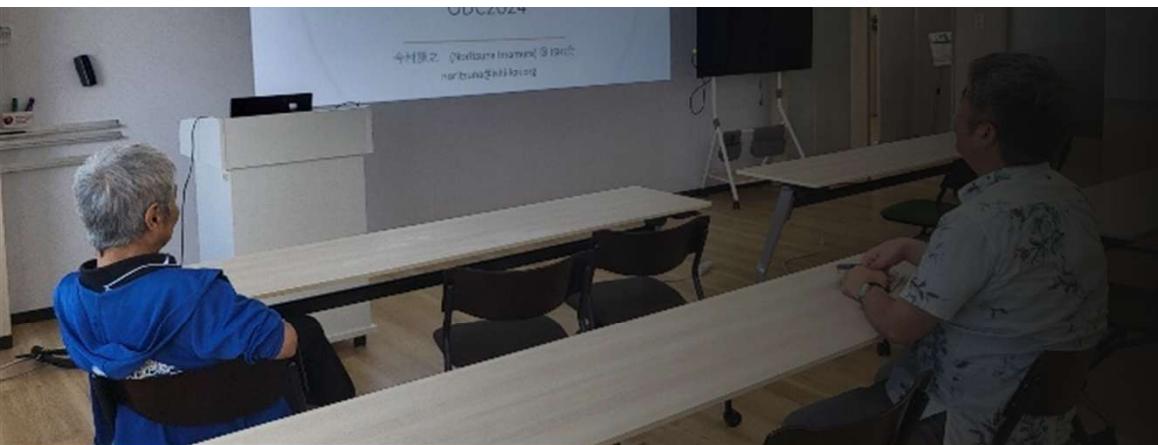
**ISHI**

2024/08/04 (日) 13:00~ 8/20  
ゆるゆるイベント：フェニックスシャトル最終サポート雑談会  
Noritsuna Imamura 他



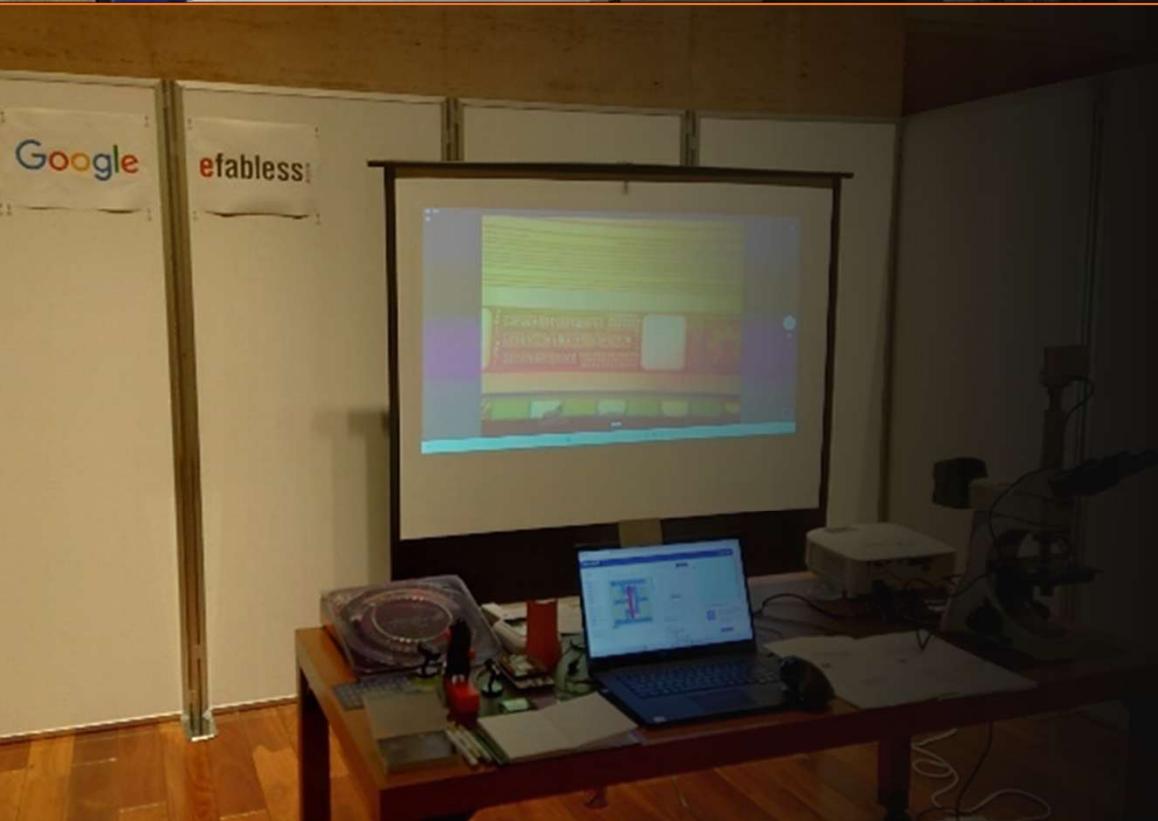
## Exhibition: Maker Faire

- Exhibit at Maker Faire Tokyo 2023



# Exhibition

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- Community Events/Exhibitions
  - Industry Events/Exhibitions



することができます。

## 【A - F】

### Analog Hard IP (Design Knowledge)

- AFE : Analog Front-End の略。センサー等のアナログ出力信号をデジタル信号へ変換するアナログ回路を指す。一般には、アンプやA/Dコンバータ、フィルタなどのアナログ回路を指すことが多いが、高速シリアル通信向けのクロックが重畠された小振幅信号やPAM(Pulse Amplitude Modulation)信号に変調された信号をデジタル信号に復調するミックスドシグナル回路もAFEと呼ぶことがある。SoC内部にAFEを搭載する場合と、SoCとは別チップでAFEを構成する場合がある。
- BGR : BandGap voltage Referenceの略。正の温度特性を持つPN接合を流れる電流を、負の温度特性を持つ抵抗に流することで、温度によらずに一定の電圧を発生する、基準電圧回路。SiのBandGap(1.26V)に近い電圧を出力する。回路安定点が2つあり適切なスタートアップ回路が必須である。
- CDR : Clock and Data Recovery の略。データとクロックを重畠させたシリアル信号から、受信側でクロック成分とデータ成分を切り分ける回路を指す。送信側では、データに含まれるエッジの場所や数を保証してコード変換(代表的な例として8b10bエンコードがある)し、受信側では信号に含まれるクロック成分をPLLで同期することでクロックを抽出、抽出したクロックでデータを復調する。
- DLL : Delay Locked Loopの略。外部クロックとインバーター（遅延をアナログ的に制御する場合と、量子化された遅延をデジタル的に選択する場合がある）の遅延信号との間で位相をロックすることで、負の遅延を持ったクロック信号を発生して、セットアップ・ホールドのタイミングマージンを改善できる。同様に外部クロックに対して複数の位相を持った多層クロックを発生したり、数多くの応用回路が提案されている。PLLと比較して、外部クロックの位相の変化に瞬時に追随できる利点がある一方で、PLLの様に、任意の遅倍クロックを発生することは出来ない。
- LDO : Low Dropout Regulator の略。ディスクリート部品の三端子レギュレーターの事。チップ内部で使用する電源を、外部から入力された電源から降圧する回路。高電圧側(外部)と降圧電圧(内部)の間に可変抵抗(=トランジスタ)を挿入して、その抵抗率を調整することで、出力電圧を調整する。

## Other Cooperation

### VLSI.jp

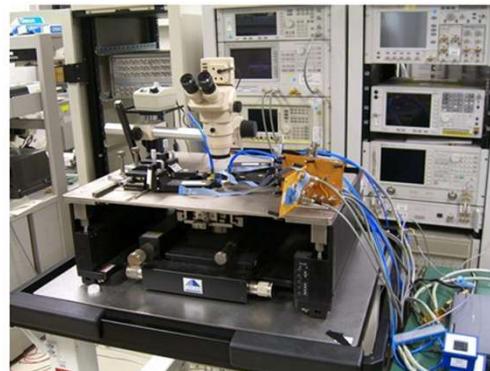
- Documentation of various hands-on findings related to open source silicon
- Production of "Glossary of Terms Used in Semiconductor Design" for beginners of semiconductor design.

# Shuttle Submissions

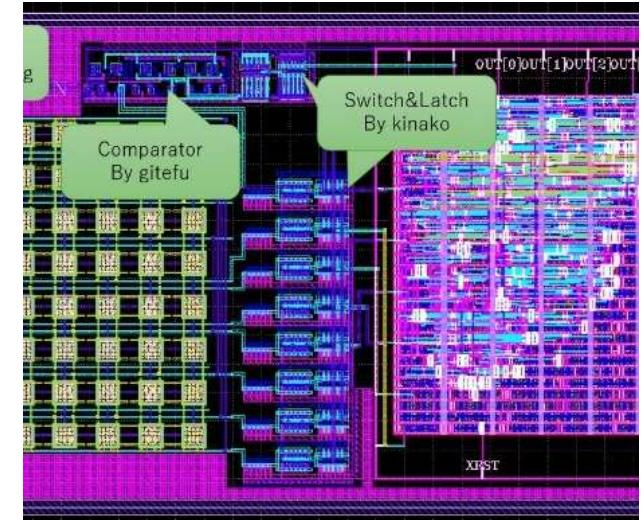
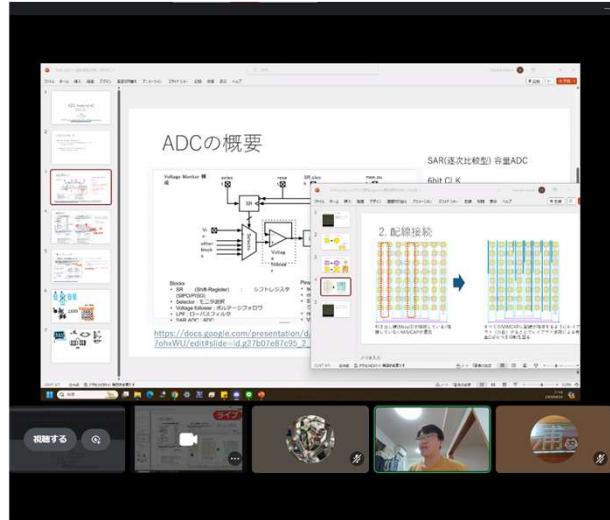
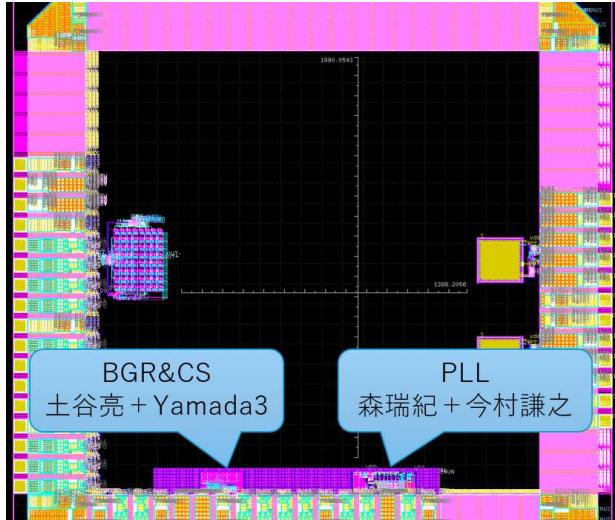


# Chipathon2023

Prof. Tsuchiya called for  
the formation of a  
Japanese team



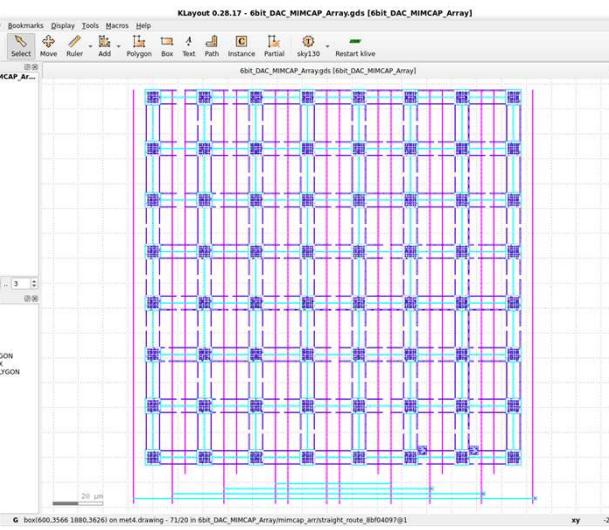
# Chipathon2023 Results



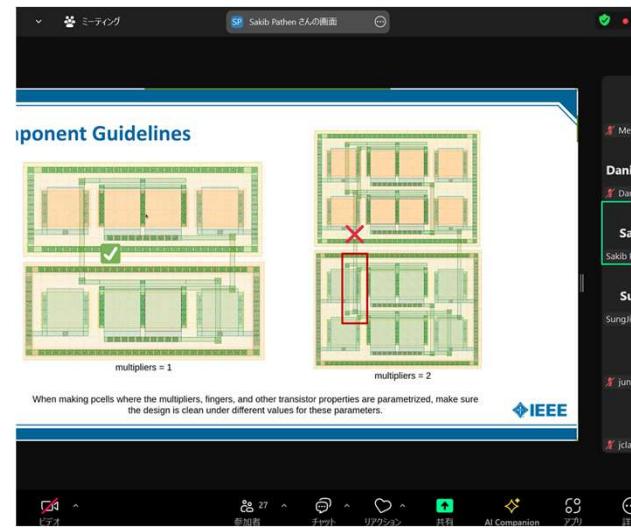
- BGR+CS Group
  - Prof.Tsuchiya & Yamada3
- PLL Group
  - Mori & Noritsuna
- ADC Group
  - Led by Prof. Kuboki, 4 young CS undergraduates and young people working in hardware companies

# Chipathon2024 Result : SaltyChip Team

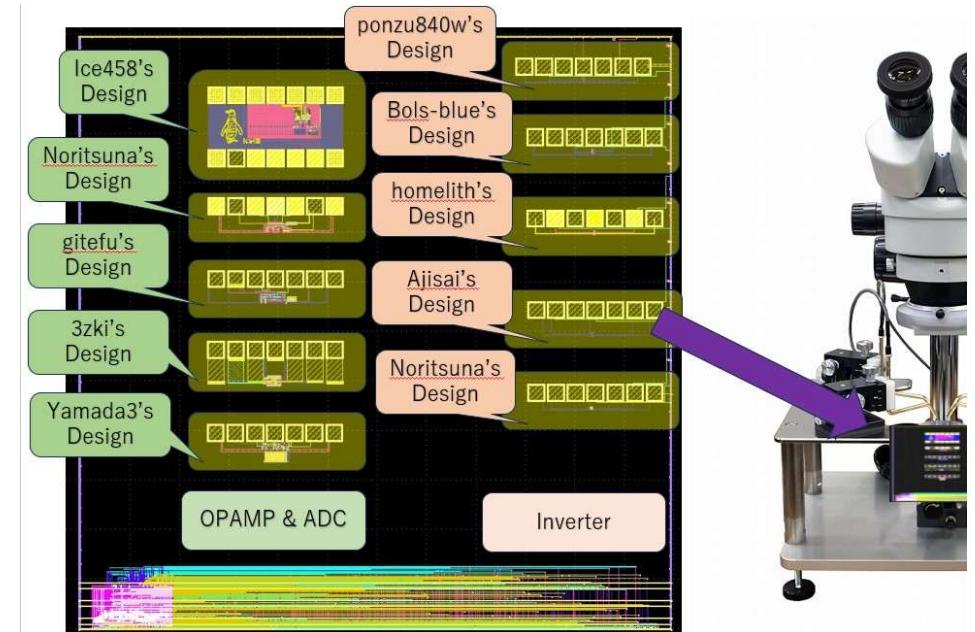
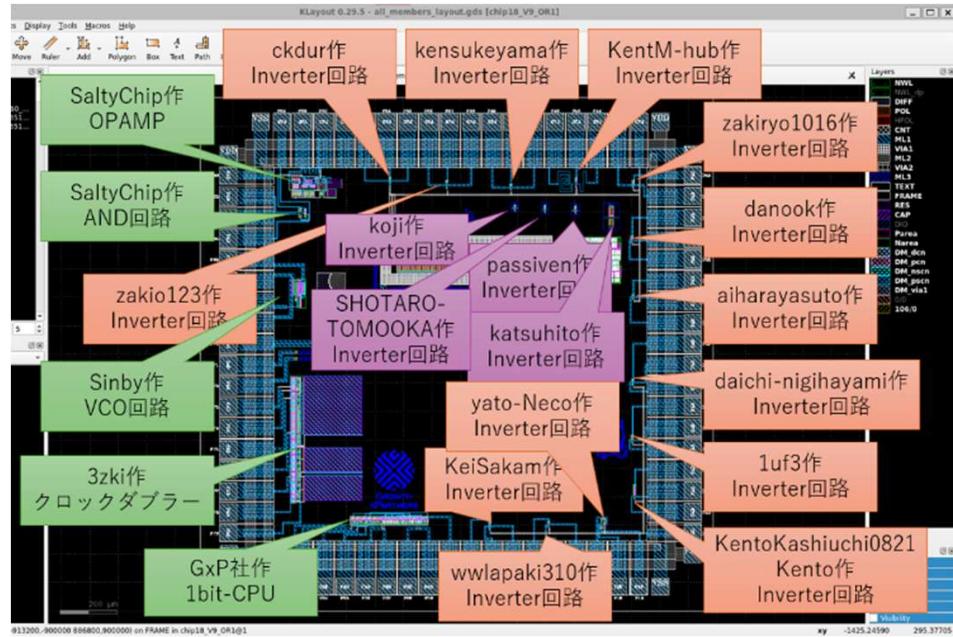
- DAC
  - Submitted!



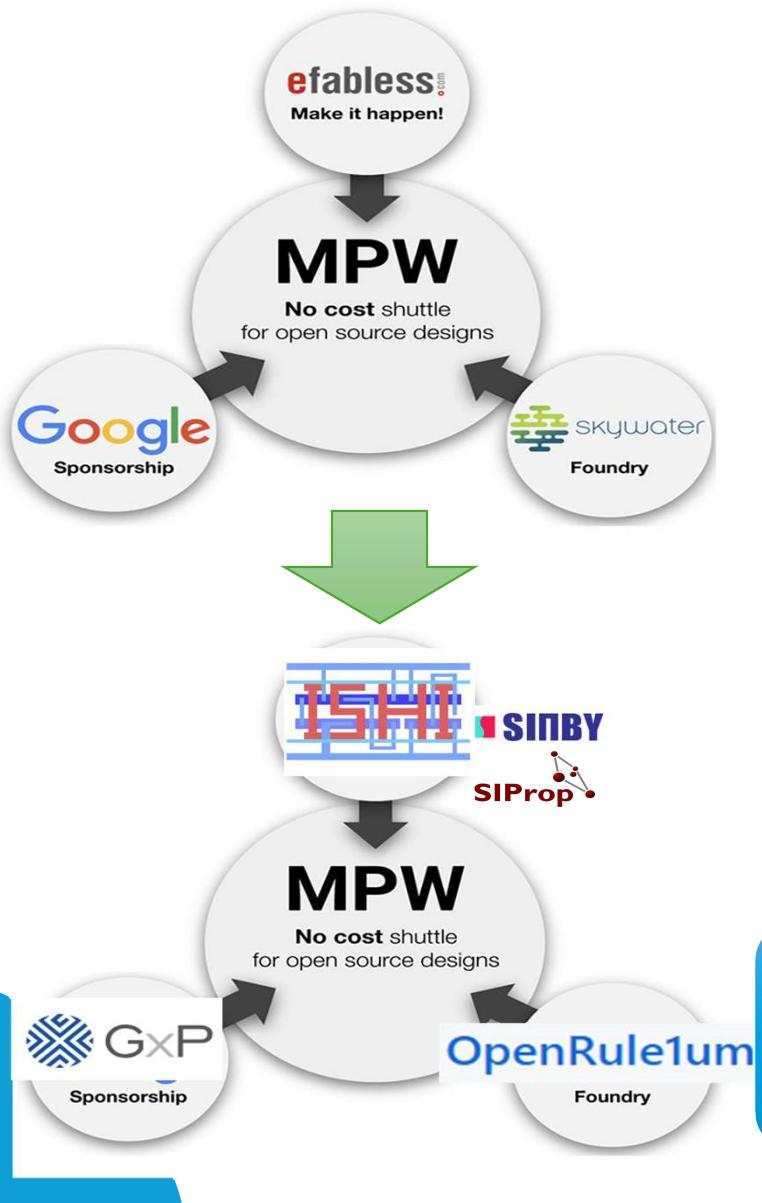
```
chip > mimcap.py
2024-11-12 05:18:53.808 | INFO      | gdsfactory.pdk:activate:337
- 'sky130' PDK is now active
/usr/bin/miniconda3/lib/python3.10/site-packages/gdsfactory/show.py:40: UserWarning: Unnamed cells, 1 in '6bit_DAC_MIMCAP_Array'
gdspath = component.write_gds(
Loaded /tmp/gdsfactory/6bit_DAC_MIMCAP_Array.gds
2024-11-12 05:19:06.503 | INFO      | gdsfactory.show:55 - M
essage from klive: {"version": "0.3.3", "klayout_version": "0.28.17", "type": "open", "file": "/tmp/gdsfactory/6bit_DAC_MIMCAP_Array.gds"}
root > Klayout 0.28.17 - 6bit_DAC_MIMCAP_Array.gds [6bit_DAC_MIMCAP_Array]
iprof File Edit View Bookmarks Display Icons Status Help
chip > sky130
root >
```



# Sharing a Shuttle



- Support for multiple users to share a shuttle
  - Hands-on seminars for beginners
  - Team Submissions



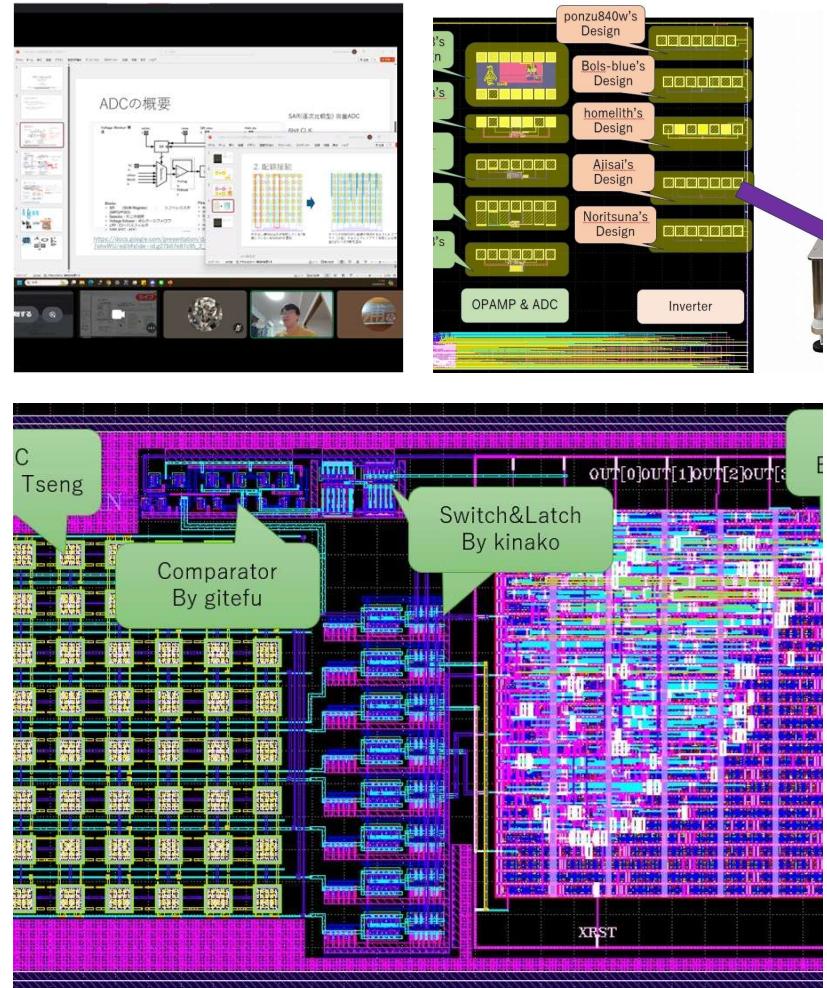
# ISHI-KAI's OpenMPW!

- Community
  - eFabless ⇔ ISHI-KAI
- Sponsor
  - Google ⇔ GxP
- Fab
  - SkywaterPDK ⇔ OpenRule1umPDK

Hosting as ISHI-KAI's OpenMPW-PTC06-1

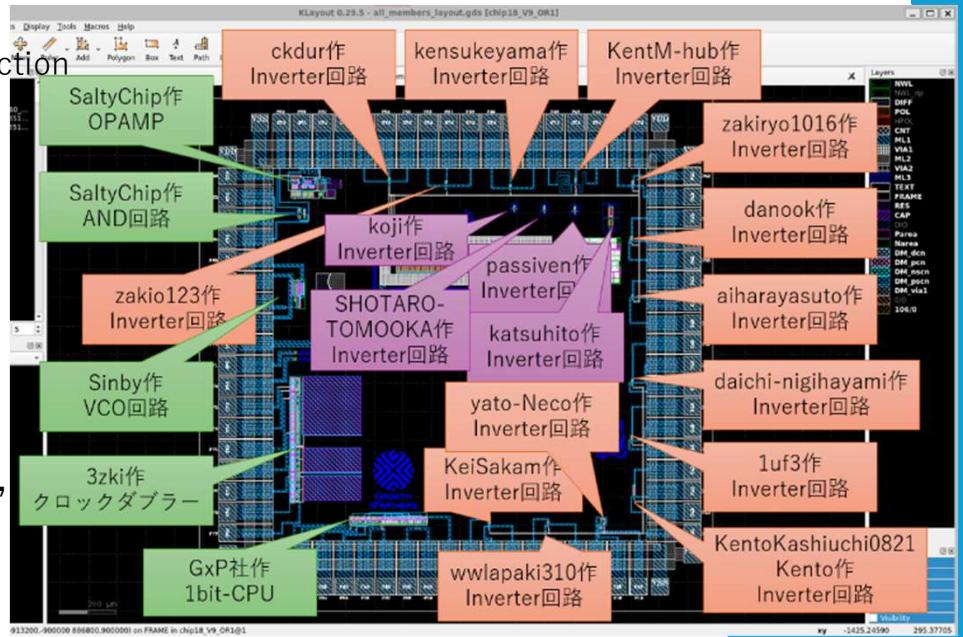
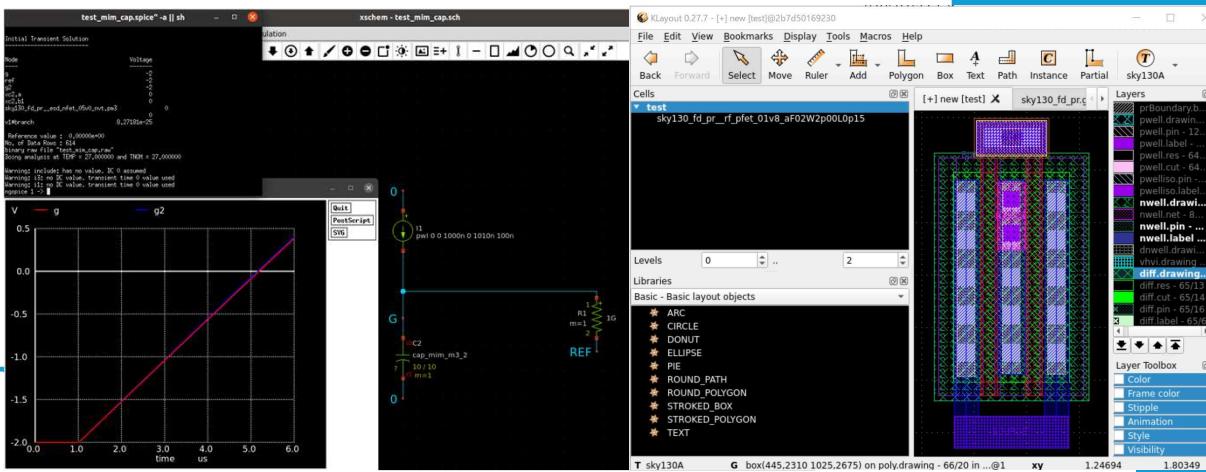
# Shuttle: ISHI-KAI Share Results

- 2023/12
  - OpenMPW GF-1
    - [https://github.com/ishi-kai/ISHI-KAI\\_Multiple\\_Projects\\_OpenGFMPW-1/](https://github.com/ishi-kai/ISHI-KAI_Multiple_Projects_OpenGFMPW-1/)
- 2024/05
  - Chipathon2023
    - [https://github.com/ishi-kai/Chipathon2023\\_ADC/tree/main/submit\\_version](https://github.com/ishi-kai/Chipathon2023_ADC/tree/main/submit_version)
    - <https://github.com/atuchiya/DC23-LTC2/tree/japan-test/TOP>
- 2024/08
  - ISHI-KAI's OpenMPW PTC06-1(Phenitec)
    - [https://github.com/ishi-kai/ISHI-KAI\\_Multiple\\_Projects\\_OpenMPW\\_PTC06-1](https://github.com/ishi-kai/ISHI-KAI_Multiple_Projects_OpenMPW_PTC06-1)
- 2024/10
  - ISHI-KAI's OpenMPW TR10-1(Tokairika)
    - [https://github.com/ishi-kai/ISHI-KAI\\_Multiple\\_Projects\\_OpenMPW\\_TR10-1](https://github.com/ishi-kai/ISHI-KAI_Multiple_Projects_OpenMPW_TR10-1)
- 2024/12
  - ISHI-KAI's OpenMPW MF20-1(minimalfab)
    - [https://github.com/ishi-kai/ISHI-KAI\\_Multiple\\_Projects\\_OpenMPW\\_MF20-1](https://github.com/ishi-kai/ISHI-KAI_Multiple_Projects_OpenMPW_MF20-1)



# Hands-on Seminar

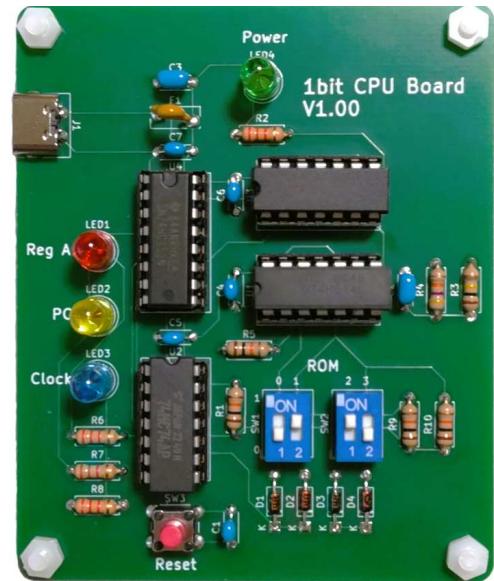
- Learn all the basics of semiconductor design from zero knowledge!
  - Hands-on seminar on the simplest inverter circuit
    - Circuit Design with Xschem
      - Working with combinations of transistors to achieve a function
    - Circuit Characteristics Simulation with NGspice
      - Work to verify that the above circuits work properly
    - Layout by klayout
      - Layout of transistors on actual semiconductors
  - Maker's voice
    - The chip design experience was very technically stimulating.
    - Semiconductors were completely unknown to me, but understanding them gave me new insights.



# Hands-on Seminar: Target

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- The goal is to provide the first "hands-on" semiconductor design experience
  - Increase the number of semiconductor designers within software and hardware companies
- Motivation of Makers
  - I've been hearing a lot about semiconductors, and I'd like to know more about them specifically!
    - Basic knowledge of semiconductors
    - Semiconductor factory process details
  - I want to know more about how computers work!
    - Perhaps because even the compiler level has been covered up, a return to a more principled approach is taking place.

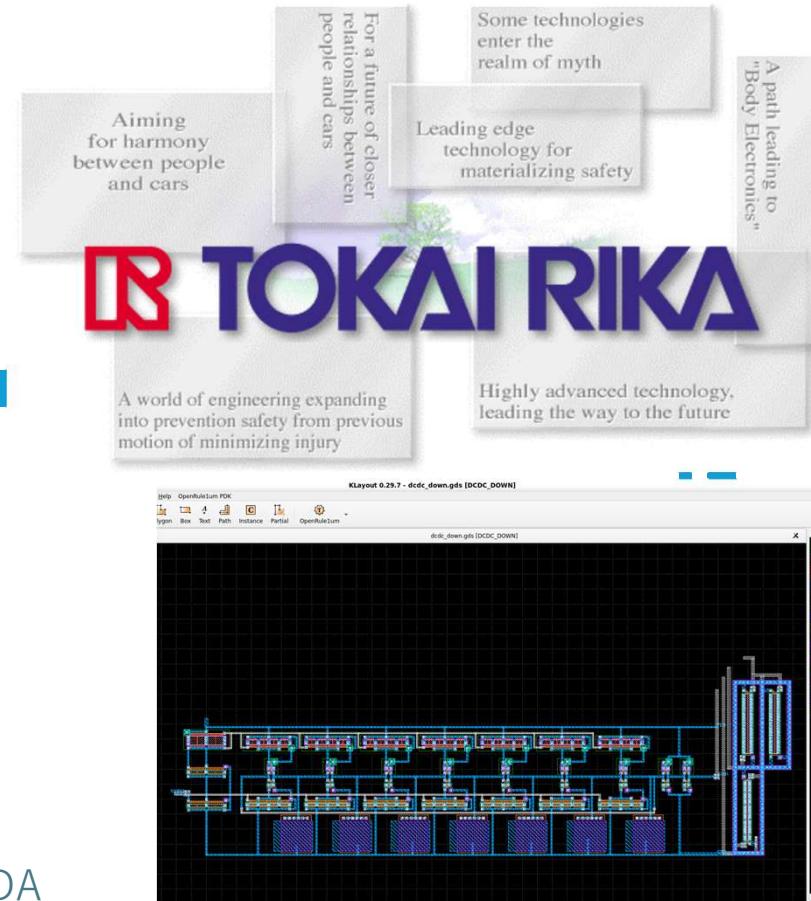


# Team Submissions

- Content
  - Have multiple people create one theme (circuit)
    - Leader
      - Have an intermediate or advanced person lead the team.
    - Members
      - Beginners design and layout with the help of a leader.
- Target
  - Leader
    - Gain the ability to serve as a bridge resource for software and hardware companies seeking to create their own chips
  - Members
    - Soloing is difficult unless you are at least intermediate level, but the ISHI-KAI's main demographic is beginners. This makes it possible for many people to participate.

# Ex: Tokairika Shuttle

- Details of implementation
  - Create "two teams" of two types of DCDC,  
a boosting DCDC and a bucking DCDC.
  - 5V->12V, 12V->5V
- Rules
  - Use OpenRule1um
    - [https://github.com/ishi-kai/OpenRule1umPDK\\_setupEDA](https://github.com/ishi-kai/OpenRule1umPDK_setupEDA)
  - Max size is "1000um(1mm) x 1000um(1mm)"
  - Pin count is "7-pin".
    - VDD, input voltage pin, and output voltage pin are required.
      - You are free to use the later 4 pins however you like.



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