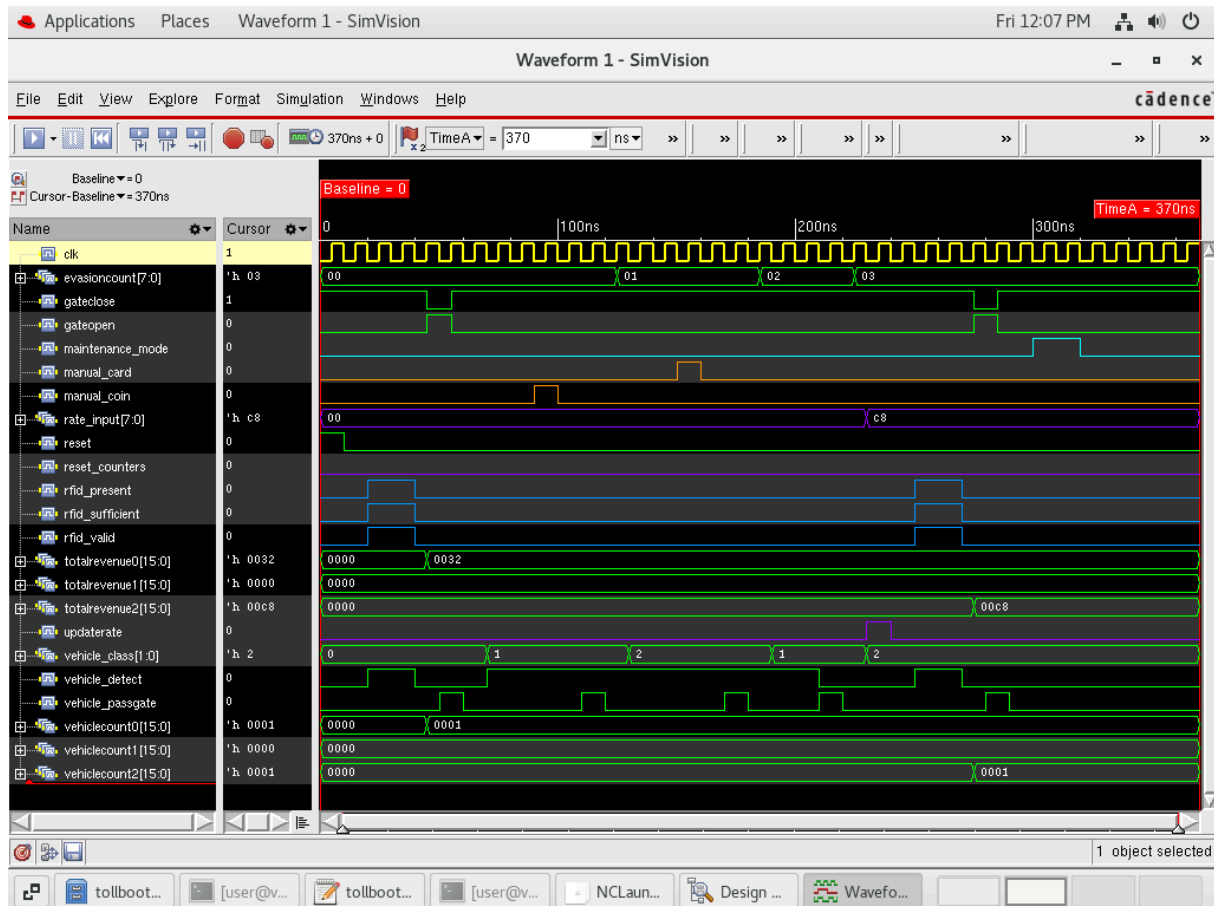
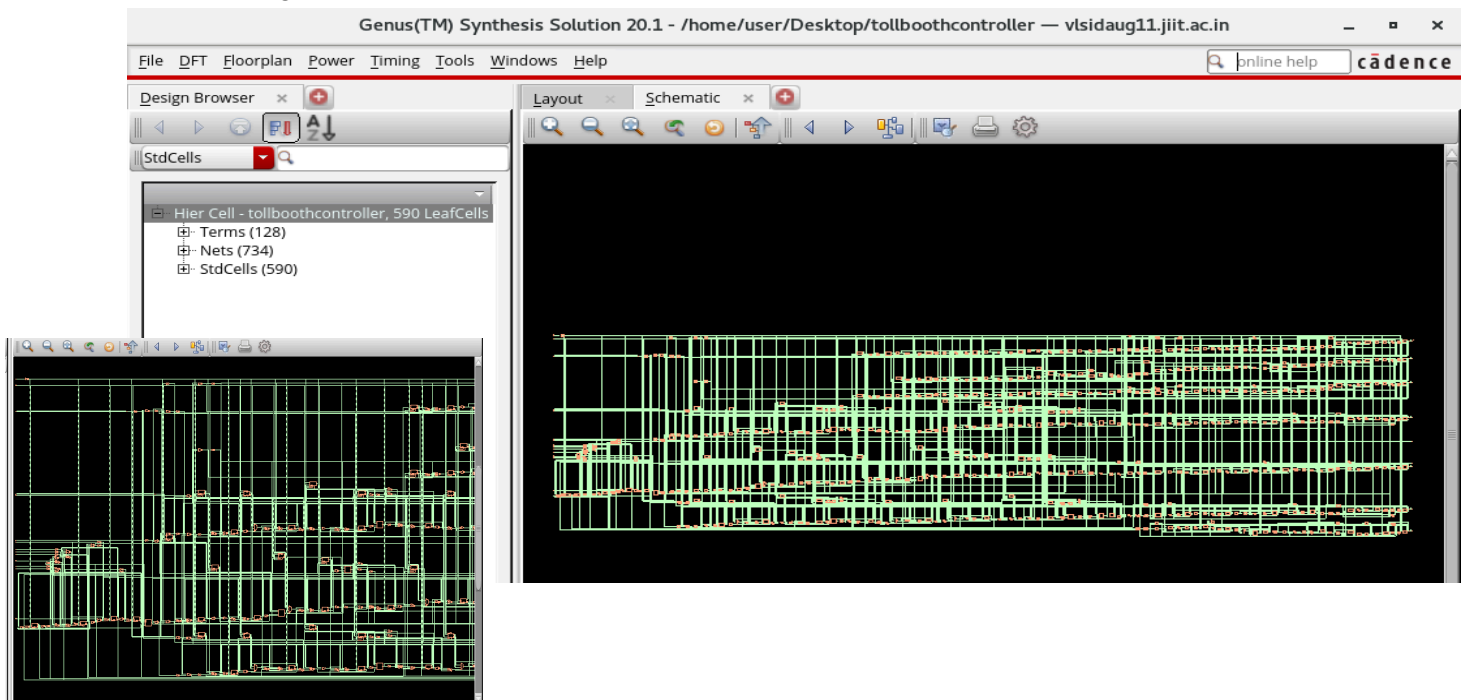


## ISHI PROJECT- TOLL BOOTH CONTROLLER

### WAVEFORM

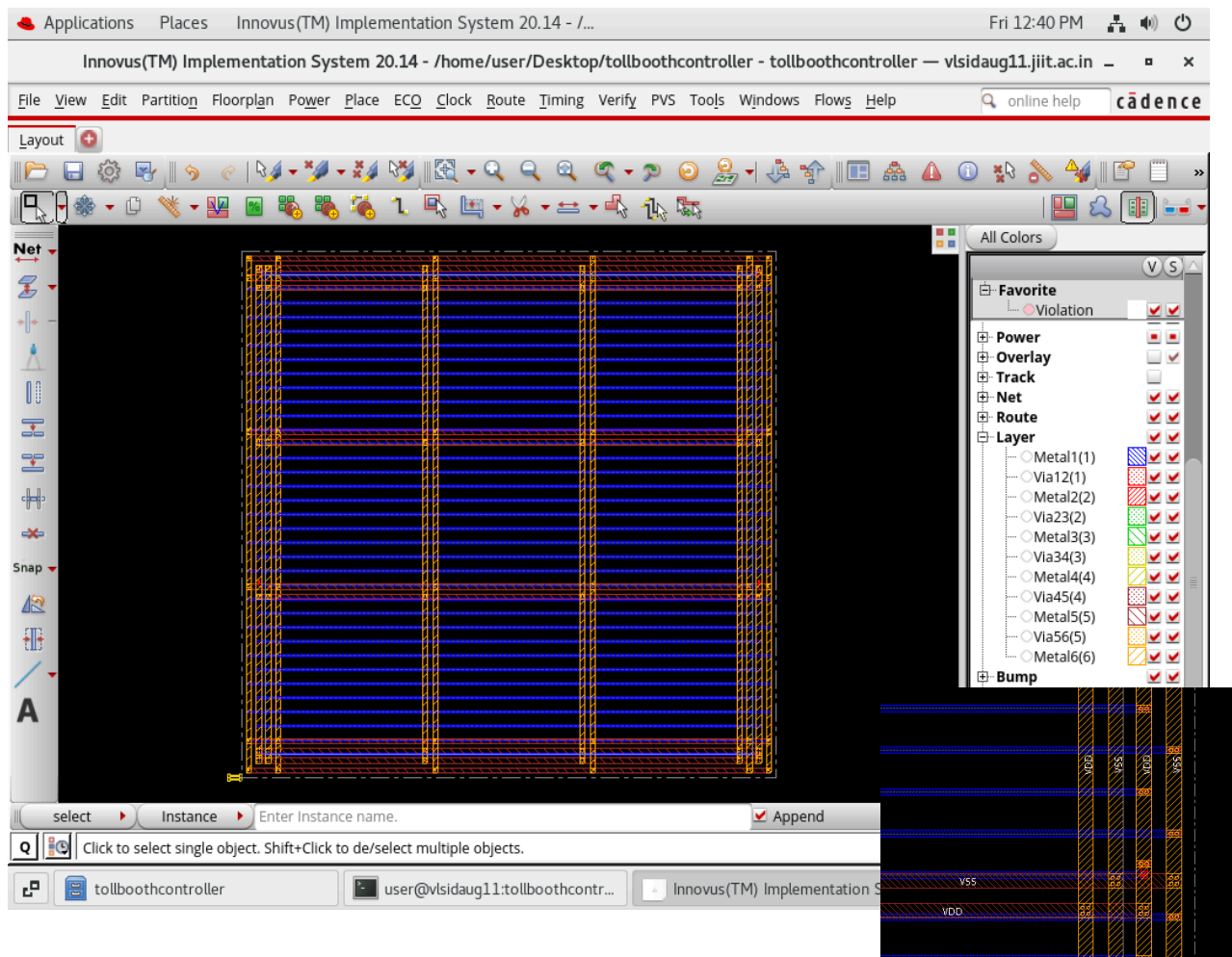


### Schematic- genus

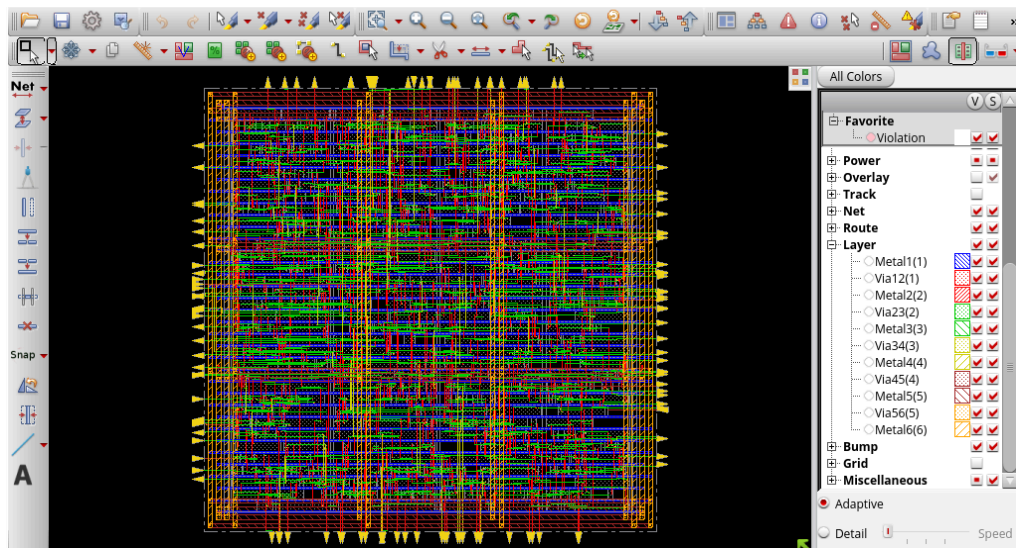


# FLOORPLAN

## SPECIAL ROUTE



## Placed (Pre Optimising)



Applications Places Terminal

user@vlsidaug11:tollboothcontroller

File Edit View Search Terminal Help

Total Power

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.154	0.02003	7.524e-05	0.1741	72.29
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.04034	0.02631	7.104e-05	0.06672	27.71
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	0.1943	0.04634	0.0001463	0.2408	100

Rail

Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
VDD	0.9	0.1943	0.04634	0.0001463	0.2408

Power Distribution Summary:

- \* Highest Average Power: g19060 (INVXL): 0.004112
- \* Highest Leakage Power: g18994 (CLKIN(X20)): 6.569e-07
- \* Total Cap: 5.1297e-12 F
- \* Total instances in design: 590
- \* Total instances in design with no power: 0
- \* Total instances in design with no activity: 0
- \* Total Fillers and Decap: 0

tollboothcontroller user@vlsidaug11:tollboothcontr... Innovus(TM) Impl

Applications Places Terminal

user@vlsidaug11:tollboot

File Edit View Search Terminal Help

timeDesign Summary

Setup views included:  
WORST

Setup mode	all	reg2reg	default
WNS (ns):	-0.363	5.957	-0.363
TNS (ns):	-0.701	0.000	-0.701
Violating Paths:	2	0	2
All Paths:	456	170	411

DRVs	Real	Total
Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	1 (1)	1 (1)
max_tran	0 (0)	0 (0)
max_fanout	0 (0)	0 (0)
max_length	0 (0)	0 (0)

Density: 84.400%

Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports

Total CPU time: 0.21 sec

Total Real time: 1.0 sec

Total Memory Usage: 1512.832031 Mbytes

\*\*\* timeDesign #1 [finish] : cpu/real = 0:00:00.2/0:00:00.9 (0.2), totSession cp

innovus l> report\_area

Hinst Name	Module Name	Inst Count	Total Area
tollboothcontroller		590	23863.594

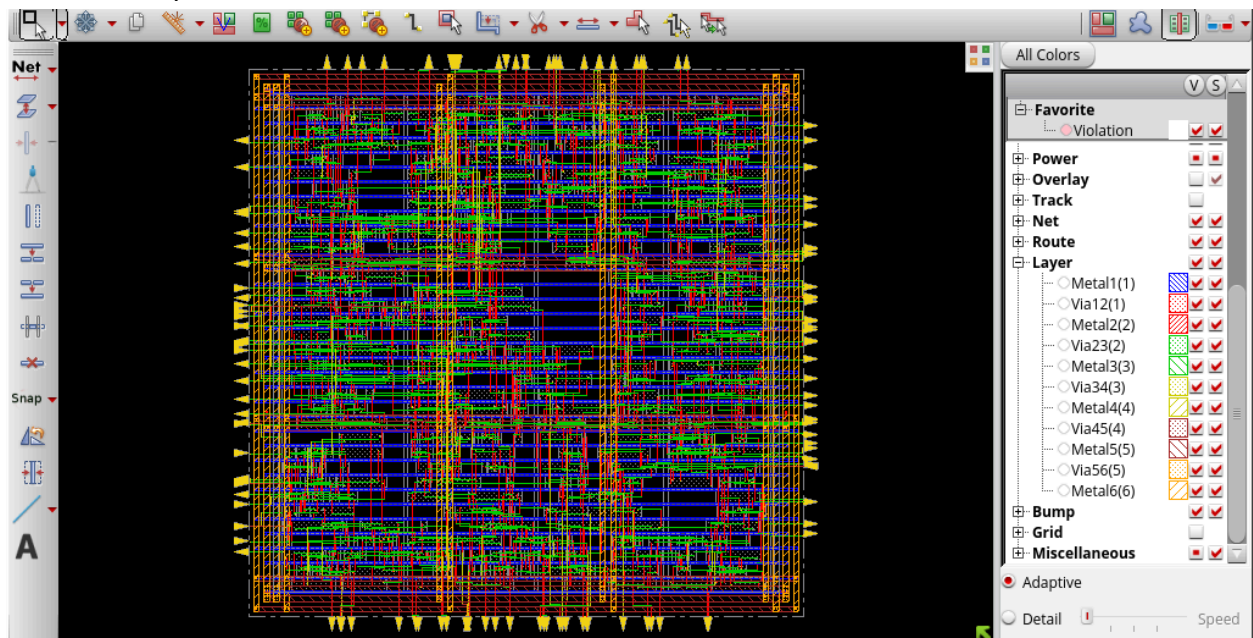
innovus z>

tollboothcontroller user@vlsidaug11:tollboothcontr...

Area: 23863.594

Power: 0.2408

## Placed and optimised



Applications Places Terminal

user@vlsidaug11:tollboothcontroller

File Edit View Search Terminal Help

Total Power

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.1356	0.01163	3.848e-05	0.1472	79.18
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.01895	0.01973	3.472e-05	0.03871	20.82
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
<b>Total</b>	<b>0.1545</b>	<b>0.03136</b>	<b>7.321e-05</b>	<b>0.186</b>	<b>100</b>

Rail

Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
VDD	0.9	0.1545	0.03136	7.321e-05	0.186

Power Distribution Summary:

Power	FE_OFCL_n_593 (BUF2):	0.001428
Highest Average Power:	tollrates2_reg[6] (SDFFRHX1):	3.722e-07
Total Cap:	3.92635e-12 F	
Total instances in design:	593	
Total instances in design with no power:	0	
Total instances in design with no activity:	0	
Total Fillers and Decap:	0	

tollboothcontroller user@vlsidaug11:tollboothcontr... Innovus(TM) Implemer

Applications Places Terminal

user@vlsidaug11:tollboothco

File Edit View Search Terminal Help

timeDesign Summary

Setup views included:  
WORST

Setup mode	all	reg2reg	default
WNS (ns):	5.274	5.274	6.436
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	456	170	411

DRVs	Real		Total	
	Nr nets(terms)	Worst Vio	Nr nets(terms)	
max_cap	0 (0)	0.000	0 (0)	
max_tran	0 (0)	0.000	0 (0)	
max_fanout	0 (0)	0	0 (0)	
max_length	0 (0)	0	0 (0)	

Density: 61.012%

Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports

Total CPU time: 0.15 sec

Total Real time: 1.0 sec

Total Memory Usage: 1552.601562 Mbytes

\*\*\* timeDesign #2 [finish] : cpu/real = 0:00:00.2/0:00:00.9 (0.2), totSession cpu/r

innovus 3> report\_area

Hinst Name	Module Name	Inst Count	Total Area
tollboothcontroller		593	17250.710

innovus 4>

tollboothcontroller user@vlsidaug11:tollboothcontr... Inn

Area: 17250.710

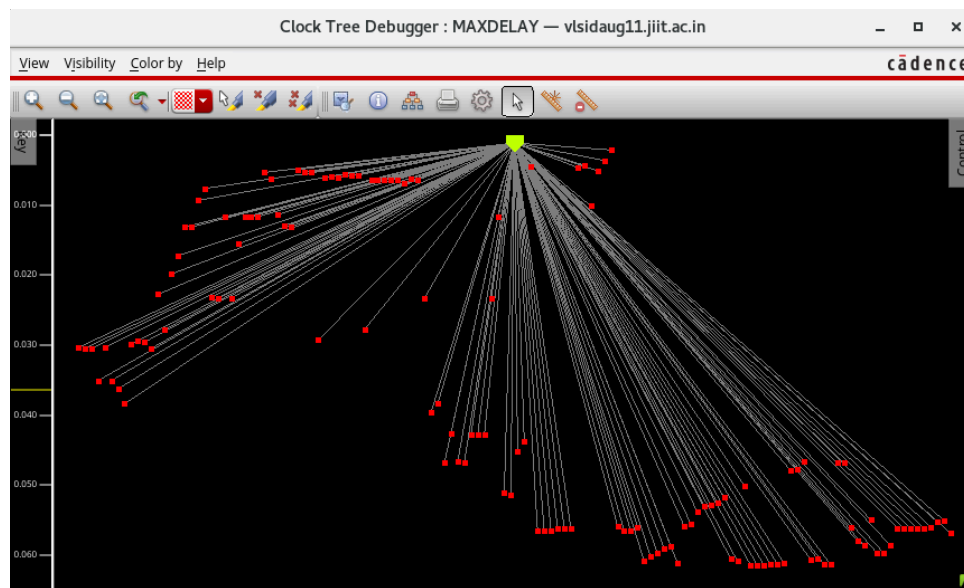
Power: 0.186

Improvisation %:

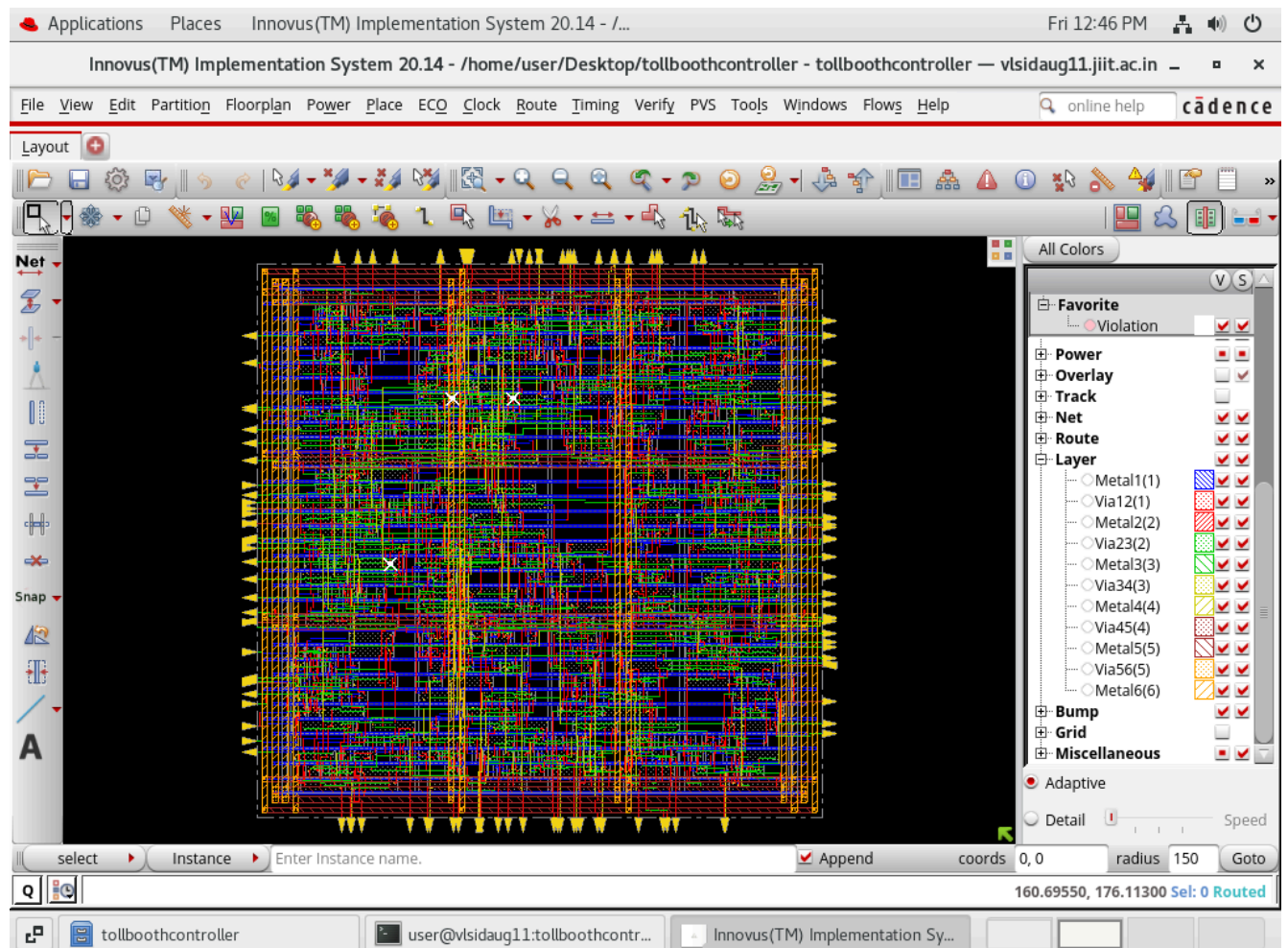
Area reduced by 27.71%

Power reduced by 22.75%

# CLOCK TREE



# NANOROUTED





## WORST REPORTS

### Power

ApplicationsPlacesTerminal

user@vlsidaug11:tollboothcontroller

FileEditViewSearchTerminalHelp

Total Power

Total Internal Power:0.1545199683.3784%

Total Switching Power:0.0307305416.5821%

Total Leakage Power:0.000073210.0395%

Total Power:0.18532371

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.1356	0.01135	3.848e-05	0.147	79.3
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.01895	0.01938	3.472e-05	0.03836	20.7
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	0.1545	0.03073	7.321e-05	0.1853	100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
VDD	0.9	0.1545	0.03073	7.321e-05	0.1853	100

\* Power Distribution Summary:

\* Highest Average Power:FE\_0FC1\_n\_593 (BUF2):0.001419

\* Highest Leakage Power:tollrates2\_reg[6] (SDFFRHX1):3.722e-07

\* Total Cap:3.85075e-12 F

\* Total instances in design:593

\* Total instances in design with no power:0

\* Total instances in design with no activity:0

\* Total Fillers and Decap:0

tollboothcontroller

user@vlsidaug11:tollboothcontr...

Innovus(TM) Imple

## BEST REPORTS

### Power

ApplicationsPlacesTerminal

user@vlsidaug11:tollboothcontroller

FileEditViewSearchTerminalHelp

Total Power

Total Internal Power:0.1545199683.3784%

Total Switching Power:0.0307305416.5821%

Total Leakage Power:0.000073210.0395%

Total Power:0.18532371

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	0.1356	0.01135	3.848e-05	0.147	79.3
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.01895	0.01938	3.472e-05	0.03836	20.7
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	0.1545	0.03073	7.321e-05	0.1853	100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
VDD	0.9	0.1545	0.03073	7.321e-05	0.1853	100

\* Power Distribution Summary:

\* Highest Average Power:FE\_0FC1\_n\_593 (BUF2):0.001419

\* Highest Leakage Power:tollrates2\_reg[6] (SDFFRHX1):3.722e-07

\* Total Cap:3.85075e-12 F

\* Total instances in design:593

\* Total instances in design with no power:0

\* Total instances in design with no activity:0

\* Total Fillers and Decap:0

tollboothcontroller

user@vlsidaug11:tollboothcontr...

Innovus(TM) Imple

### Area and time

ApplicationsPlacesTerminal

user@vlsidaug11:tollboothc

FileEditViewSearchTerminalHelp

timeDesign Summary

Setup views included:  
WORST

Setup mode	all	reg2reg	default
WNS (ns):	5.370	5.370	6.513
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	456	170	411

DRVs	Real	Total
Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0 (0)
max_tran	0 (0)	0 (0)
max_fanout	0 (0)	0 (0)
max_length	0 (0)	0 (0)

Density: 61.012%  
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports  
Total CPU time: 0.09 sec  
Total Real time: 1.0 sec  
Total Memory Usage: 1689.832031 Mbytes  
\*\*\* timeDesign #3 [finish] : cpu/real = 0:00:00.1/0:00:01.1 (0.1), totSession cpu/innovus 5>  
innovus 5> report\_area  
Hinst NameModule NameInst CountTotal Area  
tollboothcontroller59317250.710  
innovus 6>

tollboothcontroller

user@vlsidaug11:tollboothcontr...

lr

### Area and time

ApplicationsPlacesTerminal

user@vlsidaug11:tollboothcont

FileEditViewSearchTerminalHelp

# Parasitics Mode: No SPEF/RCDB  
# Signoff Settings: SI Off  
#####  
Calculate delays in BcWc mode...  
Start delay calculation (fullDC) (1 T). (MEM=1680.34)  
\*\*\* Calculating scaling factor for MINTIME libraries using the default operating cond:  
Total number of fetched objects 740  
AAE INFO: Total number of nets for which stage creation was skipped for all views 0  
End delay calculation. (MEM=1707.54 CPU=0:00:00.0 REAL=0:00:00.0)  
End delay calculation (fullDC). (MEM=1707.54 CPU=0:00:00.0 REAL=0:00:00.0)  
\*\*\* Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0 totSessionCpu=0:02:02 mer

timeDesign Summary

Hold views included:  
BEST

Hold mode	all	reg2reg	default
WNS (ns):	-0.087	-0.087	-0.012
TNS (ns):	-9.709	-9.401	-0.307
Violating Paths:	173	143	30
All Paths:	456	170	411

Density: 61.012%  
Routing Overflow: 0.00% H and 0.00% V

Reported timing to dir timingReports  
Total CPU time: 0.15 sec  
Total Real time: 0.0 sec  
Total Memory Usage: 1645.019531 Mbytes  
\*\*\* timeDesign #4 [finish] : cpu/real = 0:00:00.1/0:00:00.1 (1.0), totSession cpu/rea  
innovus 7>  
innovus 7> report\_area  
Hinst NameModule NameInst CountTotal Area  
tollboothcontroller59317250.710  
innovus 8>

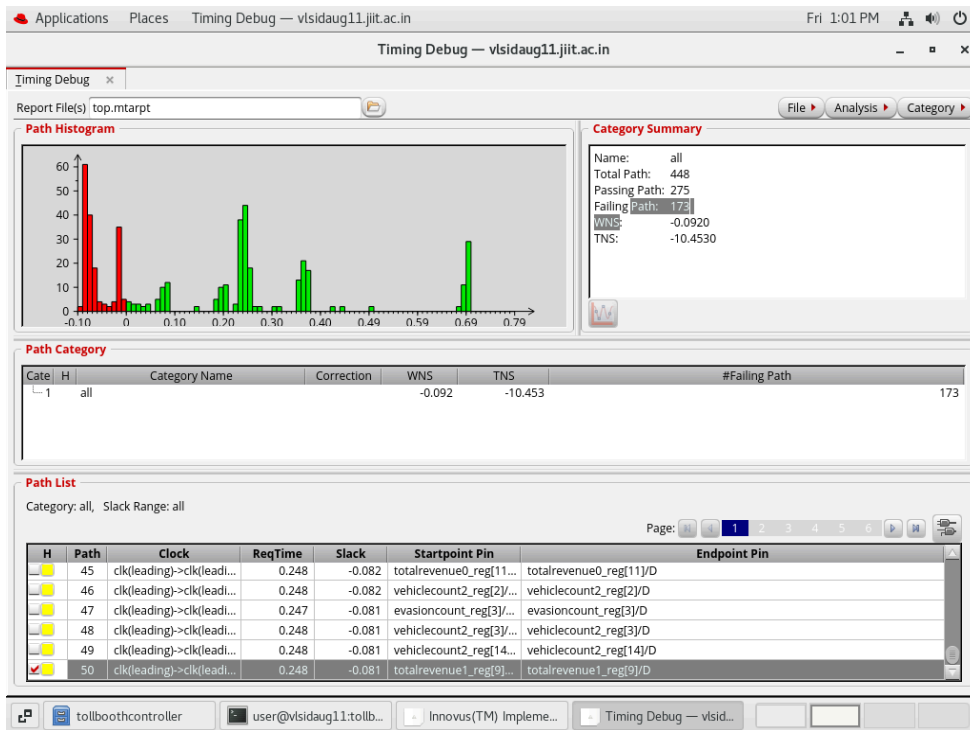
tollboothcontroller

user@vlsidaug11:tollboothcontr...

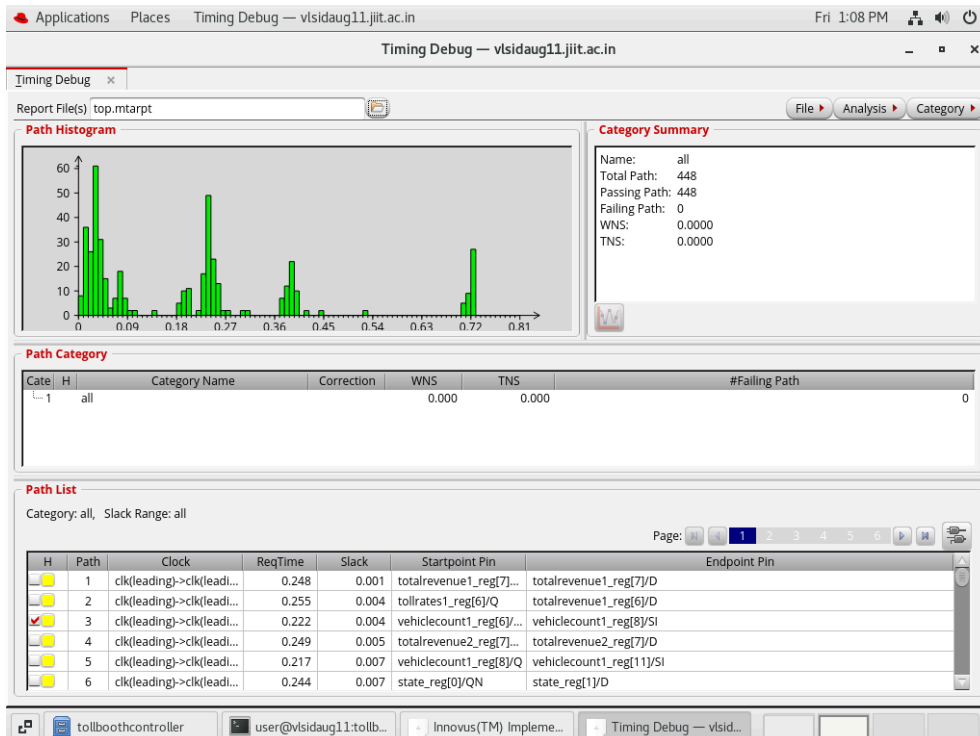
Innov

## STATIC TIME ANALYSIS

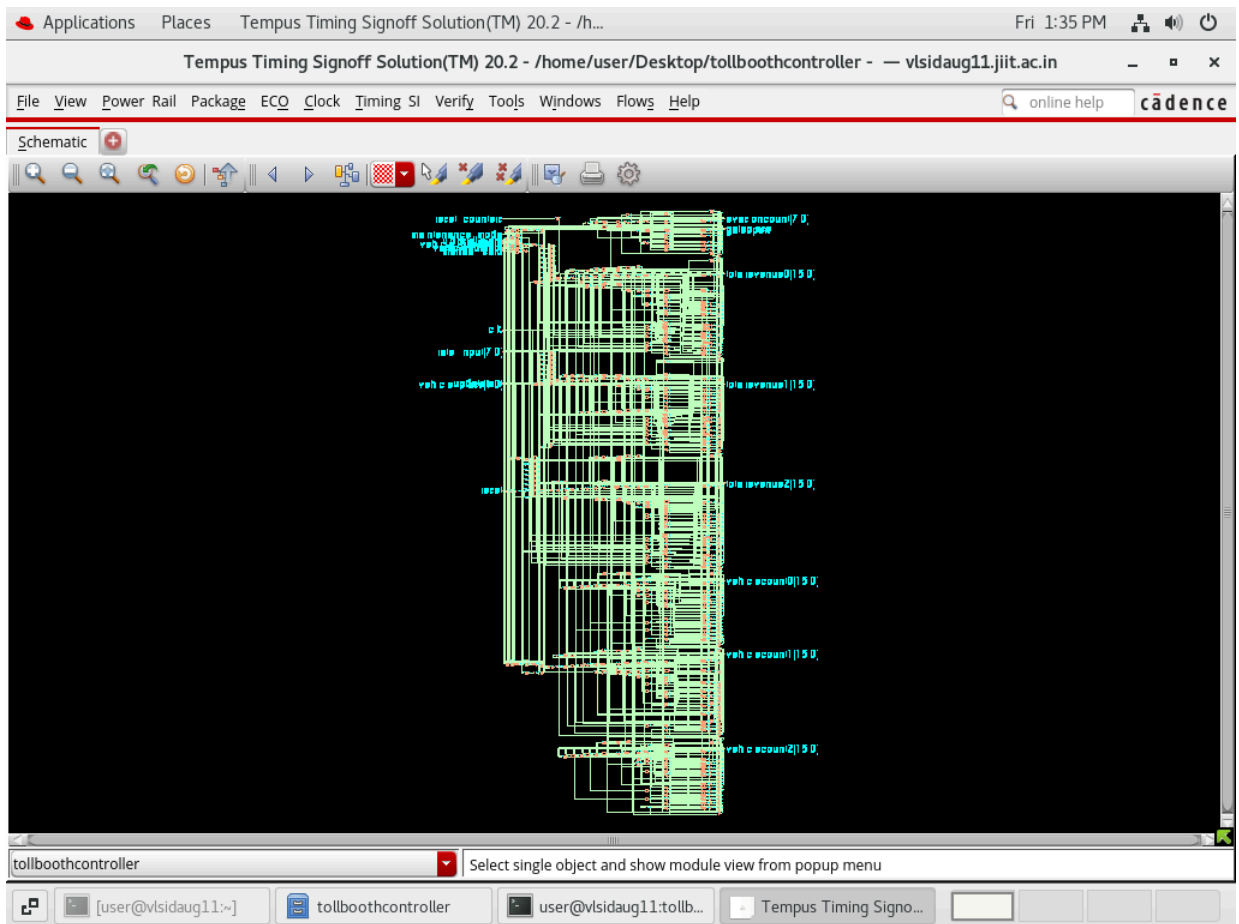
### Violations:



### Violations fixed:



## TEMPUS LAYOUT



## FINAL LAYOUT

