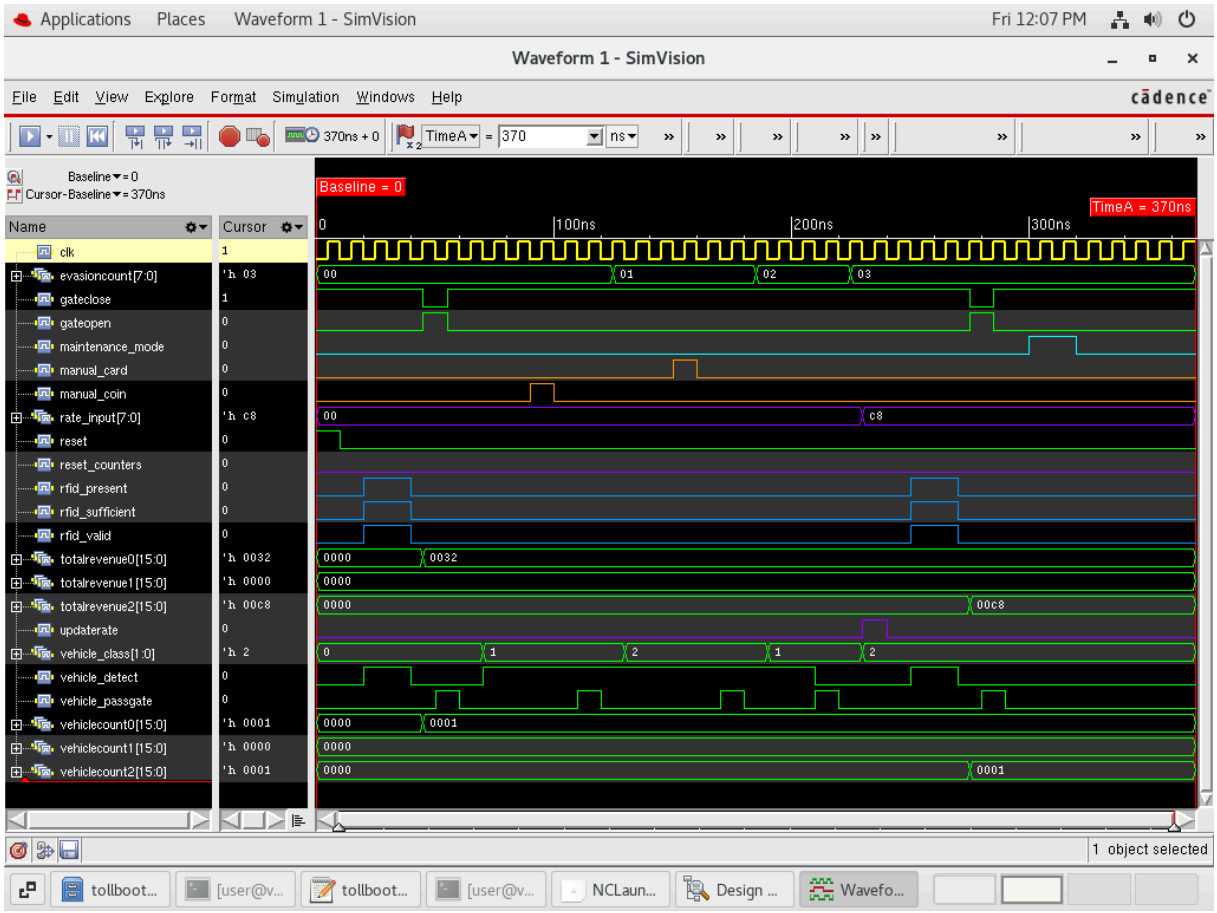
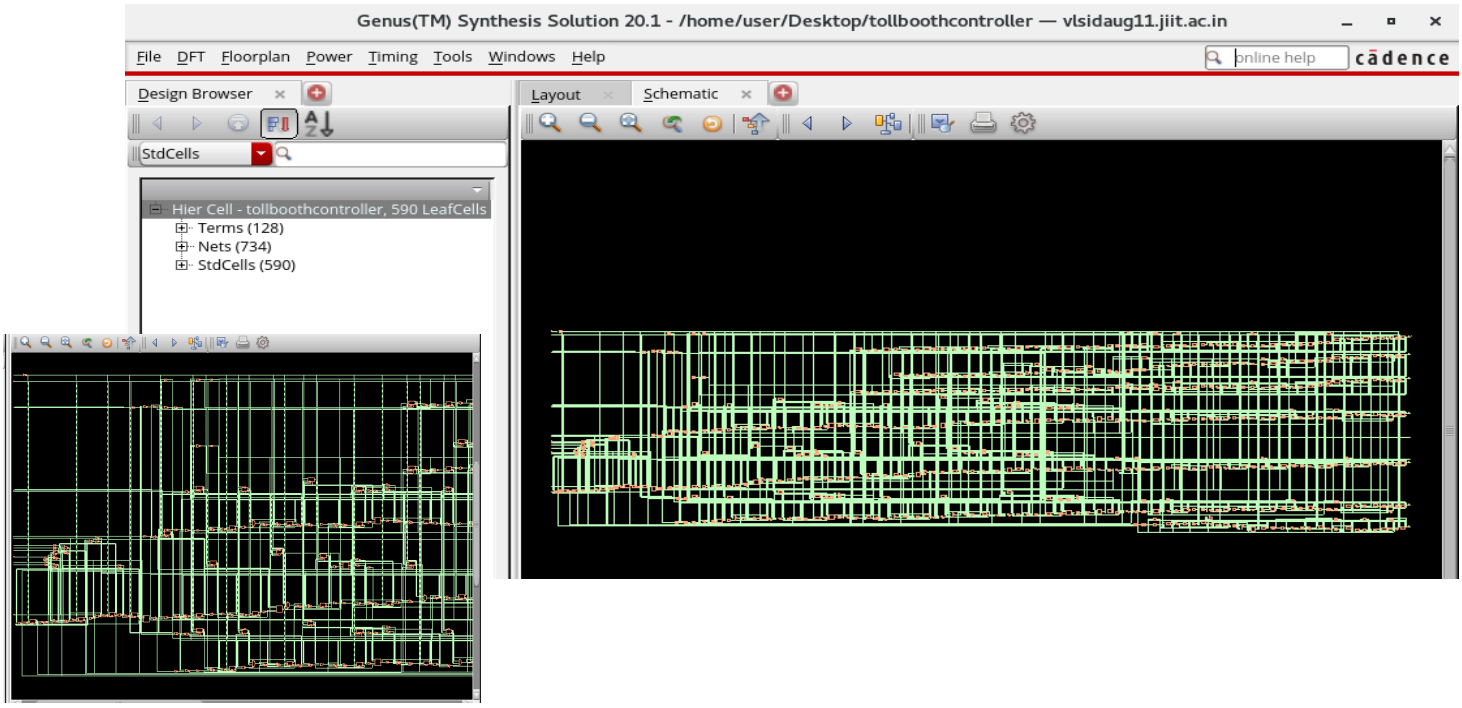
ISHI PROJECT- TOLL BOOTH CONTROLLER

WAVEFORM

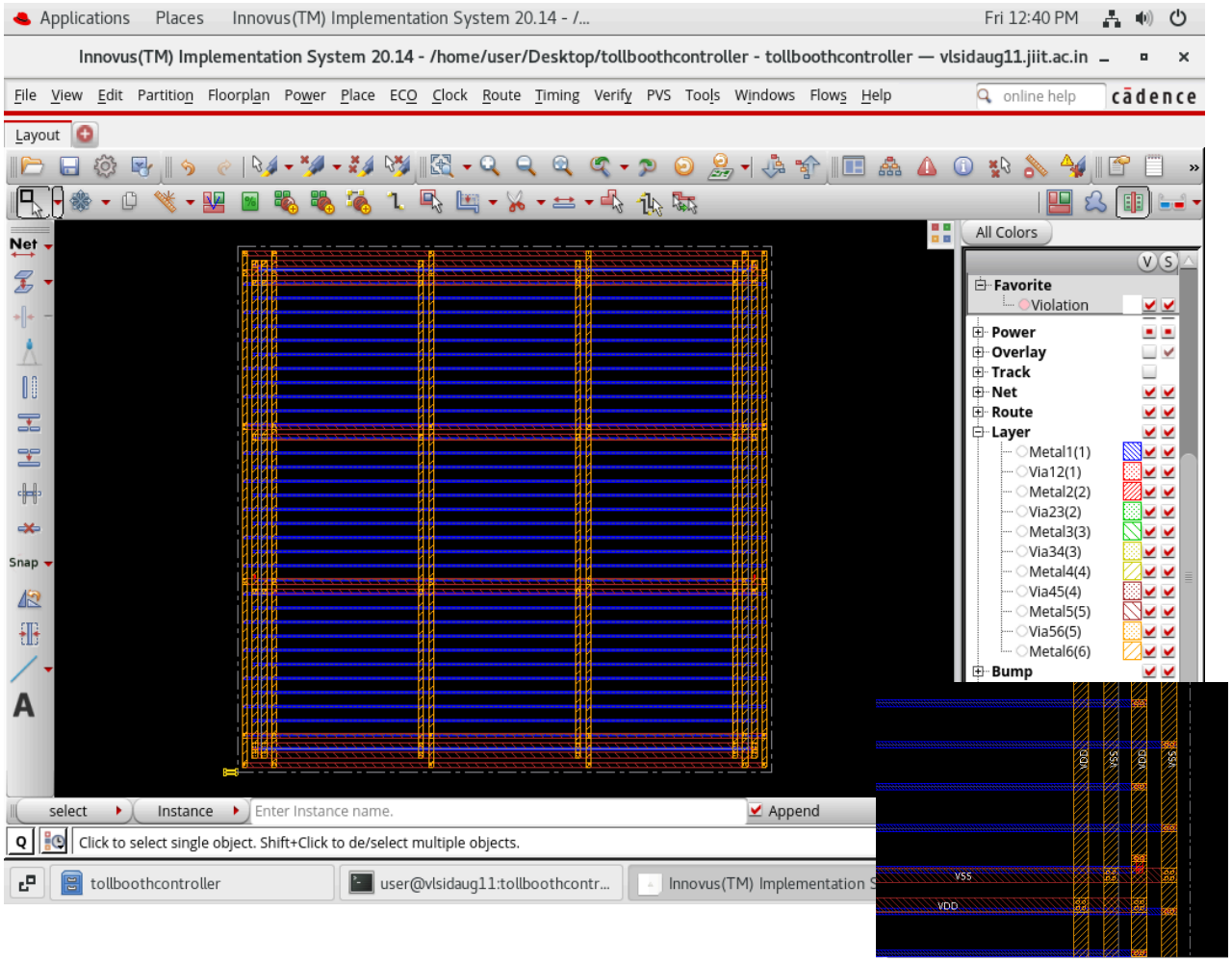


Schematic- genus

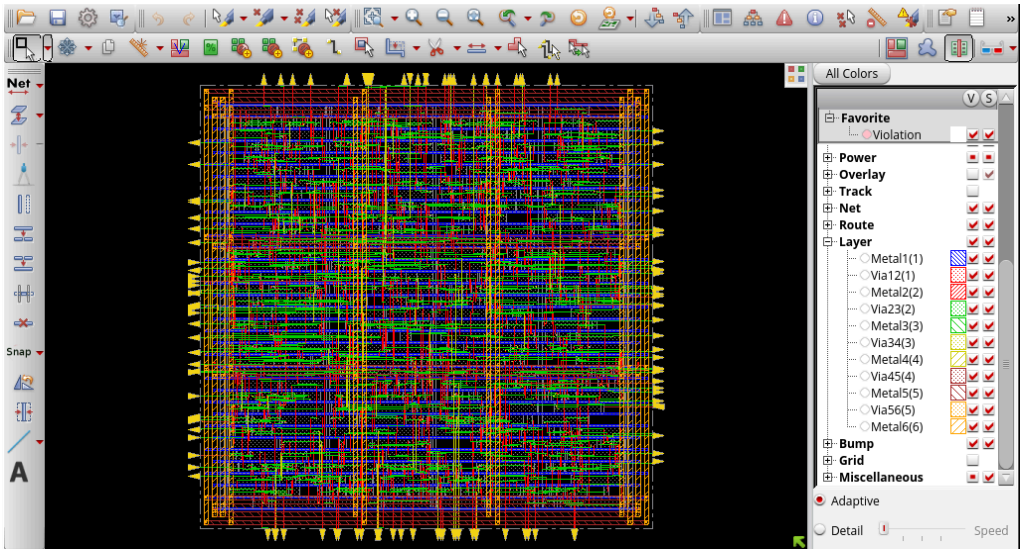


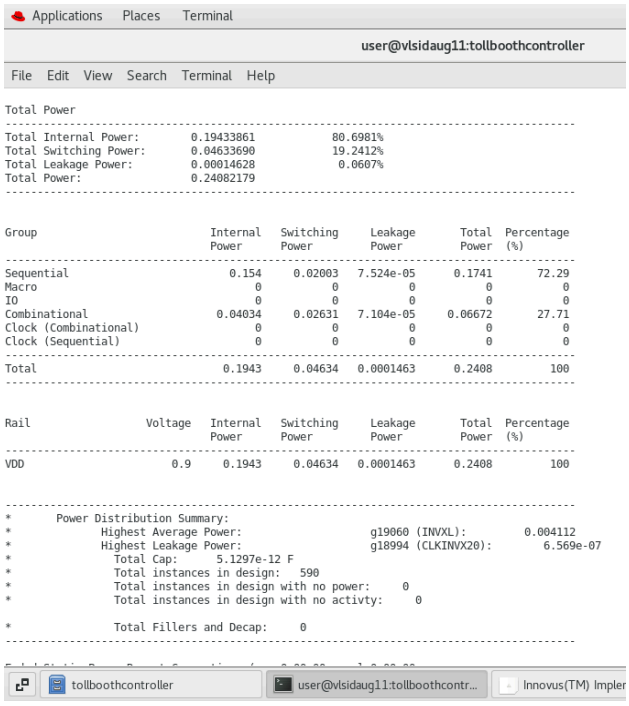
FLOORPLAN

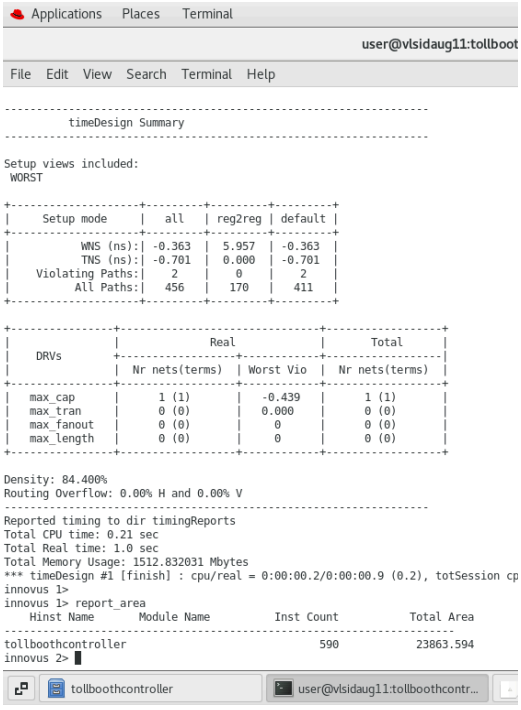
SPECIAL ROUTE



Placed (Pre Optimising)

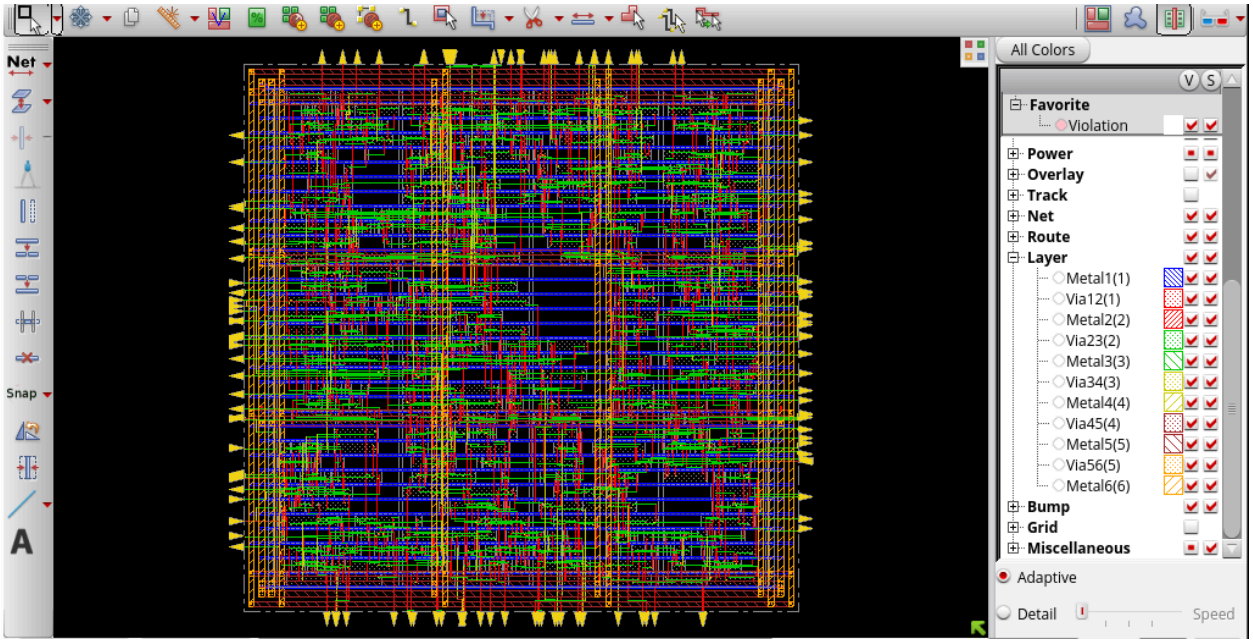


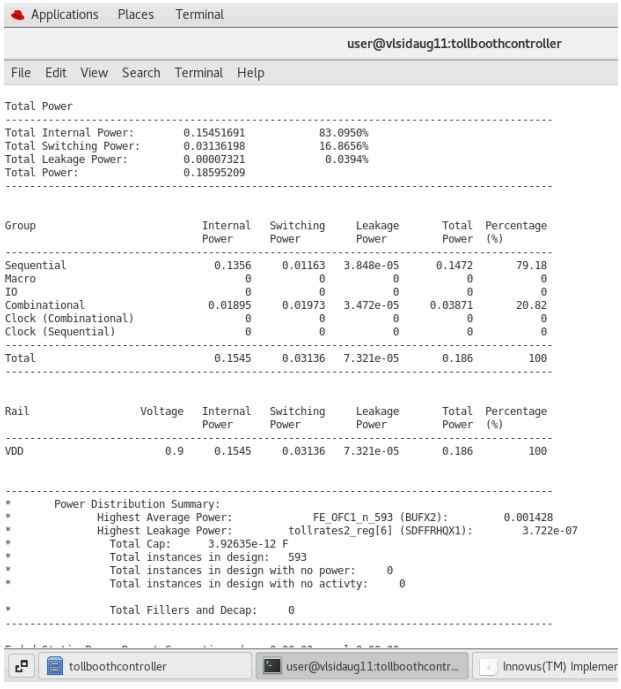


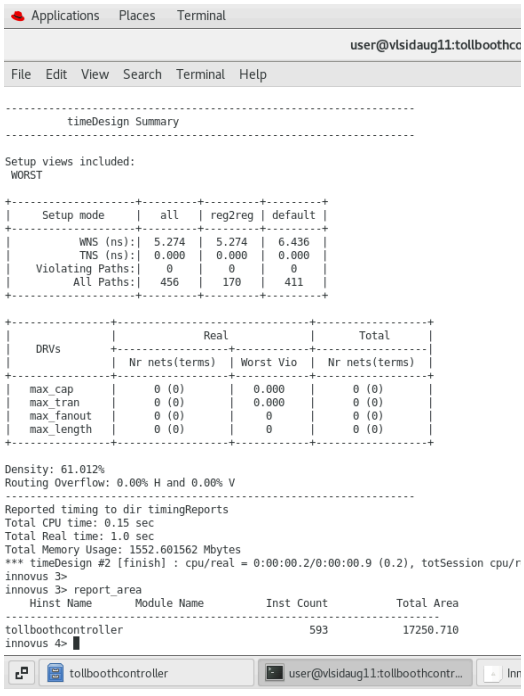


Area: 23863.594
Power: 0.2408

Placed and optimised



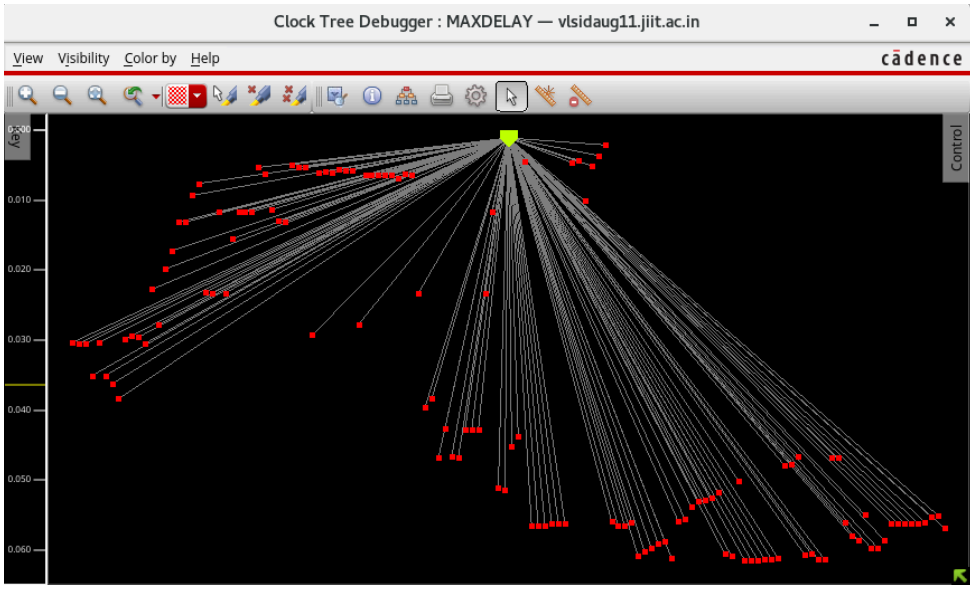




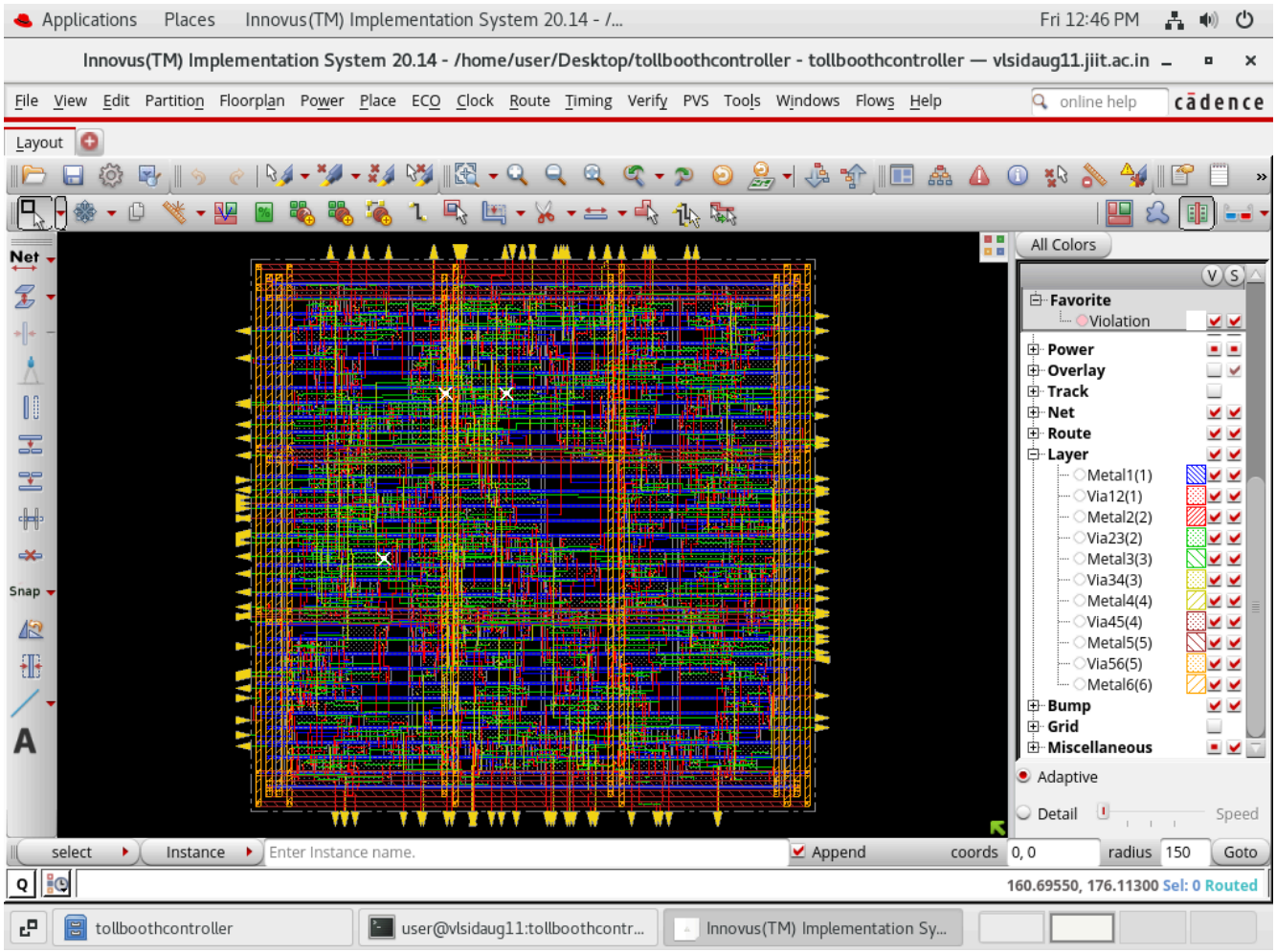
Area: 17250.710
Power: 0.186

Improvisation %:
Area reduced by 27.71%
Power reduced by 22.75%

CLOCK TREE

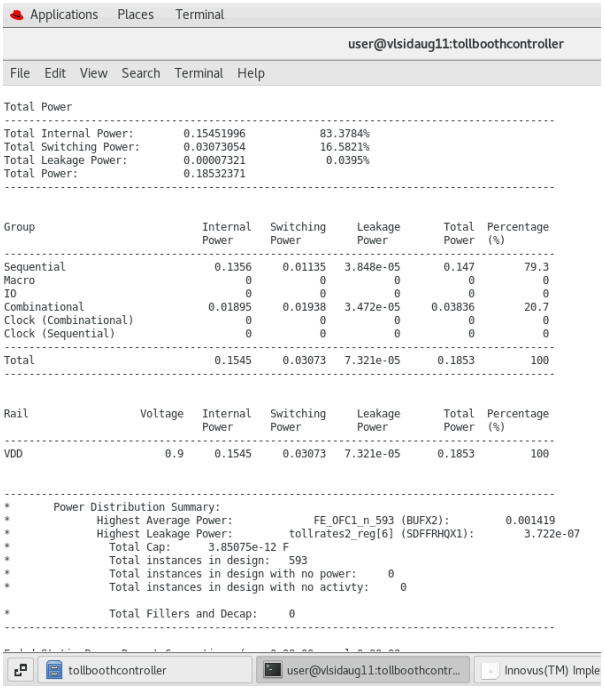


NANOROUTED



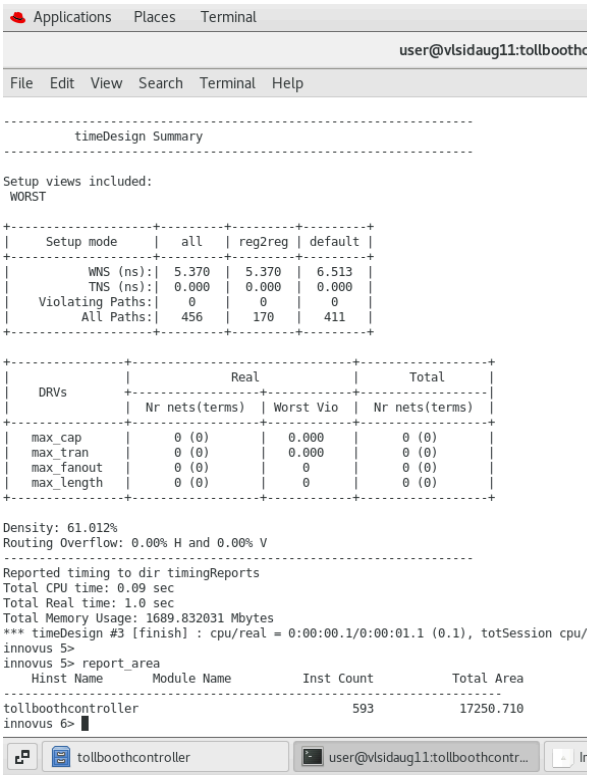
WORST REPORTS

Power



```
Applications  Places  Terminal
                                                  user@vlsidaug11:tollboothcontroller
File  Edit  View  Search  Terminal  Help

Total Power
-----------------------------------------------------------------------------------
Total Internal Power:        0.15451996            83.3784%
Total Switching Power:       0.03073054            16.5821%
Total Leakage Power:         0.00007321             0.0395%
Total Power:                 0.18532371
-----------------------------------------------------------------------------------


Group                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------
Sequential                        0.1356     0.01135   3.848e-05       0.147        79.3
Macro                                  0          0           0           0           0
IO                                     0          0           0           0           0
Combinational                   0.01895     0.01938   3.472e-05     0.03836        20.7
Clock (Combinational)                  0          0           0           0           0
Clock (Sequential)                     0          0           0           0           0
-----------------------------------------------------------------------------------
Total                             0.1545     0.03073   7.321e-05      0.1853         100
-----------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------
VDD                       0.9     0.1545     0.03073   7.321e-05      0.1853         100


-----------------------------------------------------------------------------------
*       Power Distribution Summary:
*              Highest Average Power:           FE_OFC1_n_593 (BUFX2):        0.001419
*              Highest Leakage Power:       tollrates2_reg[6] (SDFFRHQX1):        3.722e-07
*                Total Cap:      3.85075e-12 F
*                Total instances in design:   593
*                Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*               Total Fillers and Decap:     0
-----------------------------------------------------------------------------------
tollboothcontroller   user@vlsidaug11:tollboothcontr...   Innovus(TM) Imple
```

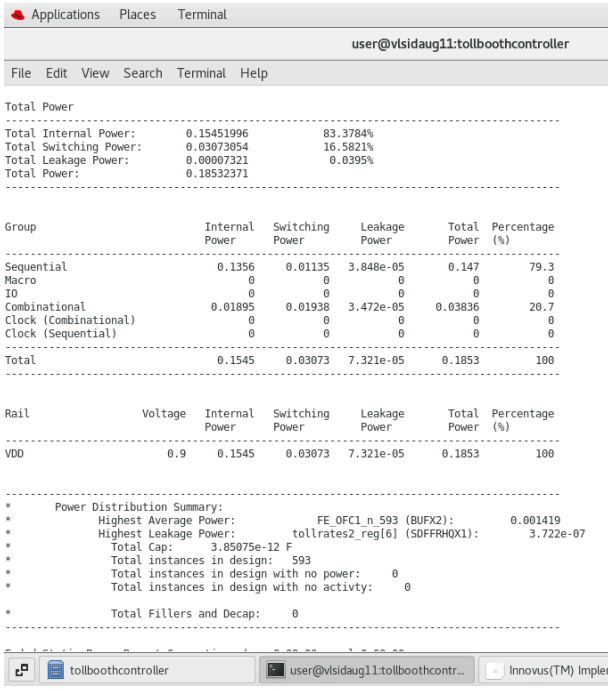
Area and time



```
Applications  Places  Terminal
                                                  user@vlsidaug11:tollbootho
File  Edit  View  Search  Terminal  Help

-------------------------------------------------------------
         timeDesign Summary
-------------------------------------------------------------

Setup views included:
 WORST

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  5.370  |  5.370  |  6.513  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   456   |   170   |   411   |
+--------------------+---------+---------+---------+

+----------------+-----------------------------+------------------+
|                |             Real            |       Total      |
|    DRVs        +------------------+----------+------------------|
|                |  Nr nets(terms)  | Worst Vio |  Nr nets(terms)  |
+----------------+------------------+-----------+------------------+
|   max_cap      |      0 (0)       |   0.000   |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000   |      0 (0)       |
|   max_fanout   |      0 (0)       |     0     |      0 (0)       |
|   max_length   |      0 (0)       |     0     |      0 (0)       |
+----------------+------------------+-----------+------------------+

Density: 61.012%
Routing Overflow: 0.00% H and 0.00% V
-------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.09 sec
Total Real time: 1.0 sec
Total Memory Usage: 1689.832031 Mbytes
*** timeDesign #3 [finish] : cpu/real = 0:00:00.1/0:00:01.1 (0.1), totSession cpu/
innovus 5>
innovus 5> report_area
    Hinst Name       Module Name          Inst Count           Total Area
-------------------------------------------------------------------------
tollboothcontroller                            593            17250.710
innovus 6>
tollboothcontroller   user@vlsidaug11:tollboothcontr...   Ir
```

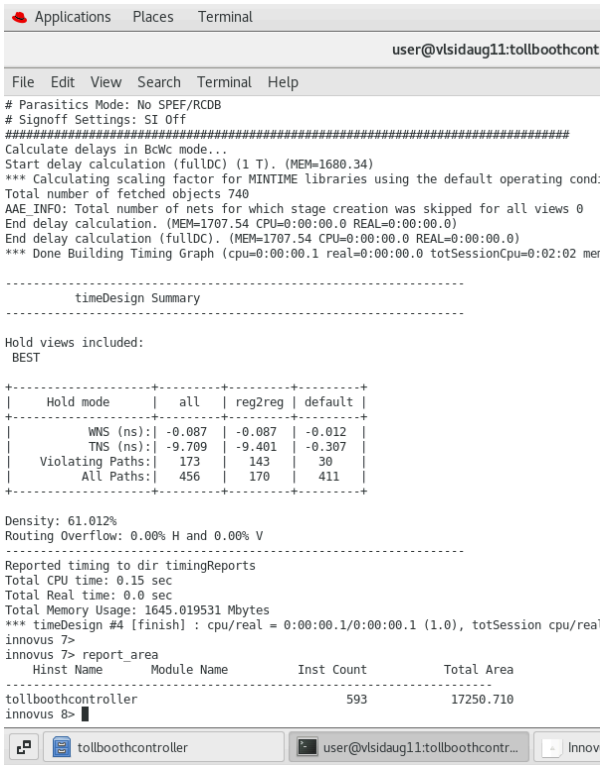
BEST REPORTS

Power



```
Applications  Places  Terminal
                                                  user@vlsidaug11:tollboothcontroller
File  Edit  View  Search  Terminal  Help

Total Power
-----------------------------------------------------------------------------------
Total Internal Power:        0.15451996            83.3784%
Total Switching Power:       0.03073054            16.5821%
Total Leakage Power:         0.00007321             0.0395%
Total Power:                 0.18532371
-----------------------------------------------------------------------------------


Group                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------
Sequential                        0.1356     0.01135   3.848e-05       0.147        79.3
Macro                                  0          0           0           0           0
IO                                     0          0           0           0           0
Combinational                   0.01895     0.01938   3.472e-05     0.03836        20.7
Clock (Combinational)                  0          0           0           0           0
Clock (Sequential)                     0          0           0           0           0
-----------------------------------------------------------------------------------
Total                             0.1545     0.03073   7.321e-05      0.1853         100
-----------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------
VDD                       0.9     0.1545     0.03073   7.321e-05      0.1853         100


-----------------------------------------------------------------------------------
*       Power Distribution Summary:
*              Highest Average Power:           FE_OFC1_n_593 (BUFX2):        0.001419
*              Highest Leakage Power:       tollrates2_reg[6] (SDFFRHQX1):        3.722e-07
*                Total Cap:      3.85075e-12 F
*                Total instances in design:   593
*                Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*               Total Fillers and Decap:     0
-----------------------------------------------------------------------------------
tollboothcontroller   user@vlsidaug11:tollboothcontr...   Innovus(TM) Imple
```

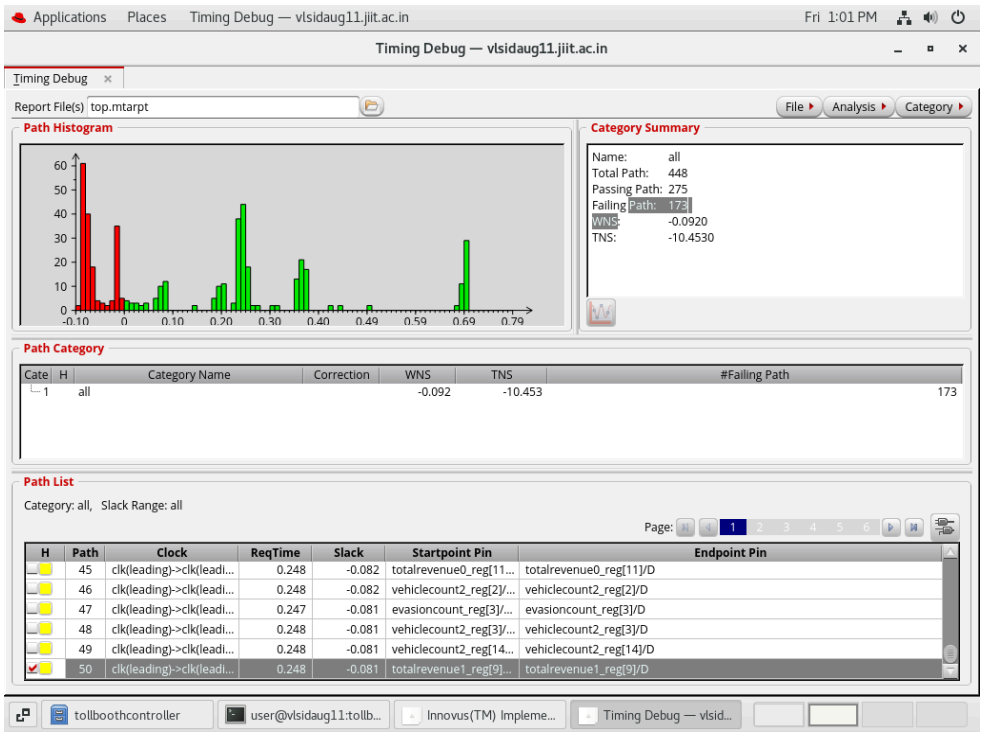
Area and time



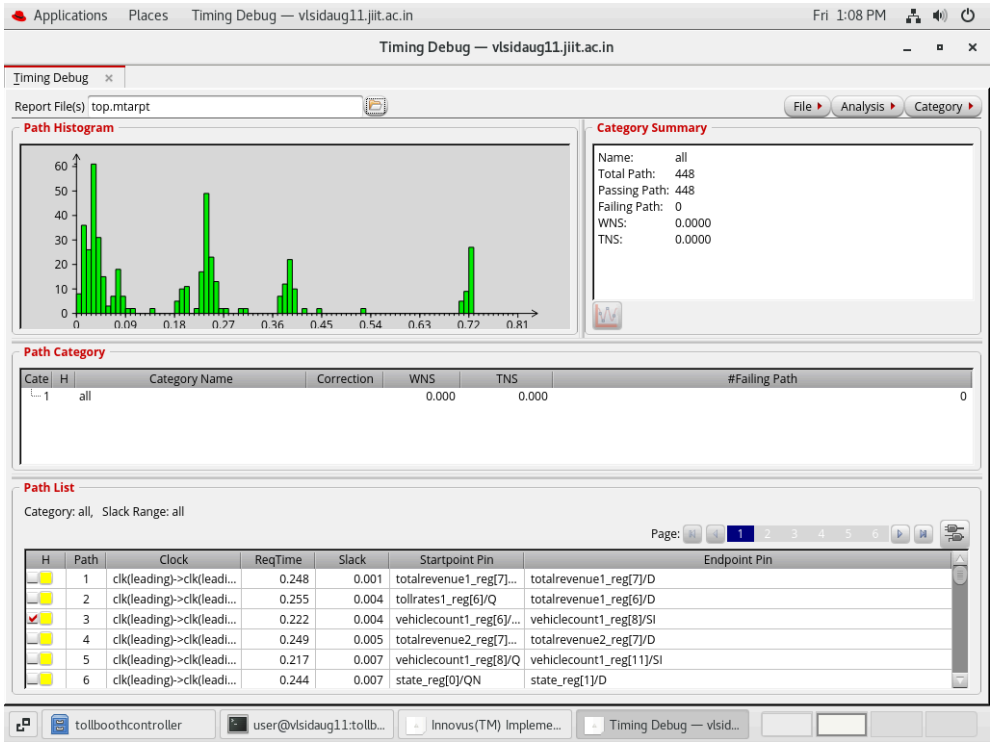
```
Applications  Places  Terminal
                                                  user@vlsidaug11:tollboothcont
File  Edit  View  Search  Terminal  Help
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
################################################################################
Calculate delays in BcWc mode...
Start delay calculation (fullDC) (1 T). (MEM=1680.34)
*** Calculating scaling factor for MINTIME libraries using the default operating cond
Total number of fetched objects 740
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
End delay calculation. (MEM=1707.54 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1707.54 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0 totSessionCpu=0:02:02 mer

-------------------------------------------------------------
         timeDesign Summary
-------------------------------------------------------------

Hold views included:
 BEST

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -0.087  | -0.087  | -0.012  |
|           TNS (ns):| -9.709  | -9.401  | -0.307  |
|    Violating Paths:|   173   |   143   |   30    |
|          All Paths:|   456   |   170   |   411   |
+--------------------+---------+---------+---------+

Density: 61.012%
Routing Overflow: 0.00% H and 0.00% V
-------------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.15 sec
Total Real time: 0.0 sec
Total Memory Usage: 1645.019531 Mbytes
*** timeDesign #4 [finish] : cpu/real = 0:00:00.1/0:00:00.1 (1.0), totSession cpu/real
innovus 7>
innovus 7> report_area
    Hinst Name       Module Name          Inst Count           Total Area
-------------------------------------------------------------------------
tollboothcontroller                            593            17250.710
innovus 8>
tollboothcontroller   user@vlsidaug11:tollboothcontr...   Innov
```

STATIC TIME ANALYSIS

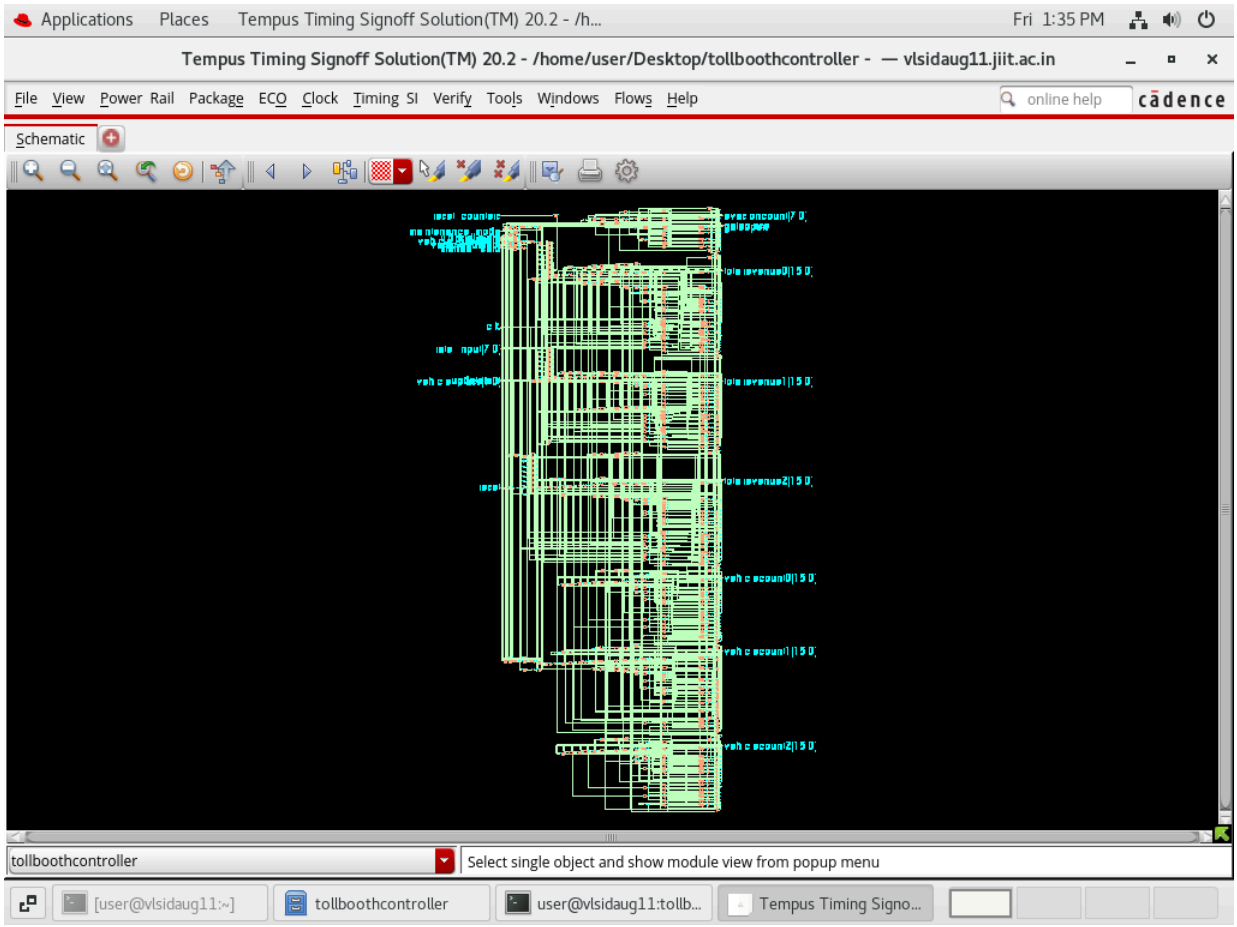
Violations:



Violations fixed:



TEMPUS LAYOUT



FINAL LAYOUT