ISHITA MUKHOPADHYAY

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EDUCATION

CORNELL UNIVERSITY — **Ithaca, New York, USA**
Ph.D., *Electrical Engineering, GPA:* ***4.08/4.00*** — 2009 - 2014

CORNELL UNIVERSITY — **Ithaca, New York, USA**
M.S., *Electrical Engineering, GPA:* ***4.08/4.00*** — 2009 - 2013

INDIAN INSTITUTE OF TECHNOLOGY — **New Delhi, India**
Master of Information and Communication Technology, *Electrical Engineering, CGPA:* ***9.38/10*** — 2008 - 2009

INDIAN INSTITUTE OF TECHNOLOGY — **New Delhi, India**
Bachelor of Technology, *Electrical Engineering, CGPA:* ***8.89/10*** — 2004 - 2008

WORK EXPERIENCE

Intel Corporation — **Folsom, California, USA**
Analog Product Development Engineer — December 2014 – August 2017

- Developed analog tests to catch manufacturing defects in high speed serial I/O in chipset products to ensure the quality of products for customers by utilizing analog circuit design knowledge.
- Acquired knowledge to characterize various functionalities of several high speed interfaces and carried out their testing in industrial testers.
- Developed techniques to enable wider characterization in high volume manufacturing (HVM) environment to decrease the turnaround time from first silicon to final product along with high quality product delivery to customers.

Intel Corporation — **Santa Clara, California, USA**
Graduate Technical Intern — June 2011 – December 2011
Guides: Dr. Prashant Goteti (HIP DFX), Dr. Suriyaprakash Natarajan (TMG/DTS Strategic CAD Labs)

- **Project: High speed serial I/O HVM test quality evaluation in presence of unexpected parametric shifts/variations**
  - Significantly reduced the number of parameters that need to be considered in the regime of unexpected process variation by employing sensitivity-like approach leading to significant reduction in required time and space.
  - Using the reduced parametric space, evaluated some of the existing high volume manufacturing (HVM) tests used in high speed serial I/O in SoC products in terms of their ability to detect circuit failure and came out with the respective system-level coverage.

INRIA - National Institute for Research in Computer Science and Control — **Rennes, France**
Undergraduate Research Intern — May 2007 – July 2007
Guide: Dr. Albert Benveniste (Head of DistribCom, INRIA, Rennes)

- **Project: Comparison of Optimization Algorithms for QoS Negotiation**
  - Distributed algorithms are preferred to optimize the cost to satisfy a request in a network but performance of existing distributed algorithms were of no match to the centralized algorithms.
  - Proposed an improved distributed Forward-Backward algorithm whose order came out to be same as that of the centralized algorithms and it had more than 50% improvement over the existing distributed algorithms as number of existing chains increased.

ACADEMIC RESEARCH EXPERIENCE

CORNELL UNIVERSITY — **Ithaca, New York, USA**
Electrical Engineering — 2009 - 2014

- **PhD Thesis: Variation tolerant calibration circuits for high performance I/O**
  Advisor: Prof. Alyssa Apsel
  - Investigated techniques to improve the accuracy of thermometer coded DAC, whose resolution, which is severely affected under process, voltage and temperature (PVT) variations, is critical for the calibration purposes of many circuit blocks in high speed I/O.
  - Proposed a dual-calibration technique which achieves an improvement of 36% in differential non-linearity (DNL) and 50% in integral non-linearity (INL) across several chip measurements.
  - Developed mathematical models of the proposed technique enabling the determination of overall yield.
  - Modeled high speed I/O links and observed the effect of non-linearity of DACs on different circuit blocks like phase interpolator and how overall performance is affected in terms of bit error rate (BER).

INDIAN INSTITUTE OF TECHNOLOGY — **New Delhi, India**
Electrical Engineering — 2008 - 2009

- **MTech Thesis: Error correction for VLSI logic synthesis**
  Advisor: Prof. Jayadeva
  - Investigated communications techniques for compensating the detrimental effects of reduced noise margin and the inherent unreliability of nanoscale transistors.
  - Proposed a new error correction scheme using learning techniques like Support Vector Machines (SVM) for VLSI logic synthesis when working with lower supply voltage and increased frequency of operation.

HONORS & AWARDS

- *Intel PhD Fellowship*, a prestigious award which recognizes winning students as being amongst the best in their specific areas of research, for the fourth year of PhD program at Cornell University, which was given to *only eighteen (18)* graduate students all over United States, 2012.
- *Jacob Fellowship* for the first year of PhD program at Cornell University, which was given to *only nine (9)* graduate students, 2009.
- Scholarship from Ministry of Human Resource Development (MHRD), India for final year of Dual Degree program which is given to *top 10%* students of IIT Delhi, 2008-09.
- *Dr. J.K. Pal Memorial Award*, which is given to *only one (1)* student member from each student branch of IEEE Delhi Section, 2009.
- *Outstanding Educational Impact and Undergraduate Teamwork Award* (the highest award) in the final competition of the IEEE 2007 International Future Energy Challenge out of 16 teams worldwide. Project was a joint venture of students of the ECE Dept of University of Colorado at Boulder, USA and EE Dept of IIT Delhi, India.
- IIT Delhi Semester Merit Award for *topping* the Dual Degree Program in Electrical Engineering, 2006.
- *Best Volunteer of IEEE Student Branch IIT Delhi*, out of more than 100 students, 2007-08.

PUBLICATIONS

Journal Publications:

- **Ishita Mukhopadhyay**, Mustansir Mukadam, Rajendran Narayanan, Frank O'Mahony, Alyssa Apsel, "Dual-calibration Technique for Improving Static Linearity of Thermometer DACs for I/O", *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 24, no. 3, pp. 1050-1058, March 2016.
- Xuan Zhang, Bojiong Ni, **Ishita Mukhopadhyay**, Alyssa Apsel, "Improving Absolute Accuracy of Integrated Resistors With Device Diversification", *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol.59, no.6, pp. 346-350, June 2012.
- Xuan Zhang, **Ishita Mukhopadhyay**, Rajeev Dokania, Alyssa Apsel, "A 46μW Self-Calibrated GHz VCO for Low Power Radios", *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 58, no.12, pp. 847-851, December 2011.
- Xuan Zhang, Mustansir Mukadam, **Ishita Mukhopadhyay**, and Alyssa Apsel, "Process Compensation Loops for High Speed Ring Oscillators in Sub-Micron CMOS", *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on*, vol.1, no. 1, pp. 59-70, March 2011.

Conference Publications:

- Debesh Bhatta, **Ishita Mukhopadhyay**, Suriyaprakash Natarajan, Prashant Goteti, Bin Xue, "Framework for analog test coverage", *Quality Electronic Design (ISQED), 2013 14th International Symposium on*, pp. 468-475, 4-6 March 2013.
- **Ishita Mukhopadhyay**, Hélia Pouyllau, "Distributed Optimization Algorithms for X-Domain End-to-End QoS Negotiation", *IEEE Advanced International Conference on Telecommunications (AICT)*, pp.7-12, June 2008.

TECHNICAL SKILLS & LANGUAGES

Analog Design	Cadence Virtuoso, Calibre, ADS, PSpice
Programming	MATLAB, Verilog-A, VHDL, C/C++, HTML, Bash Shell Scripting, Tcl/Tk, SML
CAD	Eclipse CDT, Circuit Maker, Altera MAX+II
Laboratory tools	Wire-bonding, Spectrum Analyzer, Real time and Equivalent time oscilloscopes, Wafer probing
Miscellaneous	LaTeX, Doxygen
Operating Systems	Windows, Linux/Unix
Languages	English (Fluent), Hindi (Fluent), Bengali (Fluent)

TEACHING EXPERIENCE

Digital VLSI Design — **Ithaca, New York, USA**
Teaching Assistant, Cornell University — January 2014 – May 2014

- Helped in designing and evaluating exams and quizzes for the course.
- Provided guidance to students to design/research final design projects in digital VLSI.

CATALYST — **Ithaca, New York, USA**
Cornell University — July 2010

- Summer program for high school students from under-represented groups intended to pique their interest in engineering.
- Helped students to design/research group projects in opto-electronics with various applications in energy and communications.

LEADERSHIP EXPERIENCE

- **Treasurer**, Cornell India Association, organized the annual flagship cultural event *Art of India* with participation from various student music & dance groups across Cornell University, 2012-13.
- **Treasurer**, ECEGO (ECE Graduate Organization) at Cornell University, 2010-11.
- **Treasurer**, IEEE Student Branch IIT Delhi, with more than 100 IEEE Student Members in IIT Delhi, 2007-09.
- **Event Coordinator**, Tryst, Annual Technical Festival of IIT Delhi with a budget of Rs. 1 million and students participation from colleges all over India, 2007.