GDSII OF 8 BIT SUBTRACTOR

IN SYNOPSYS

PROJECT REPORT

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INTRODUCTION

GDSII, or Graphic Data Stream II, is a vital file format widely used in the semiconductor industry to send information for making ICs.

Converting an RTL design into a GDSII layout involves key stages in VLSI design using Synopsys tools.

1. RTL defines circuit functionality in Verilog , initiating the design flow.
2. Floorplanning sets chip dimensions, core positioning, and power grid layout for optimal area use and signal flow.
Power planning ensures efficient power distribution and integrity.
3. Placement optimizes cell positioning for minimal wiring and maximum performance.
4. Clock tree synthesis balances clock distribution to minimize skew.
5. Routing establishes interconnections to form signal paths, power networks, and clock distribution.

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These stages collectively ensure the final layout meets speed, area, and power requirements, yielding a robust IC design.

1. RTL SYNTHESIS

RTL Synthesis is the process of converting high level HDL Code into a gate level mapped netlist.

The first step is to create a new file (named sub8bit) in the rtl directory of SRM_WOrkshop directory and write HDL Description of 8 Bit Subtractor.

Terminal - ws2_26@ws2:~/SRM_Workshop/rtl

File Edit View Terminal Tabs Help

```
module sub8bit(
    input wire [7:0] A,
    input wire [7:0] B,
    input wire Clock,
    output reg [7:0] diff,
    output reg borrow
);

reg [8:0] B_comp;
reg [8:0] Res;

always @(posedge Clock) begin
    B_comp = {1'b0, ~B} + 9'b000000001;
    Res = {1'b0, A} + B_comp;
    diff = Res[7:0];
    borrow = Res[8];
end

endmodule
~
~
```

Compiled the code(used vcs sub8bit -full64 and ./simv)

```
Parsing design file 'sub8bit_rtl.v'
Top Level Modules:
       sub8bit
No TimeScale specified
Starting vcs inline pass...

1 module and 0 UDP read.
        However, due to incremental compilation, no re-compilation is necessary.
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod a-x ../simv; fi
g++  -o ../simv      -rdynamic  -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-rpath=/usr/synopsys/vcs/V-2023.12/linux64/lib -L/usr/syno
psys/vcs/V-2023.12/linux64/lib  -Wl,-rpath-link=./  /usr/lib64/libnuma.so.1   objs/amcQw_d.o   _31115_archive_1.so _prev_archive_1.so   SIM_l.o      rma
pats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o           -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -lucli
native /usr/synopsys/vcs/V-2023.12/linux64/lib/vcs_tls.o   -Wl,-whole-archive  -lvcsucli    -Wl,-no-whole-archive          /usr/synopsys/vcs/V-2023.12/l
inux64/lib/vcs_save_restore_new.o -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .340 seconds to compile + .450 seconds to elab + .225 seconds to link
[ws2_26@ws2 rtl]$ ./simv
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detected on the machine. To enable $save functionality, ASLR will be switched
 off and simv re-executed.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_INFO' to suppress this message.
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version V-2023.12_Full64; Runtime version V-2023.12_Full64;  Jul 11 17:27 2024
          V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.450 seconds;       Data structure size:   0.0Mb
Thu Jul 11 17:27:59 2024
[ws2_26@ws2 rtl]$
```

Next step is to change the design name to “sub8bit” in the commom_setup.tcl file in the rm_setup directory in DC directory.

```
puts "RM-Info: Running script [info script]\n"

##############################################################################
##########
# Variables common to all reference methodology scripts
# Script: common_setup.tcl
# Version: N-2017.09-SP4 (April 23, 2018)
# Copyright (C) 2007-2017 Synopsys, Inc. All rights reserved.
##############################################################################
##########

set DESIGN_NAME                   "sub8bit"  ;#  The name of the top-level desig
n
set PDK_PATH                    "./../ref/" ; # to set the PDK path for the desi
gn
set DESIGN_REF_DATA_PATH          ""   ;#  Absolute path prefix variable for libr
ary/design data.
                                       #  Use this variable to prefix the common
 absolute path
                                       #  to the common variables defined below.
                                       #  Absolute paths are mandatory for hiera
rchical
                                       #  reference methodology flow.
"common_setup.tcl" [dos] 79L, 4838C                          1,1           Top
```

Then we have to create a .SDC file in the CONSTRAINTS directory.

```
File  Edit  View  Terminal  Tabs  Help
create_clock -period 1 [get_ports Clock]

set_input_delay -max 0.6 -clock Clock [all_inputs]
set_input_transition 0.15 [all_inputs]

set_output_delay -max 0.4 -clock Clock [all_outputs]

set_clock_uncertainty -setup -1.00 [get_clocks Clock]
set_clock_uncertainty -hold -1.00 [get_clocks Clock]
set_max_transition 0.250 [current_design]
set_max_transition -clock_path 0.1 [get_clocks Clock]
```

Constraints ensure that the physical and electrical characteristics of the chip meet required specifications, like power, area and performance.

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Now in the DC directory, invoke dc_shell and then start_gui.
Now run the run_dc.tcl file.

Result of elaborate command:

```
dc_shell> elaborate ${DESIGN_NAME}
Loading db file '/usr/synopsys/syn/V-2023.12/libraries/syn/gtech.db'
Loading db file '/usr/synopsys/syn/V-2023.12/libraries/syn/standard.sldb'
  Loading link library 'gtech'
Running PRESTO HDLC

Inferred memory devices in process
        in routine sub8bit line 12 in file
                './../rtl/sub8bit_rtl.v'.
===============================================================================
|    Register Name    |    Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|     borrow_reg      | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
|      diff_reg       | Flip-flop |   8   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully. (sub8bit)
Elaborated 1 design.
Current design is now 'sub8bit'.
1
Current design is 'sub8bit'.
```

Result of compile_ultra:

```
dc_shell> compile_ultra
Information: Performing leakage power optimization. (PWR-850)
CPU Load: 136%, Ram Free: 0 GB, Swap Free: 7 GB, Work Disk Free: 9 GB, Tmp Disk Free: 6 GB
Alib files are up-to-date.
Information: Evaluating DesignWare library utilization. (UISN-27)

============================================================================
| DesignWare Building Block Library  |         Version         | Available |
============================================================================
| Basic DW Building Blocks           | V-2023.12-DWBB_202312.0 |     *     |
| Licensed DW Building Blocks        | V-2023.12-DWBB_202312.0 |     *     |
============================================================================
```

```
==============================================================================================
| Flow Information                                                                           |
----------------------------------------------------------------------------------------------
| Flow         | Design Compiler WLM                                                         |
| Command Line | compile_ultra                                                               |
==============================================================================================
| Design Information                                        | Value                            |
==============================================================================================
| Number of Scenarios                                       | 0                                |
| Leaf Cell Count                                           | 12                               |
| Number of User Hierarchies                                | 0                                |
| Sequential Cell Count                                     | 9                                |
| Macro Count                                               | 0                                |
| Number of Power Domains                                   | 0                                |
| Number of Path Groups                                     | 2                                |
| Number of VT Class                                        | 1                                |
| Number of Clocks                                          | 1                                |
| Number of Dont Touch Cells                                | 0                                |
| Number of Dont Touch Nets                                 | 0                                |
| Number of Size Only Cells                                 | 0                                |
| Design with UPF Data                                      | false                            |
==============================================================================================
Information: Sequential output inversion is enabled.  SVF file must be used for formal verification. (OPT-1208)
  Simplifying Design 'sub8bit'

Loaded alib file './alib-52/saed32rvt_tt0p78vn40c.db.alib'
  Building model 'DW01_NAND2'
Information: Ungrouping 0 of 1 hierarchies before Pass 1 (OPT-775)
CPU Load: 145%, Ram Free: 0 GB, Swap Free: 7 GB, Work Disk Free: 9 GB, Tmp Disk Free: 6 GB
Information: State dependent leakage is now switched from on to off.
```

```
Threshold voltage group cell usage:
>> saed32cell_svt 100.00%

  Beginning Mapping Optimizations  (Ultra High effort)
  -------------------------------

                                TOTAL
   ELAPSED            WORST NEG  SETUP    DESIGN                              LEAKAGE
    TIME      AREA      SLACK    COST    RULE COST         ENDPOINT           POWER
  --------- --------- --------- --------- --------- ------------------------- ---------
    0:00:04     248.3      0.00       0.0       0.0                           526381.1250
    0:00:04     248.3      0.00       0.0       0.0                           526381.1250

Threshold voltage group cell usage:
>> saed32cell_svt 100.00%

  Beginning Constant Register Removal
  -----------------------------------
    0:00:04     248.3      0.00       0.0       0.0                           526381.1250
    0:00:04     248.3      0.00       0.0       0.0                           526381.1250

Threshold voltage group cell usage:
>> saed32cell_svt 100.00%
```

```
  0:00:05     237.9      0.00       0.0       0.0                              466134.8125
  0:00:05     237.9      0.00       0.0       0.0                              466134.8125
  0:00:05     237.9      0.00       0.0       0.0                              466134.8125
  0:00:05     237.9      0.00       0.0       0.0                              466134.8125

                                 TOTAL
  ELAPSED            WORST NEG   SETUP    DESIGN                                LEAKAGE
   TIME      AREA      SLACK     COST    RULE COST         ENDPOINT             POWER
 --------- --------- --------- --------- --------- ------------------------- ---------
  0:00:05     237.9      0.00       0.0       0.0                              466134.8125
  0:00:05     239.4      0.05       0.1       0.0                              465187.6250
  0:00:05     248.0      0.03       0.0       0.0                              560683.2500
  0:00:05     248.0      0.03       0.0       0.0                              560683.2500
  0:00:05     248.0      0.03       0.0       0.0                              560683.2500
  0:00:05     242.7      0.00       0.0       0.0                              528760.8750
  0:00:05     242.7      0.00       0.0       0.0                              528760.8750
  0:00:05     242.7      0.00       0.0       0.0                              528760.8750
  0:00:05     242.7      0.00       0.0       0.0                              528760.8750
  0:00:05     242.7      0.00       0.0       0.0                              528760.8750
  0:00:05     242.7      0.00       0.0       0.0                              528760.8750
  0:00:05     237.6      0.00       0.0       0.0                              458665.5625
PU Load: 153%, Ram Free: 0 GB, Swap Free: 7 GB, Work Disk Free: 9 GB, Tmp Disk Free: 6 GB
oading db file '/ve/ws_home/ws2_26/SRM_Workshop/ref/lib/stdcell_rvt/saed32rvt_tt0p78vn40c.db'


ote: Symbol # after min delay cost means estimated hold TNS across all active scenarios


 Optimization Complete
 ---------------------
nformation: State dependent leakage is now switched from off to on.
nformation: Propagating switching activity (low effort zero delay simulation). (PWR-6)
```

```
 Optimization Complete
 ---------------------
Information: State dependent leakage is now switched from off to on.
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
CPU Load: 153%, Ram Free: 0 GB, Swap Free: 7 GB, Work Disk Free: 9 GB, Tmp Disk Free: 6 GB
Information: Total number of MV cells in the design.
-----------------------------------------------------------------------------------------
 MV Cells                                          Total Number
-----------------------------------------------------------------------------------------
 Level Shifter:                                    0
 Enable Level Shifter:                             0
 Isolation Cell:                                   0
 Retention Cell:                                   0
 Retention Clamp Cell:                             0
 Switch Cell:                                      0
 Always-On Cell:                                   0
 Repeater Cell:                                    0

-----------------------------------------------------------------------------------------
Unmapped MV Cells
-----------------------------------------------------------------------------------------
0 Isolation Cells are unmapped
0 Retention Clamp Cells are unmapped
-----------------------------------------------------------------------------------------
1
Current design is 'sub8bit'.
dc_shell> dc_shell> report_qor
Information: Updating design information... (UID-85)

****************************************
```

Result of report_qor command:

QOR stands for Quality Of Results. It gives overview of all the parameters.

```
****************************************
Report : qor
Design : sub8bit
Version: V-2023.12
Date   : Mon Jul  8 16:13:14 2024
****************************************


  Timing Path Group 'Clock'
  -----------------------------------
  Levels of Logic:              15.00
  Critical Path Length:          1.31
  Critical Path Slack:           0.01
  Critical Path Clk Period:      1.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:          0
  Hierarchical Port Count:          0
  Leaf Cell Count:                108
  Buf/Inv Cell Count:              31
  Buf Cell Count:                   0
  Inv Cell Count:                  31
  CT Buf/Inv Cell Count:            0
```

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```
  Buf/Inv Cell Count:              31
  Buf Cell Count:                   0
  Inv Cell Count:                  31
  CT Buf/Inv Cell Count:            0
  Combinational Cell Count:        99
  Sequential Cell Count:            9
  Macro Count:                      0
  -----------------------------------


  Area
  -----------------------------------
  Combinational Area:      177.646663
  Noncombinational Area:    59.977986
  Buf/Inv Area:             39.392320
  Total Buffer Area:             0.00
  Total Inverter Area:          39.39
  Macro/Black Box Area:      0.000000
  Net Area:                 31.083046
  -----------------------------------
  Cell Area:               237.624649
  Design Area:             268.707695


  Design Rules
  -----------------------------------
  Total Number of Nets:           125
  Nets With Violations:             0
  Max Trans Violations:             0
  Max Cap Violations:               0
  -----------------------------------


  Hostname: ws2.trg.vlsiexpert.in
```

Result od report_timing command:
It gives detailed timing report for synthesized designs.

```
  Hostname: ws2.trg.vlsiexpert.in

  Compile CPU Statistics
  ----------------------------------------
  Resource Sharing:                    0.08
  Logic Optimization:                  0.53
  Mapping Optimization:                0.28
  ----------------------------------------
  Overall Compile Time:                6.83
  Overall Compile Wall Clock Time:     8.27

  --------------------------------------------------------------------

  Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


  Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

  --------------------------------------------------------------------


1
dc_shell> report_timing

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : sub8bit
Version: V-2023.12
Date   : Mon Jul  8 16:14:49 2024
****************************************
```

```
Operating Conditions: tt0p78vn40c   Library: saed32rvt_tt0p78vn40c
Wire Load Model Mode: enclosed

  Startpoint: B[1] (input port clocked by Clock)
  Endpoint: diff_reg[7]
            (rising edge-triggered flip-flop clocked by Clock)
  Path Group: Clock
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  sub8bit            8000                  saed32rvt_tt0p78vn40c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock Clock (rise edge)                  0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     0.60       0.60 f
  B[1] (in)                                0.00       0.60 f
  U53/Y (INVX1_RVT)                        0.11       0.71 r
  U55/Y (OR2X1_RVT)                        0.10       0.82 r
  U32/Y (INVX0_RVT)                        0.04       0.86 f
  U56/Y (OR2X1_RVT)                        0.09       0.94 f
  U58/Y (AND2X1_RVT)                       0.09       1.03 f
  U63/Y (OR2X1_RVT)                        0.11       1.14 f
  U72/Y (AND2X1_RVT)                       0.09       1.23 f
  U77/Y (OR2X1_RVT)                        0.10       1.33 f
```

Slack = 0.01

```
  input external delay                        0.60       0.60 f
  B[1] (in)                                   0.00       0.60 f
  U53/Y (INVX1_RVT)                           0.11       0.71 r
  U55/Y (OR2X1_RVT)                           0.10       0.82 r
  U32/Y (INVX0_RVT)                           0.04       0.86 f
  U56/Y (OR2X1_RVT)                           0.09       0.94 f
  U58/Y (AND2X1_RVT)                          0.09       1.03 f
  U63/Y (OR2X1_RVT)                           0.11       1.14 f
  U72/Y (AND2X1_RVT)                          0.09       1.23 f
  U77/Y (OR2X1_RVT)                           0.10       1.33 f
  U82/Y (AND2X1_RVT)                          0.08       1.41 f
  U83/Y (AND2X1_RVT)                          0.09       1.50 f
  U88/Y (OR2X1_RVT)                           0.10       1.60 f
  U93/Y (AND2X1_RVT)                          0.08       1.68 f
  U94/Y (AND2X1_RVT)                          0.09       1.77 f
  U20/Y (INVX0_RVT)                           0.05       1.82 r
  U109/Y (AND2X1_RVT)                         0.08       1.90 r
  diff_reg[7]/D (DFFX1_RVT)                   0.01       1.91 r
  data arrival time                                      1.91

  clock Clock (rise edge)                     1.00       1.00
  clock network delay (ideal)                 0.00       1.00
  clock uncertainty                           1.00       2.00
  diff_reg[7]/CLK (DFFX1_RVT)                 0.00       2.00 r
  library setup time                         -0.08       1.92
  data required time                                     1.92
  -------------------------------------------------------------
  data required time                                     1.92
  data arrival time                                     -1.91
  -------------------------------------------------------------
  slack (MET)                                            0.01


1
```

History of dc_shell:

```
Writing verilog file '/ve/ws_home/ws2_26/SRM_Workshop/DC/results/sub8bit.mapped.v'.
1
dc_shell> history
     1  start_gui
     2  source -echo -verbose ./rm_setup/dc_setup.tcl
     3  set RTL_SOURCE_FILES ./../rtl/sub8bit_rtl.v
     4  define_design_lib WORK -path ./WORK
     5  set_dont_use [get_lib_cells */FADD*]
     6  set_dont_use [get_lib_cells */HADD*]
     7  set_dont_use [get_lib_cells */AO*]
     8  set_dont_use [get_lib_cells */OA*]
     9  set_dont_use [get_lib_cells */NAND*]
    10  set_dont_use [get_lib_cells */XOR*]
    11  set_dont_use [get_lib_cells */NOR*]
    12  set_dont_use [get_lib_cells */XNOR*]
    13  set_dont_use [get_lib_cells */MUX*]
    14  analyze -format verilog ${RTL_SOURCE_FILES}
    15  elaborate ${DESIGN_NAME}
    16  current_design
    17  read_sdc ./../CONSTRAINTS/sub8bit.sdc
    18  compile_ultra
    19  report_qor
    20  report_timing
    21  write -format verilog -hierarchy -output ${RESULTS_DIR}/${DCRM_FINAL_VERILOG_OUTPUT_FILE}
    22  history
dc_shell>
```

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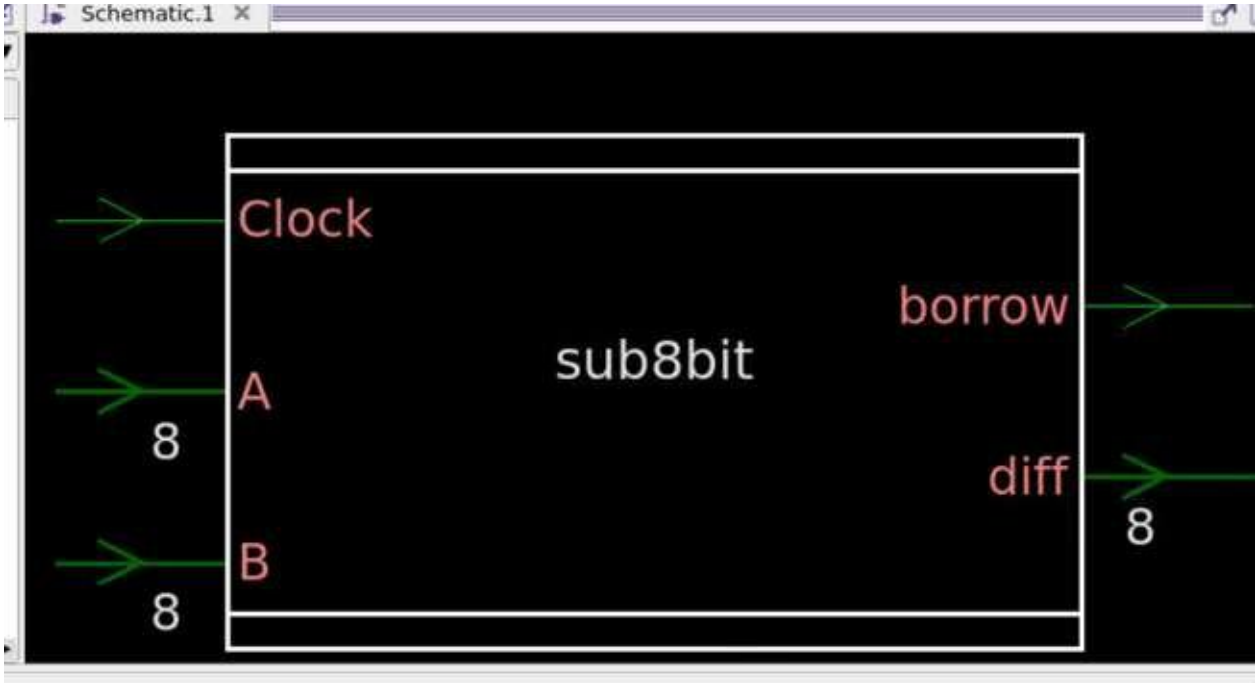
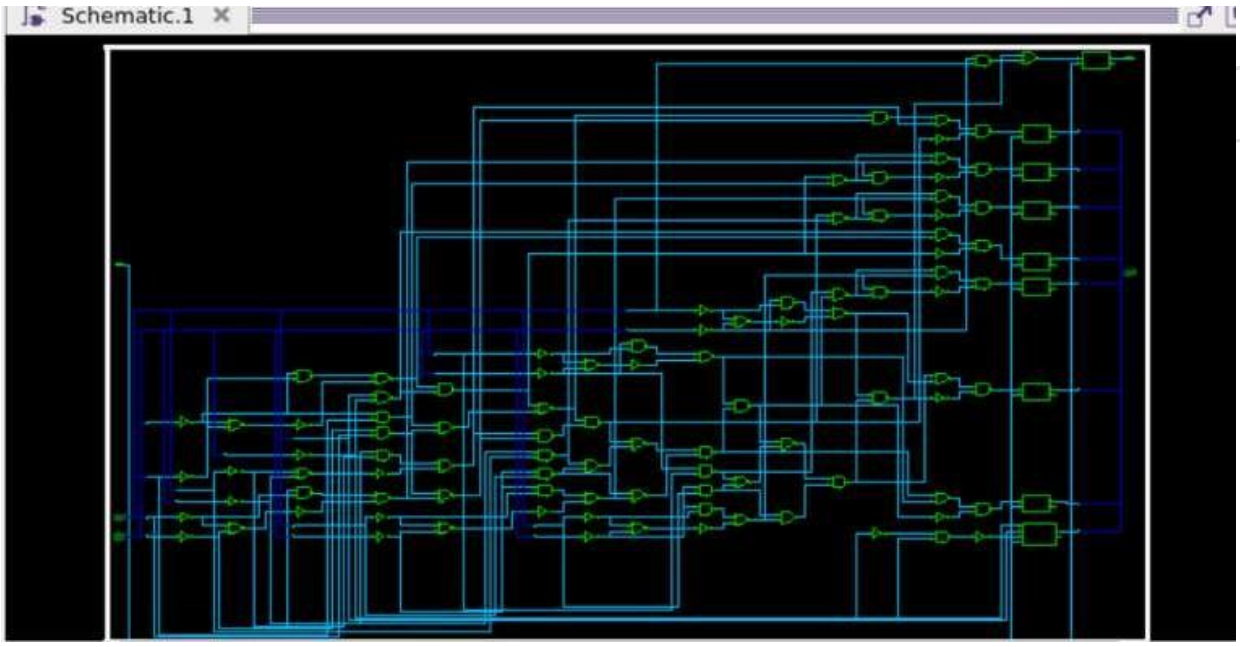
Block Diagram of 8 Bit Subtractor:



Gate Level Diagram:



. Sub8bit.mapped.v file:

Gate level mapped netlist file

```
File  Edit  View  Terminal  Tabs  Help
/////////////////////////////////////////////////////////////
// Created by: Synopsys DC Ultra(TM) in wire load mode
// Version   : V-2023.12
// Date      : Mon Jul  8 16:18:03 2024
/////////////////////////////////////////////////////////////


module sub8bit ( A, B, Clock, diff, borrow );
  input [7:0] A;
  input [7:0] B;
  output [7:0] diff;
  input Clock;
  output borrow;
  wire   N7, N18, N19, N20, N21, N22, N23, N24, N25, n1, n2, n3, n4, n5, n6,
         n7, n8, n9, n10, n11, n12, n13, n14, n15, n16, n17, n18, n19, n20,
         n21, n22, n23, n24, n25, n26, n27, n28, n29, n30, n31, n32, n33, n34,
         n35, n36, n37, n38, n39, n40, n41, n42, n43, n44, n45, n46, n47, n48,
         n49, n50, n51, n52, n53, n54, n55, n56, n57, n58, n59, n60, n61, n62,
         n63, n64, n65, n66, n67, n68, n69, n70, n71, n72, n73, n74, n75, n76,
         n77, n78, n79, n80, n81, n82, n83, n84, n85, n86, n87, n88, n89, n90;

  DFFX1_RVT borrow_reg ( .D(N25), .CLK(Clock), .Q(borrow) );
  DFFX1_RVT \diff_reg[7]  ( .D(N24), .CLK(Clock), .Q(diff[7]) );
  DFFX1_RVT \diff_reg[6]  ( .D(N23), .CLK(Clock), .Q(diff[6]) );
  DFFX1_RVT \diff_reg[5]  ( .D(N22), .CLK(Clock), .Q(diff[5]) );
  DFFX1_RVT \diff_reg[4]  ( .D(N21), .CLK(Clock), .Q(diff[4]) );
  DFFX1_RVT \diff_reg[3]  ( .D(N20), .CLK(Clock), .Q(diff[3]) );
  DFFX1_RVT \diff_reg[2]  ( .D(N19), .CLK(Clock), .Q(diff[2]) );
  DFFX1_RVT \diff_reg[1]  ( .D(N18), .CLK(Clock), .Q(diff[1]) );
  DFFSSRX1_RVT \diff_reg[0]  ( .D(N7), .SETB(A[0]), .RSTB(n90), .CLK(Clock),
        .Q(diff[0]) );
  OR2X1_RVT U11 ( .A1(n87), .A2(n49), .Y(N25) );
  OR2X1_RVT U12 ( .A1(n86), .A2(n85), .Y(n89) );
```

```
Terminal - ws2_26@ws2:~/SRM_Workshop/DC/results
File  Edit  View  Terminal  Tabs  Help
  DFFX1_RVT \diff_reg[5]  ( .D(N22), .CLK(Clock), .Q(diff[5]) );
  DFFX1_RVT \diff_reg[4]  ( .D(N21), .CLK(Clock), .Q(diff[4]) );
  DFFX1_RVT \diff_reg[3]  ( .D(N20), .CLK(Clock), .Q(diff[3]) );
  DFFX1_RVT \diff_reg[2]  ( .D(N19), .CLK(Clock), .Q(diff[2]) );
  DFFX1_RVT \diff_reg[1]  ( .D(N18), .CLK(Clock), .Q(diff[1]) );
  DFFSSRX1_RVT \diff_reg[0]  ( .D(N7), .SETB(A[0]), .RSTB(n90), .CLK(Clock),
        .Q(diff[0]) );
  OR2X1_RVT U11 ( .A1(n87), .A2(n49), .Y(N25) );
  OR2X1_RVT U12 ( .A1(n86), .A2(n85), .Y(n89) );
  AND2X1_RVT U13 ( .A1(n62), .A2(n61), .Y(n64) );
  OR2X1_RVT U14 ( .A1(n51), .A2(n50), .Y(n53) );
  OR2X1_RVT U15 ( .A1(n75), .A2(n74), .Y(n77) );
  OR2X1_RVT U16 ( .A1(n68), .A2(n67), .Y(n69) );
  OR2X1_RVT U17 ( .A1(n55), .A2(n54), .Y(n56) );
  OR2X1_RVT U18 ( .A1(n79), .A2(n78), .Y(n80) );
  INVX1_RVT U19 ( .A(A[1]), .Y(n11) );
  INVX0_RVT U20 ( .A(n87), .Y(n88) );
  INVX0_RVT U21 ( .A(n82), .Y(n83) );
  INVX0_RVT U22 ( .A(n78), .Y(n76) );
  INVX0_RVT U23 ( .A(n71), .Y(n72) );
  INVX0_RVT U24 ( .A(n68), .Y(n65) );
  INVX0_RVT U25 ( .A(n58), .Y(n59) );
  INVX0_RVT U26 ( .A(n55), .Y(n52) );
  INVX0_RVT U27 ( .A(n2), .Y(n90) );
  INVX0_RVT U28 ( .A(n18), .Y(n19) );
  INVX0_RVT U29 ( .A(n23), .Y(n24) );
  INVX0_RVT U30 ( .A(n4), .Y(n5) );
  INVX0_RVT U31 ( .A(n32), .Y(n33) );
  INVX0_RVT U32 ( .A(n13), .Y(n14) );
  INVX0_RVT U33 ( .A(n8), .Y(n9) );
  INVX0_RVT U34 ( .A(n42), .Y(n43) );
  INVX1_RVT U35 ( .A(B[0]), .Y(N7) );
  INVX0_RVT U36 ( .A(A[3]), .Y(n17) );
```

Terminal - ws2_26@ws2:~/SRM_Workshop/DC/r

File Edit View Terminal Tabs Help

```
INVX0_RVT U36 ( .A(A[3]), .Y(n17) );
INVX0_RVT U37 ( .A(A[0]), .Y(n1) );
INVX0_RVT U38 ( .A(A[2]), .Y(n22) );
INVX0_RVT U39 ( .A(A[5]), .Y(n7) );
INVX0_RVT U40 ( .A(A[4]), .Y(n31) );
INVX0_RVT U41 ( .A(B[3]), .Y(n28) );
INVX0_RVT U42 ( .A(A[6]), .Y(n41) );
INVX0_RVT U43 ( .A(A[7]), .Y(n3) );
AND2X1_RVT U44 ( .A1(n1), .A2(N7), .Y(n2) );
INVX1_RVT U45 ( .A(B[7]), .Y(n48) );
AND2X1_RVT U46 ( .A1(n48), .A2(n3), .Y(n6) );
OR2X1_RVT U47 ( .A1(n3), .A2(n48), .Y(n4) );
OR2X1_RVT U48 ( .A1(n6), .A2(n5), .Y(n85) );
INVX1_RVT U49 ( .A(B[5]), .Y(n38) );
AND2X1_RVT U50 ( .A1(n38), .A2(n7), .Y(n10) );
OR2X1_RVT U51 ( .A1(n7), .A2(n38), .Y(n8) );
OR2X1_RVT U52 ( .A1(n10), .A2(n9), .Y(n74) );
INVX1_RVT U53 ( .A(B[1]), .Y(n12) );
AND2X1_RVT U54 ( .A1(n12), .A2(n11), .Y(n15) );
OR2X1_RVT U55 ( .A1(n12), .A2(n11), .Y(n13) );
OR2X1_RVT U56 ( .A1(n15), .A2(n14), .Y(n50) );
OR2X1_RVT U57 ( .A1(A[0]), .A2(N7), .Y(n51) );
AND2X1_RVT U58 ( .A1(n50), .A2(n51), .Y(n55) );
AND2X1_RVT U59 ( .A1(n12), .A2(A[1]), .Y(n54) );
INVX1_RVT U60 ( .A(B[2]), .Y(n21) );
AND2X1_RVT U61 ( .A1(n21), .A2(A[2]), .Y(n26) );
OR2X1_RVT U62 ( .A1(n54), .A2(n26), .Y(n16) );
OR2X1_RVT U63 ( .A1(n55), .A2(n16), .Y(n62) );
AND2X1_RVT U64 ( .A1(n28), .A2(n17), .Y(n20) );
OR2X1_RVT U65 ( .A1(n17), .A2(n28), .Y(n18) );
OR2X1_RVT U66 ( .A1(n20), .A2(n19), .Y(n63) );
AND2X1_RVT U67 ( .A1(n21), .A2(n22), .Y(n25) );
OR2X1_RVT U68 ( .A1(n22), .A2(n21), .Y(n23) );
```

Terminal - ws2_26@ws2:~/SRM_Workshop/DC/results

File Edit View Terminal Tabs Help

```
OR2X1_RVT U68 ( .A1(n22), .A2(n21), .Y(n23) );
OR2X1_RVT U69 ( .A1(n25), .A2(n24), .Y(n57) );
OR2X1_RVT U70 ( .A1(n26), .A2(n57), .Y(n61) );
AND2X1_RVT U71 ( .A1(n63), .A2(n61), .Y(n27) );
AND2X1_RVT U72 ( .A1(n62), .A2(n27), .Y(n68) );
AND2X1_RVT U73 ( .A1(n28), .A2(A[3]), .Y(n67) );
INVX1_RVT U74 ( .A(B[4]), .Y(n30) );
AND2X1_RVT U75 ( .A1(n30), .A2(A[4]), .Y(n35) );
OR2X1_RVT U76 ( .A1(n67), .A2(n35), .Y(n29) );
OR2X1_RVT U77 ( .A1(n68), .A2(n29), .Y(n37) );
AND2X1_RVT U78 ( .A1(n30), .A2(n31), .Y(n34) );
OR2X1_RVT U79 ( .A1(n31), .A2(n30), .Y(n32) );
OR2X1_RVT U80 ( .A1(n34), .A2(n33), .Y(n70) );
OR2X1_RVT U81 ( .A1(n35), .A2(n70), .Y(n36) );
AND2X1_RVT U82 ( .A1(n37), .A2(n36), .Y(n75) );
AND2X1_RVT U83 ( .A1(n74), .A2(n75), .Y(n78) );
AND2X1_RVT U84 ( .A1(n38), .A2(A[5]), .Y(n79) );
INVX1_RVT U85 ( .A(B[6]), .Y(n40) );
AND2X1_RVT U86 ( .A1(n40), .A2(A[6]), .Y(n45) );
OR2X1_RVT U87 ( .A1(n79), .A2(n45), .Y(n39) );
OR2X1_RVT U88 ( .A1(n78), .A2(n39), .Y(n47) );
AND2X1_RVT U89 ( .A1(n40), .A2(n41), .Y(n44) );
OR2X1_RVT U90 ( .A1(n41), .A2(n40), .Y(n42) );
OR2X1_RVT U91 ( .A1(n44), .A2(n43), .Y(n81) );
OR2X1_RVT U92 ( .A1(n45), .A2(n81), .Y(n46) );
AND2X1_RVT U93 ( .A1(n47), .A2(n46), .Y(n86) );
AND2X1_RVT U94 ( .A1(n85), .A2(n86), .Y(n87) );
AND2X1_RVT U95 ( .A1(n48), .A2(A[7]), .Y(n49) );
AND2X1_RVT U96 ( .A1(n53), .A2(n52), .Y(N18) );
OR2X1_RVT U97 ( .A1(n56), .A2(n57), .Y(n60) );
AND2X1_RVT U98 ( .A1(n57), .A2(n56), .Y(n58) );
AND2X1_RVT U99 ( .A1(n60), .A2(n59), .Y(N19) );
OR2X1_RVT U100 ( .A1(n64), .A2(n63), .Y(n66) );
```

```
Terminal - ws2_26@ws2:~/SRM_Workshop/DC/results
File  Edit  View  Terminal  Tabs  Help
  OR2X1_RVT U79 ( .A1(n31), .A2(n30), .Y(n32) );
  OR2X1_RVT U80 ( .A1(n34), .A2(n33), .Y(n70) );
  OR2X1_RVT U81 ( .A1(n35), .A2(n70), .Y(n36) );
  AND2X1_RVT U82 ( .A1(n37), .A2(n36), .Y(n75) );
  AND2X1_RVT U83 ( .A1(n74), .A2(n75), .Y(n78) );
  AND2X1_RVT U84 ( .A1(n38), .A2(A[5]), .Y(n79) );
  INVX1_RVT U85 ( .A(B[6]), .Y(n40) );
  AND2X1_RVT U86 ( .A1(n40), .A2(A[6]), .Y(n45) );
  OR2X1_RVT U87 ( .A1(n79), .A2(n45), .Y(n39) );
  OR2X1_RVT U88 ( .A1(n78), .A2(n39), .Y(n47) );
  AND2X1_RVT U89 ( .A1(n40), .A2(n41), .Y(n44) );
  OR2X1_RVT U90 ( .A1(n41), .A2(n40), .Y(n42) );
  OR2X1_RVT U91 ( .A1(n44), .A2(n43), .Y(n81) );
  OR2X1_RVT U92 ( .A1(n45), .A2(n81), .Y(n46) );
  AND2X1_RVT U93 ( .A1(n47), .A2(n46), .Y(n86) );
  AND2X1_RVT U94 ( .A1(n85), .A2(n86), .Y(n87) );
  AND2X1_RVT U95 ( .A1(n48), .A2(A[7]), .Y(n49) );
  AND2X1_RVT U96 ( .A1(n53), .A2(n52), .Y(N18) );
  OR2X1_RVT U97 ( .A1(n56), .A2(n57), .Y(n60) );
  AND2X1_RVT U98 ( .A1(n57), .A2(n56), .Y(n58) );
  AND2X1_RVT U99 ( .A1(n60), .A2(n59), .Y(N19) );
  OR2X1_RVT U100 ( .A1(n64), .A2(n63), .Y(n66) );
  AND2X1_RVT U101 ( .A1(n66), .A2(n65), .Y(N20) );
  OR2X1_RVT U102 ( .A1(n69), .A2(n70), .Y(n73) );
  AND2X1_RVT U103 ( .A1(n70), .A2(n69), .Y(n71) );
  AND2X1_RVT U104 ( .A1(n73), .A2(n72), .Y(N21) );
  AND2X1_RVT U105 ( .A1(n77), .A2(n76), .Y(N22) );
  OR2X1_RVT U106 ( .A1(n80), .A2(n81), .Y(n84) );
  AND2X1_RVT U107 ( .A1(n81), .A2(n80), .Y(n82) );
  AND2X1_RVT U108 ( .A1(n84), .A2(n83), .Y(N23) );
  AND2X1_RVT U109 ( .A1(n89), .A2(n88), .Y(N24) );
endmodule
```

We are done with the RTL Synthesis step.

2. FLOORPLAN

- A floorplan is basically a blueprint for organizing stuff, like processors, memory, and input/output pads, on a chip.
- It's all about figuring out where to put each part, how big they should be, and how they connect.
- This planning is key to making the chip run faster, use less power, and take up less space.

To create the floorplan of the chip, we will invoke icc2_
shell in th ICCII Directory of SRM_WORKSHOP Directory.
After invoking icc2_shell we will start gui (to get the floorplan design) then we will open floorplan.tcl file from the script directory of ICCII directory in other terminal and execute all the commands one by one.

```
icc2_shell> read_verilog {./../DC/results/sub8bit.mapped.v} -library SUB8BIT_LIB
 -design sub8bit -top sub8bit
Information: Reading Verilog into new design 'sub8bit' in library 'SUB8BIT_LIB'.
 (VR-012)
Loading verilog file '/ve/ws_home/ws2_26/SRM_Workshop/DC/results/sub8bit.mapped.
v'
Number of modules read: 1
Top level ports: 26
Total ports in all modules: 26
Total nets in all modules: 125
Total instances in all modules: 108
Elapsed = 00:00:00.58, CPU = 00:00:00.07
1
icc2_shell> link_block
Using libraries: SUB8BIT_LIB saed32rvt_c
Linking block SUB8BIT_LIB:sub8bit.design
Information: User units loaded from library 'saed32rvt_c' (LNK-040)
Design 'sub8bit' was successfully linked.
1
icc2_shell>
```

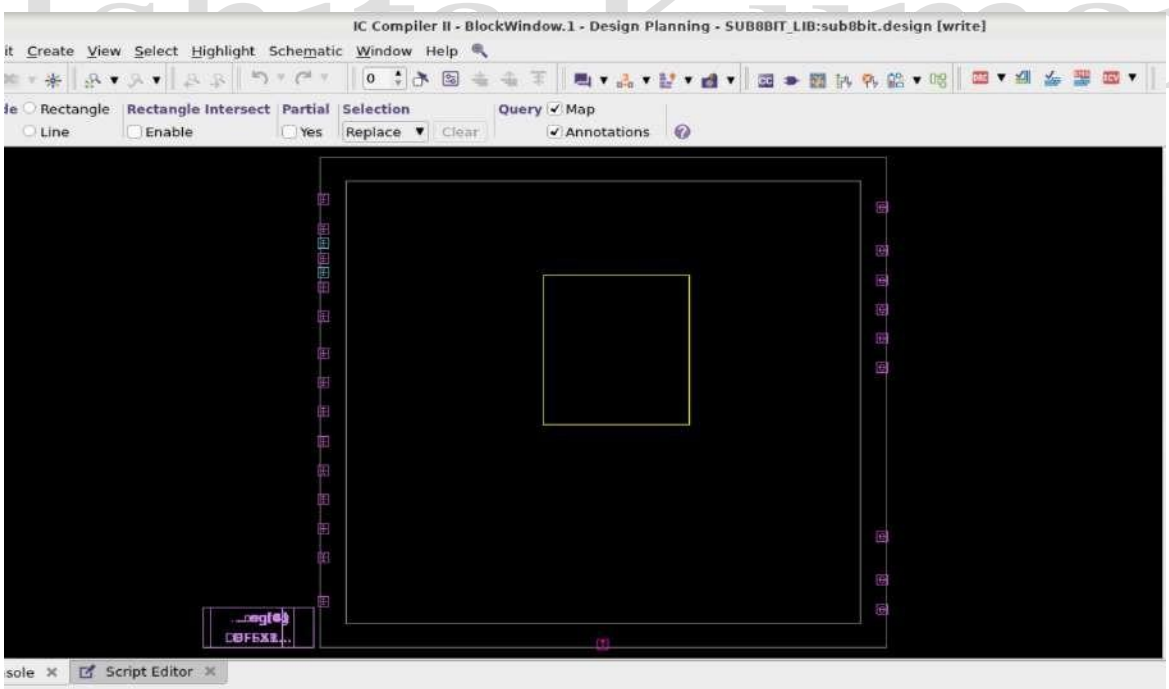
```
1
icc2_shell> initialize_floorplan -core_utilization 0.6 -coincident_boundary true
 -core_offset {1 1}
Removing existing floorplan objects
Creating core...
Core utilization ratio = 65.38%
Unplacing all cells...
Creating site array...
Creating routing tracks...
Initializing floorplan completed.
icc2_shell>
```

```
Number of block ports: 26
Number of block pin locations assigned from router: 0
CPU Time for Pin Preparation: 00:00:00.00u 00:00:00.00s 00:00:00.01e:
Number of PG ports on blocks: 0
Number of pins created: 26
CPU Time for Pin Creation: 00:00:00.00u 00:00:00.01s 00:00:00.02e:
Total Pin Placement CPU Time: 00:00:00.00u 00:00:00.04s 00:00:00.11e:
Information: Ending   'place_pins' (FLW-8001)
Information: Time: 2024-07-09 13:14:29 / Session:  00:25:59 / Command:  00:00:00
 / CPU:  00:00:00 / Memory: 454 MB (FLW-8100)
1
icc2_shell>
```

SPECIFICATIONS:

- Initialize the floorplan with 60% core utilization and coincident boundary with offset of {1 1}.
- Place input pins on side 1 and output pins on side 3.
- Create placement with high effort.

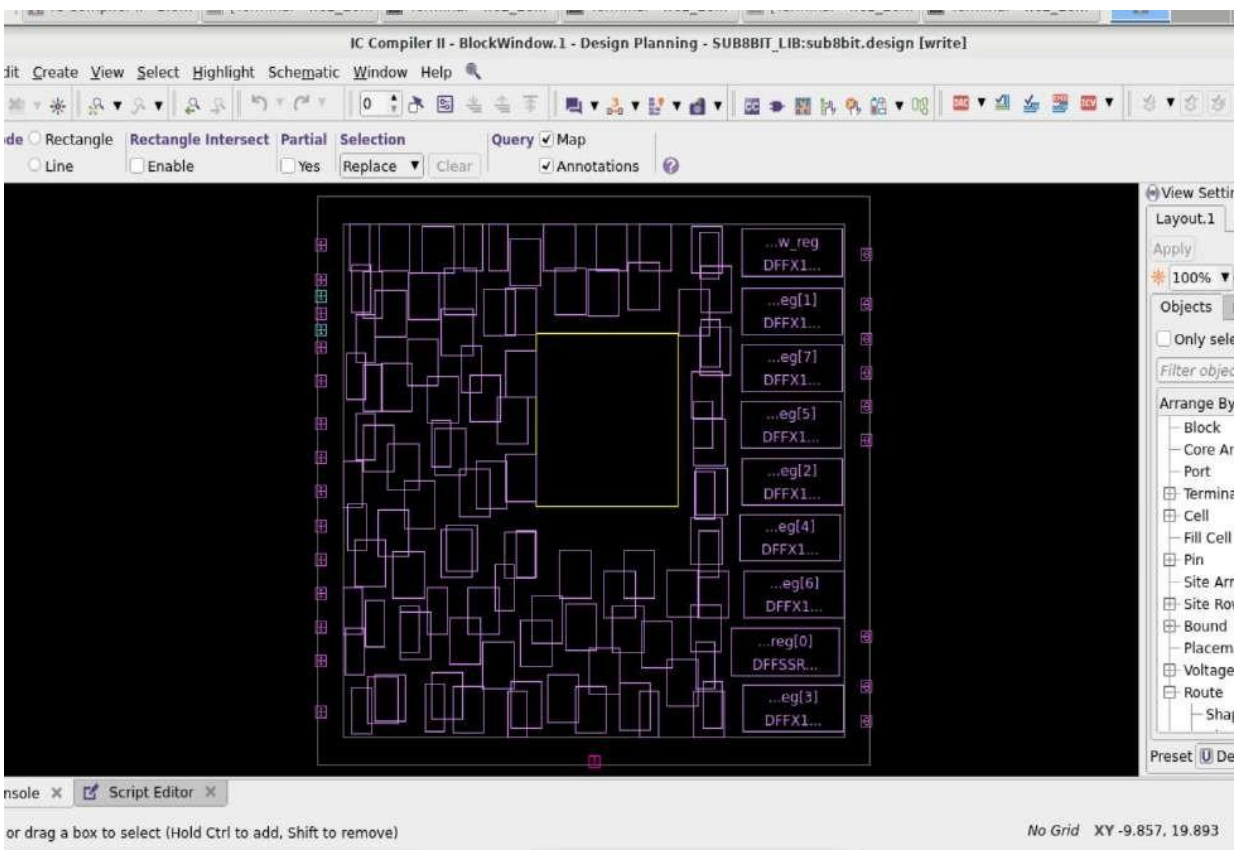
Ishita Kumari



Commands for Floorplanning:

```
cc2_shell> history
    1  start_gui
    2  set  PDK_PATH ./../ref
    3  create_lib -ref_lib $PDK_PATH/lib/ndm/saed32rvt_c.ndm SUB8BIT_LIB
    4  read_verilog {./../DC/results/sub8bit.mapped.v} -library SUB8BIT_LIB -design sub8bit -top sub8bit
    5  link_block
    6  initialize_floorplan -core_utilization 0.6 -coincident_boundary true -core_offset {1 1}
    7  create_placement_blockage -type hard -boundary {{8.6 9.3} {8.6 15.5} {14.2 15.5} {15.5 9.3}}
    8  create_placement_blockage -type hard -boundary {{8.6 9.3} {8.6 15.5} {14.2 15.5} {14.2 9.3}}
    9  set_individual_pin_constraints -ports [get_ports {A B}] -sides "1" -pin_spacing_distance "1"
   10  set_individual_pin_constraints -ports [get_ports {A B}] -sides 1 -pin_spacing_distance 1
   11  set_individual_pin_constraints -ports [get_ports {diff borrow}] -sides 3 -pin_spacing_distance 1
   12  place_pins -self
   13  create_placement -floorplan -effort high
   14  save_block
   15  save_lib
```

Floorplanning Result:



3. POWERPLAN

- A Powerplan is like a map for how electricity flows through a computer chip.
- It's about setting up grids and connections to make sure every part of the chip gets enough power without any problems.
- This setup includes designing grids, rings, and special capacitors to reduce any drops in voltage or noise, which helps the chip work smoothly and reliably.

.

To create the powerplan of the chip, we will invoke icc2_
shell in th ICCII Directory of SRM_WORKSHOP Directory.
After invoking icc2_shell we will start gui (to get the powerplan design) then we will open powerplan.tcl file from the script directory of ICCII directory in other terminal and execute all the commands one by one.

Ishita Kumari

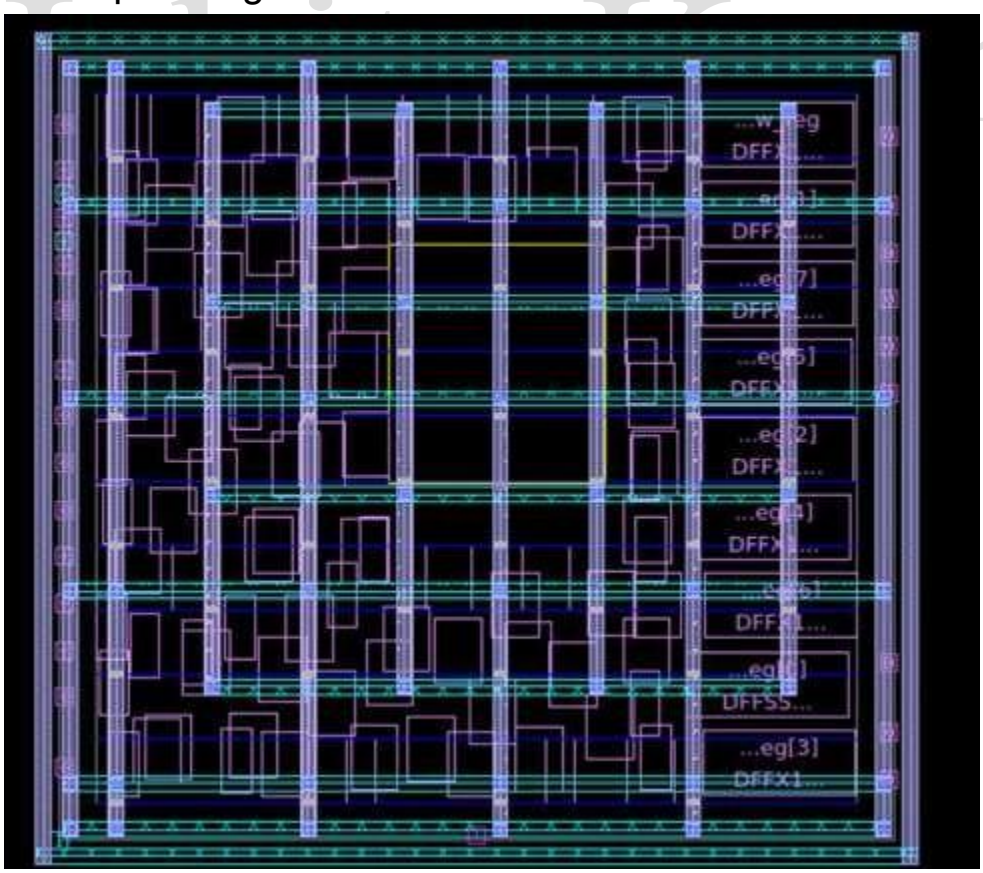
```
icc2_shell> create_net -power {VDD}
{VDD}
icc2_shell> create_net -ground {VSS}
{VSS}
icc2_shell>
icc2_shell> connect_pg_net -all_blocks -automatic
****************************************
Report : Power/Ground Connection Summary
Design : sub8bit
Version: V-2023.12
Date   : Tue Jul  9 13:44:25 2024
****************************************
P/G net name                  P/G pin count(previous/current)
--------------------------------------------------------------------------------
Power net VDD                 0/108
Ground net VSS                0/108
--------------------------------------------------------------------------------
Information: connections of 216 power/ground pin(s) are created or changed.
1
icc2_shell>
```

```
Successfully create PG ring pattern core_ring_pattern.
icc2_shell> set_pg_strategy core_power_ring -core -pattern {{name : core_ring_pattern}{nets : {
Successfully set PG strategy core_power_ring.
icc2_shell> compile_pg -strategies core_power_ring
Sanity check for inputs.
No strategy-level via rule is specified, the default rule will be applied.
Automatic PG net connection through connect_pg_net is disabled.
Updating PG strategies.
Updating strategy core_power_ring.
Loading library and design information.
Number of Standard Cells: 108
Number of Hard Macros: 0
Number of Pads: 0
Creating rings.
Creating via connection between strategies and existing shapes.
Via DRC checking runtime 0.00 seconds.
Via connection runtime: 0 seconds.
Removing dangling/floating wire/vias after DRC check.
Start iteration 1:
Checking potential dangling/floating power plan wires.
Checking dangling/floating vias inside strategy core_power_ring.
Checking 4 stacked vias:0% 20% 50% 70% 100%
Finish removing all dangling or floating wires and vias.
Commiting wires and vias.
Committing wires takes 0.00 seconds.
Committing vias takes 0.00 seconds.
Committed 8 wires.
Committed 4 vias.
Committed 0 wires for via creation.
Overall PG creation runtime: 1 seconds.
Successfully compiled PG.
Overall runtime: 1 seconds.
```

```
icc2_shell> set_pg_strategy core_mesh -pattern { {pattern:mesh} {nets: VDD VSS}} -core -extension {stop: innermost_ring}
Successfully set PG strategy core_mesh.
icc2_shell> compile_pg -strategies core_mesh
Sanity check for inputs.
No strategy-level via rule is specified, the default rule will be applied.
Automatic PG net connection through connect_pg_net is disabled.
Updating PG strategies.
Updating strategy core_mesh.
Loading library and design information.
Number of Standard Cells: 108
Number of Hard Macros: 0
Number of Pads: 0
Creating straps and vias in power plan.
Creating wire shapes for strategies core_mesh .
Creating wire shapes runtime: 0 seconds
Blockage cutting and DRC fixing for wire shapes for strategies core_mesh .
Check and fix DRC for 24 wires for strategy core_mesh.
Number of threads: 1
Number of partitions: 2
Direction of partitions: vertical
Number of wires: 16
Checking DRC for 16 wires:10% 100%
Number of wires: 8
Checking DRC for 8 wires:0% 10% 20% 30% 50% 60% 70% 80% 100%
Creating 24 wires after DRC fixing.
Wire DRC checking runtime 2.00 seconds.
Creating via shapes for strategies core_mesh .
Working on strategy core_mesh.
Number of detected intersections: 64
Total runtime of via shapes creation: 0 seconds
Check and fix DRC for 64 stacked vias for strategy core_mesh.
Number of vias: 64
Checking DRC for 64 stacked vias:0% 5% 10% 15% 20% 25% 30% 35% 40% 45% 50% 55% 60% 65% 70% 75% 80% 85% 90% 95% 100%
```

```
File  Edit  View  Terminal  Tabs  Help
Number of partitions: 2
Direction of partitions: horizontal
Number of wires: 12
Checking DRC for 12 wires:15% 100%
Creating 12 wires after DRC fixing.
Wire DRC checking runtime 0.00 seconds.
Creating via connection between strategies and existing shapes.
Check and fix DRCs for 80 stacked vias.
Number of vias: 80
Checking DRC for 80 stacked vias:0% 5% 10% 15% 20% 25% 30% 35% 40% 45% 50% 55% 60% 65% 70% 75% 80% 85% 90% 95% 100%
40 regular vias are not fixed
Via DRC checking runtime 1.00 seconds.
via connection runtime: 1 seconds.
Removing dangling/floating wire/vias after DRC check.
Start iteration 1:
Checking potential dangling/floating power plan wires.
Checking dangling/floating vias between strategies and existing shapes.
Checking 40 stacked vias:0% 10% 20% 30% 40% 50% 60% 70% 80% 90% 100%
Start iteration 2:
Checking potential dangling/floating power plan wires.
Checking dangling/floating vias between strategies and existing shapes.
Checking 40 stacked vias:0% 10% 20% 30% 40% 50% 60% 70% 80% 90% 100%
Finish removing all dangling or floating wires and vias.
Commiting wires and vias.
Committing wires takes 0.00 seconds.
Committing vias takes 0.00 seconds.
Committed 12 wires.
Committed 200 vias.
Committed 0 wires for via creation.
Overall PG creation runtime: 1 seconds.
Successfully compiled PG.
Overall runtime: 1 seconds.
1
icc2_shell>
```

Powerplanning Result:



Commands for Power Planning:

```
save_lib
create_net -power {VDD}
create_net -ground {VSS}
connect_pg_net -all_blocks -automatic
create_pg_ring_pattern core_ring_pattern -horizontal_layer M7 -horizontal_width .4 -horizontal_spacing .3 -vertical_layer M8 -vertical_width .4
vertical_spacing .3
set_pg_strategy core_power_ring -core -pattern {{name : core_ring_pattern}{nets : {VDD VSS}}{offset : {.5 .5}}}
compile_pg -strategies core_power_ring
create_pg_mesh_pattern mesh -layers { {{vertical_layer: M6}{width: .34} {spacing: interleaving}{pitch: 5} {offset: .5}} {{horizontal_layer: M7}{
idth: .38} {spacing: interleaving} {pitch: 5} {offset: .5}} {{vertical_layer: M8}{width: .38} {spacing: interleaving}{pitch: 5} {offset: .5}}}
set_pg_strategy core_mesh -pattern { {pattern:mesh} {nets: VDD VSS}} -core -extension {stop: innermost_ring}
compile_pg -strategies core_mesh
create_pg_std_cell_conn_pattern std_cell_rail -layers {M1} -rail_width 0.06
set_pg_strategy rail_strat -core -pattern {{name: std_cell_rail} {nets: VDD VSS} }
compile_pg -strategies rail_strat
save_block
save_lib
history
```

4. PLACEMENT

- Placement means arranging different standard cells, macros, etc on a chip in the best way possible to meet design goals and make sure everything works well.
- It's about placing these parts so that the chip runs fast, uses less power, and doesn't take up too much space.
- This process also makes it easier to build the chip .

Ishita Kumari

To create the placement of the chip, we will invoke icc2_ shell in th ICCII Directory of SRM_WORKSHOP Directory.
After invoking icc2_shell we will start gui, then we will open placement.tcl file from the script directory of ICCII directory in other terminal and execute all the commands one by one.

```
File  Edit  View  Terminal  Tabs  Help
icc2_shell> set PDK_PATH ./../ref
./../ref
icc2_shell>
icc2_shell> check_design -checks pre_placement_stage
****************************************
 Report : check_design
 Options: { pre_placement_stage }
 Design : sub8bit
 Version: V-2023.12
 Date   : Thu Jul 11 13:44:55 2024
****************************************

Running mega-check 'pre_placement_stage':
    Running atomic-check 'design_mismatch'
    Running atomic-check 'scan_chain'
    Running atomic-check 'mv_design'
    Running atomic-check 'rp_constraints'
    Running atomic-check 'timing'
    Running atomic-check 'hier_pre_placement'

  *** EMS Message summary ***
  ------------------------------------------------------------------------------------------------
  Rule         Type   Count      Message
  ------------------------------------------------------------------------------------------------
  DFT-011      Info   1          The design has no scan chain defined in the scandef.
  TCK-001      Warn   20         The reported endpoint '%endpoint' is unconstrained. Reason: '%re...
  TCK-002      Warn   9          The register clock pin '%pin' has no fanin clocks. Mode:'%mode'.
  ------------------------------------------------------------------------------------------------
  Total 30 EMS messages : 0 errors, 29 warnings, 1 info.
  ------------------------------------------------------------------------------------------------

  *** Non-EMS message summary ***
  ------------------------------------------------------------------------------------------------
  Rule         Type   Count      Message
```

```
Running mega-check 'pre_placement_stage':
    Running atomic-check 'design_mismatch'
    Running atomic-check 'scan_chain'
    Running atomic-check 'mv_design'
    Running atomic-check 'rp_constraints'
    Running atomic-check 'timing'
    Running atomic-check 'hier_pre_placement'

  *** EMS Message summary ***
  ------------------------------------------------------------------------------------------------
  Rule         Type   Count      Message
  ------------------------------------------------------------------------------------------------
  DFT-011      Info   1          The design has no scan chain defined in the scandef.
  TCK-001      Warn   20         The reported endpoint '%endpoint' is unconstrained. Reason: '%re...
  TCK-002      Warn   9          The register clock pin '%pin' has no fanin clocks. Mode:'%mode'.
  ------------------------------------------------------------------------------------------------
  Total 30 EMS messages : 0 errors, 29 warnings, 1 info.
  ------------------------------------------------------------------------------------------------

  *** Non-EMS message summary ***
  ------------------------------------------------------------------------------------------------
  Rule         Type   Count      Message
  ------------------------------------------------------------------------------------------------
  NDMUI-173    Info   1          There are no relative placement groups in the design.
  ------------------------------------------------------------------------------------------------
  Total 1 non-EMS messages : 0 errors, 0 warnings, 1 info.
  ------------------------------------------------------------------------------------------------

Warning: EMS database "check_design.ems" already exists, over-writing it. (EMS-040)

Information: EMS database is saved to file 'check_design.ems'.
Information: Non-EMS messages are saved into file 'check_design2024Jul11134454.log'.
1
icc2_shell>
```

```
Information: Non-EMS messages are saved into file 'check_design2024Jul11134454.l
og'.
1
icc2_shell> current_mode
{default}
remove_modes -all; remove_corners -all; remove_scenarios -all
1
icc2_shell>
icc2_shell> set mode1 "func"
func
icc2_shell> set corner1 "nom"
nom
icc2_shell> set scenario1 "${mode1}::${corner1}"
func::nom
icc2_shell> create_mode $mode1
1
icc2_shell> create_corner $corner1
1
icc2_shell> create_scenario -name func::nom -mode func -corner nom
Created scenario func::nom for mode func and corner nom
All analysis types are activated.
{func::nom}
icc2_shell>
```

```
icc2_shell> source ./../CONSTRAINTS/sub8bit.sdc
Warning: Redefining clock 'Clock'.
        Previously defined at: /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 1 (UIC-034)
Warning: Negative clock uncertainty specified: -1 (UIC-038)
Warning: Negative clock uncertainty specified: -1 (UIC-038)
1
icc2_shell> set_dont_use [get_lib_cells */FADD*]
Information: The design specific attribute override for lib_cell 'saed32rvt_c:FADDX1_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:FADDX2_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
1
icc2_shell> set_dont_use [get_lib_cells */HADD*]
Information: The design specific attribute override for lib_cell 'saed32rvt_c:HADDX1_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:HADDX2_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
1
icc2_shell> set_dont_use [get_lib_cells */AO*]
Information: The design specific attribute override for lib_cell 'saed32rvt_c:AO21X1_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:AO21X2_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:AO221X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:AO221X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:AO222X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:AO222X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:AO22X1_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:AO22X2_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
```

```
ual library setting may not be overwritten. (ATTR-12)
1
icc2_shell> set_dont_use [get_lib_cells */NAND*]
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NAND2X0_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NAND2X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NAND2X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NAND2X4_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NAND3X0_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NAND3X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NAND3X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NAND3X4_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NAND4X0_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NAND4X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
1
icc2_shell> set_dont_use [get_lib_cells */XOR*]
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XOR2X1_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XOR2X2_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XOR3X1_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XOR3X2_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
```

```
al library setting may not be overwritten. (ATTR-12)
1
icc2_shell> set_dont_use [get_lib_cells */NOR*]
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR2X0_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR2X1_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR2X2_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR2X4_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR3X0_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR3X1_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR3X2_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR3X4_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR4X0_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR4X1_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
1
icc2_shell> set_dont_use [get_lib_cells */XNOR*]
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XNOR2X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XNOR2X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XNOR3X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XNOR3X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
1
```

```
al library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:NOR4X1_RVT.timing' is set in the current block 'sub8bit', because the actu
al library setting may not be overwritten. (ATTR-12)
1
icc2_shell> set_dont_use [get_lib_cells */XNOR*]
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XNOR2X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XNOR2X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XNOR3X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:XNOR3X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
1
icc2_shell> set_dont_use [get_lib_cells */MUX*]
Information: The design specific attribute override for lib_cell 'saed32rvt_c:MUX21X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:MUX21X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:MUX41X1_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:MUX41X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
1
icc2_shell>
icc2_shell>
```

```
ual library setting may not be overwritten. (ATTR-12)
Information: The design specific attribute override for lib_cell 'saed32rvt_c:MUX41X2_RVT.timing' is set in the current block 'sub8bit', because the act
ual library setting may not be overwritten. (ATTR-12)
1
icc2_shell>
set parasitic1 "p1"
p1
icc2_shell> set tluplus_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmax.tluplus"
./../ref/tech/star_rcxt/saed32nm_1p9m_Cmax.tluplus
icc2_shell> set layer_map_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
./../ref/tech/star_rcxt/saed32nm_tf_itf_tluplus.map
icc2_shell> set parasitic2 "p2"
p2
icc2_shell> set tluplus_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmin.tluplus"
./../ref/tech/star_rcxt/saed32nm_1p9m_Cmin.tluplus
icc2_shell> set layer_map_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
./../ref/tech/star_rcxt/saed32nm_tf_itf_tluplus.map
icc2_shell> read_parasitic_tech -tlup $tluplus_filep1 -layermap $layer_map_filep1 -name p1
NEX(WARNING): parasitic_tech file: /ve/ws_home/ws2_26/SRM_Workshop/ref/tech/star_rcxt/saed32nm_1p9m_Cmax.tluplus already read in, mandatory 1-to-1 map b
etween tluplus file and paraTech
1
icc2_shell> read_parasitic_tech -tlup $tluplus_filep2 -layermap $layer_map_filep2 -name p2
NEX(WARNING): parasitic_tech file: /ve/ws_home/ws2_26/SRM_Workshop/ref/tech/star_rcxt/saed32nm_1p9m_Cmin.tluplus already read in, mandatory 1-to-1 map b
etween tluplus file and paraTech
1
icc2_shell>
icc2_shell> set_parasitic_parameters -late_spec $parasitic1 -early_spec $parasitic2
1
icc2_shell> set_app_options -name place.coarse.continue_on_missing_scandef -value true
place.coarse.continue_on_missing_scandef true
icc2_shell>
icc2_shell> place_pins -self
Information: Starting 'place_pins' (FLW-8000)
Information: Time: 2024-07-11 14:07:12 / Session:  00:33:54 / Command:  00:00:00 / CPU:  00:00:00 / Memory: 564 MB (FLW-8100)
```

```
Information: Starting 'place_pins' (FLW-8000)
Information: Time: 2024-07-11 14:07:12 / Session:  00:33:54 / Command:  00:00:00 / CPU:  00:00:00 / Memory: 564 MB (FLW-8100)
Load DB...
CPU Time for load db: 00:00:00.00u 00:00:00.00s 00:00:00.00e:

Min routing layer: M1
Max routing layer: MRDL


CPU Time for Top Level Pre-Route Processing: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Warning: found large number of corner keepout wiretracks on side 1 of block sub8bit on layer M9 and there is no enough wire tracks available on this sid
e (DPPA-096)
Warning: found large number of corner keepout wiretracks on side 2 of block sub8bit on layer MRDL and there is no enough wire tracks available on this s
ide (DPPA-096)
Warning: found large number of corner keepout wiretracks on side 3 of block sub8bit on layer M9 and there is no enough wire tracks available on this sid
e (DPPA-096)
Warning: found large number of corner keepout wiretracks on side 4 of block sub8bit on layer MRDL and there is no enough wire tracks available on this s
ide (DPPA-096)
Cell Min-Routing-Layer = M1
Cell Max-Routing-Layer = MRDL
Turn off antenna since no rule is specified
Information: Option route.detail.force_end_on_preferred_grid will be ignored since none of the layers have preferred grid. (ZRT-703)
Warning: Cannot find a default contact code for layer CO. (ZRT-022)

Block Pin Constraint   Min Pin Max Pin Reserve
                       Layer   Layer   Layer    Feedthroughs
--------------------   ------  ------  ------   ------------
sub8bit                M2      MRDL    MRDL     Not allowed

Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 3.55 outside the layer range. (ZRT-707)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 3.55 outside the layer range on clock nets. (ZRT-718)
Information: When applicable layer based tapering will taper up to 0.00 in distance from the pin. (ZRT-706)
Warning: Master cell sub8bit has duplicated redundant library pin shapes at {-1.368 0.001} {-1.064 20.391} on layer M3. (ZRT-625)
Warning: Master cell sub8bit has duplicated redundant library pin shapes at {-1.368 0.001} {-1.064 20.391} on layer M3. (ZRT-625)
Warning: Master cell sub8bit has duplicated redundant library pin shapes at {-1.368 0.001} {-1.064 20.391} on layer M3. (ZRT-625)
```

```
[End of Build Tech Data] Total (MB): Used   49  Alloctr   49  Proc 4203
Net statistics:
Total number of nets to route for block pin placement     = 26
Number of interface nets to route for block pin placement = 26
Net length statistics:
Net Count(Ignore Fully Rted) 52, Total Half Perimeter Wire Length (HPWL) 600 microns
HPWL   0 ~   50 microns: Net Count       52     Total HPWL          600 microns
HPWL  50 ~  100 microns: Net Count        0     Total HPWL            0 microns
HPWL 100 ~  200 microns: Net Count        0     Total HPWL            0 microns
HPWL 200 ~  300 microns: Net Count        0     Total HPWL            0 microns
HPWL 300 ~  400 microns: Net Count        0     Total HPWL            0 microns
HPWL 400 ~  500 microns: Net Count        0     Total HPWL            0 microns
HPWL 500 ~  600 microns: Net Count        0     Total HPWL            0 microns
HPWL 600 ~  700 microns: Net Count        0     Total HPWL            0 microns
HPWL 700 ~  800 microns: Net Count        0     Total HPWL            0 microns
HPWL 800 ~  900 microns: Net Count        0     Total HPWL            0 microns
HPWL 900 ~ 1000 microns: Net Count        0     Total HPWL            0 microns
HPWL     > 1000 microns: Net Count        0     Total HPWL            0 microns
Current Stage stats:
[End of Build All Nets] Elapsed real time: 0:00:00
[End of Build All Nets] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build All Nets] Stage (MB): Used    0  Alloctr    0  Proc    2
[End of Build All Nets] Total (MB): Used   49  Alloctr   50  Proc 4206
Number of partitions: 1 (1 x 1)
Size of partitions: 9 gCells x 9 gCells
Average gCell capacity  17.22    on layer (1)    M1
Average gCell capacity  18.22    on layer (2)    M2
Average gCell capacity  8.56     on layer (3)    M3
Average gCell capacity  9.11     on layer (4)    M4
Average gCell capacity  4.22     on layer (5)    M5
Average gCell capacity  4.44     on layer (6)    M6
Average gCell capacity  2.00     on layer (7)    M7
Average gCell capacity  2.11     on layer (8)    M8
Average gCell capacity  1.00     on layer (9)    M9
Average gCell capacity  0.44     on layer (10)   MRDL
```

```
[End of Add Nets Demand] Elapsed real time: 0:00:00
[End of Add Nets Demand] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Add Nets Demand] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Add Nets Demand] Total (MB): Used   49  Alloctr   50  Proc 4206
Number of user frozen nets = 0
Total stats:
[End of Build Data] Elapsed real time: 0:00:00
[End of Build Data] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Build Data] Stage (MB): Used    1  Alloctr    1  Proc    2
[End of Build Data] Total (MB): Used   49  Alloctr   50  Proc 4206
Number of partitions: 1 (1 x 1)
Size of partitions: 9 gCells x 9 gCells
Current Stage stats:
[End of Blocked Pin Detection] Elapsed real time: 0:00:00
[End of Blocked Pin Detection] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Blocked Pin Detection] Stage (MB): Used   12  Alloctr   12  Proc   15
[End of Blocked Pin Detection] Total (MB): Used   61  Alloctr   62  Proc 4221
Information: Using 1 threads for routing. (ZRT-444)
Information: Buffer distance is estimated to be ~862.0000um (257 gCells)

Start GR phase 0
Number of partitions: 1 (1 x 1)
Size of partitions: 9 gCells x 9 gCells
[rtTop] Elapsed real time: 0:00:00
[rtTop] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
Current Stage stats:
[End of Initial Routing] Elapsed real time: 0:00:00
[End of Initial Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Initial Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Initial Routing] Total (MB): Used   61  Alloctr   62  Proc 4221
Initial. Routing result:
Initial. Both Dirs: Dmd-Cap  =     0 Max = 0 GRCs =     0 (0.00%)
Initial. H routing: Dmd-Cap  =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. V routing: Dmd-Cap  =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
```

```
Initial. Layer M8 wire length = 0.00
Initial. Layer M9 wire length = 0.00
Initial. Layer MRDL wire length = 0.00
Initial. Total Number of Contacts = 53
Initial. Via VIA12SQ_C count = 26
Initial. Via VIA23SQ_C count = 26
Initial. Via VIA34SQ_C count = 1
Initial. Via VIA45SQ_C count = 0
Initial. Via VIA56SQ_C count = 0
Initial. Via VIA67SQ_C count = 0
Initial. Via VIA78SQ_C count = 0
Initial. Via VIA89_C count = 0
Initial. Via VIA9RDL count = 0
Initial. completed.
[End of Whole Chip Routing] Elapsed real time: 0:00:00
[End of Whole Chip Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Whole Chip Routing] Stage (MB): Used   13  Alloctr   13  Proc   18
[End of Whole Chip Routing] Total (MB): Used   61  Alloctr   62  Proc 4221
[End of Global Routing] Elapsed real time: 0:00:00
[End of Global Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Global Routing] Stage (MB): Used   12  Alloctr   13  Proc   18
[End of Global Routing] Total (MB): Used   61  Alloctr   62  Proc 4221
[End of dbOut] Elapsed real time: 0:00:00
[End of dbOut] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of dbOut] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of dbOut] Total (MB): Used   53  Alloctr   53  Proc 4221
CPU Time for Global Route: 00:00:00.11u 00:00:00.00s 00:00:00.15e:
Number of block ports: 26
Number of block pin locations assigned from router: 26
CPU Time for Pin Preparation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Number of PG ports on blocks: 0
Number of pins created: 26
CPU Time for Pin Creation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Total Pin Placement CPU Time: 00:00:00.11u 00:00:00.00s 00:00:00.16e:
```

```
Initial. Via VIA12SQ_C count = 26
Initial. Via VIA23SQ_C count = 26
Initial. Via VIA34SQ_C count = 1
Initial. Via VIA45SQ_C count = 0
Initial. Via VIA56SQ_C count = 0
Initial. Via VIA67SQ_C count = 0
Initial. Via VIA78SQ_C count = 0
Initial. Via VIA89_C count = 0
Initial. Via VIA9RDL count = 0
Initial. completed.
[End of Whole Chip Routing] Elapsed real time: 0:00:00
[End of Whole Chip Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Whole Chip Routing] Stage (MB): Used   13  Alloctr   13  Proc   18
[End of Whole Chip Routing] Total (MB): Used   61  Alloctr   62  Proc 4221
[End of Global Routing] Elapsed real time: 0:00:00
[End of Global Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Global Routing] Stage (MB): Used   12  Alloctr   13  Proc   18
[End of Global Routing] Total (MB): Used   61  Alloctr   62  Proc 4221
[End of dbOut] Elapsed real time: 0:00:00
[End of dbOut] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of dbOut] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of dbOut] Total (MB): Used   53  Alloctr   53  Proc 4221
CPU Time for Global Route: 00:00:00.11u 00:00:00.00s 00:00:00.15e:
Number of block ports: 26
Number of block pin locations assigned from router: 26
CPU Time for Pin Preparation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Number of PG ports on blocks: 0
Number of pins created: 26
CPU Time for Pin Creation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Total Pin Placement CPU Time: 00:00:00.11u 00:00:00.00s 00:00:00.16e:
Information: Ending   'place_pins' (FLW-8001)
Information: Time: 2024-07-11 14:07:13 / Session:  00:33:54 / Command:  00:00:00 / CPU:  00:00:00 / Memory: 611 MB (FLW-8100)
1
icc2_shell>
```

```
Legalization complete (0 total sec)

****************************************
  Report : Placement Attempts
  Site   : unit
****************************************

number of cells:                      103
number of references:                  16
number of site rows:                   11
number of locations attempted:       1367
number of locations failed:             0  (0.0%)

Legality of references at locations:
0 references had failures.

Legality of references in rows:
0 references had row failures.

****************************************
  Report : Cell Displacements
****************************************

number of cells aggregated:           103 (905 total sites)
avg row height over cells:          1.672 um
rms cell displacement:              0.000 um ( 0.00 row height)
rms weighted cell displacement:     0.000 um ( 0.00 row height)
max cell displacement:              0.000 um ( 0.00 row height)
avg cell displacement:              0.000 um ( 0.00 row height)
avg weighted cell displacement:     0.000 um ( 0.00 row height)
number of cells moved:                  0
number of large displacements:          0
large displacement threshold:       3.000 row height
```

```
Layer Demotion Info:
Bin                     OptDist       MinLen      BeforeCount       AfterCount        Diff
-----------------------------------------------------------------------------------------
None                      211.6         0.0            120              120           0
M2                        213.1        21.2              0                0           0
-----------------------------------------------------------------------------------------
Total Demoted Nets:            0


Place-opt optimization Phase 60 Iter  1        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954
INFO: New Levelizer turned on
Place-opt optimization Phase 60 Iter  2        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954
Place-opt optimization Phase 60 Iter  3        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954

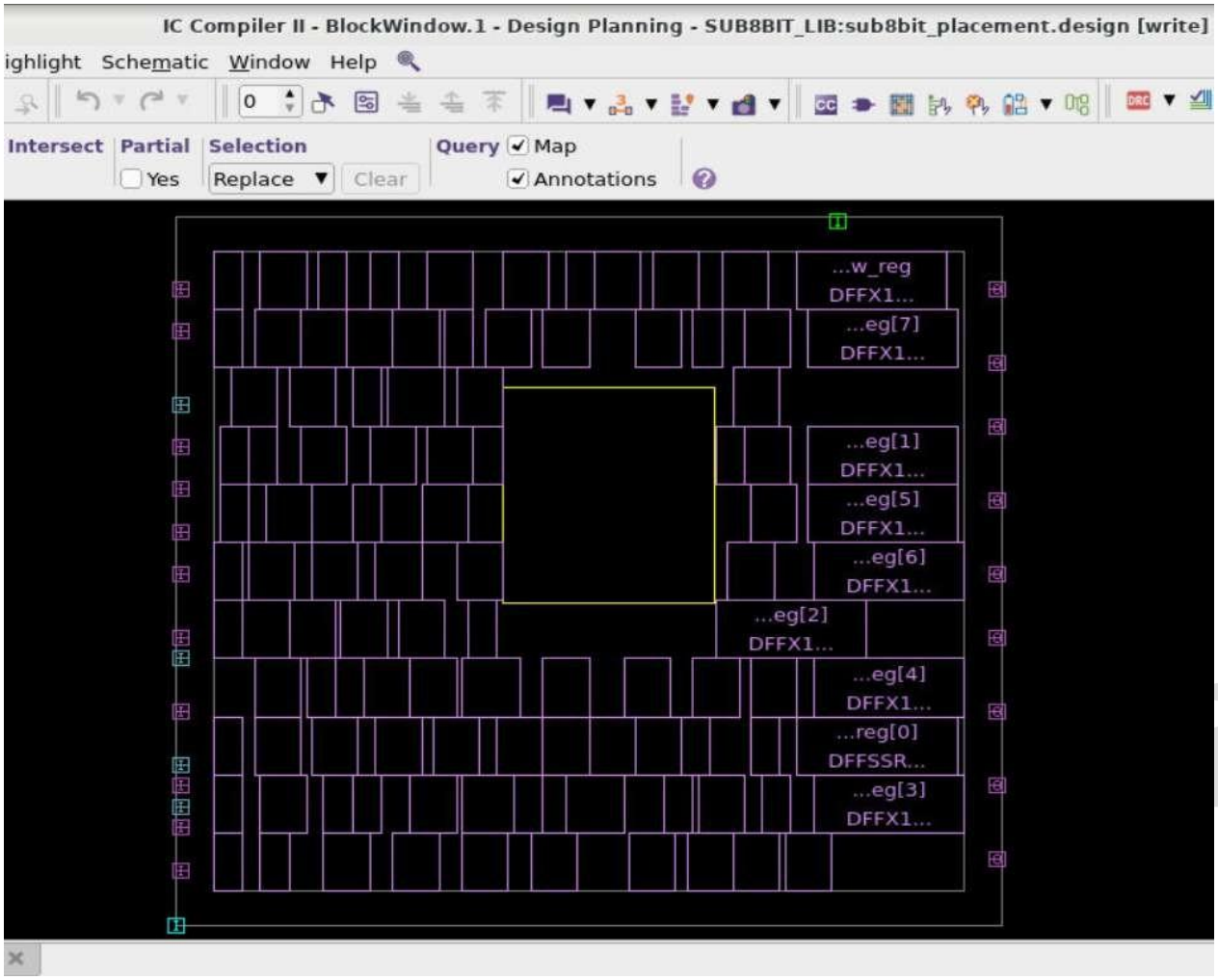
CCL: Total Usage Adjustment : 1
INFO: Derive row count 3 from GR congestion map (13/4)
INFO: Derive col count 3 from GR congestion map (13/4)
Convert timing mode ...
Place-opt optimization Phase 61 Iter  1        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954
Place-opt optimization Phase 61 Iter  2        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954
Place-opt optimization Phase 61 Iter  3        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954
Place-opt optimization Phase 61 Iter  4        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954
Place-opt optimization Phase 61 Iter  5        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954
Place-opt optimization Phase 61 Iter  6        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954
Corner Scaling is off, multiplier is 1.000000
Using default layer M4
new cutoff lpd: 2.13436e-02
corner scaling: maxCornerId = 1
corner=nom, tran factor=1.000000 (0.113319 / 0.113319)
bmap: stepx = stepy = 83600
creating bmap
DB units per micron : 10000
Place-opt optimization Phase 61 Iter  7        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954
Place-opt optimization Phase 61 Iter  8        0.00       0.00      0.00        0       230.00  478598592.00        103            0.63       954
```

```
Cell: U67 (AND2X1_RVT)
  Input location: (3.584,9.36)
  Legal location: (3.584,9.36)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U64 (AND2X1_RVT)
  Input location: (3.584,4.344)
  Legal location: (3.584,4.344)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U61 (AND2X1_RVT)
  Input location: (1.912,9.36)
  Legal location: (1.912,9.36)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U59 (AND2X1_RVT)
  Input location: (2.064,6.016)
  Legal location: (2.064,6.016)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U13 (AND2X1_RVT)
  Input location: (8.448,4.344)
  Legal location: (8.448,4.344)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U58 (AND2X1_RVT)
  Input location: (6.168,6.016)
  Legal location: (6.168,6.016)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U54 (AND2X1_RVT)
  Input location: (2.976,7.688)
  Legal location: (2.976,7.688)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U50 (AND2X1_RVT)
  Input location: (3.28,12.704)
  Legal location: (3.28,12.704)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U46 (AND2X1_RVT)
  Input location: (8.144,16.048)
  Legal location: (8.144,16.048)
```

```
  Legal location: (8.448,4.344)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U58 (AND2X1_RVT)
  Input location: (6.168,6.016)
  Legal location: (6.168,6.016)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U54 (AND2X1_RVT)
  Input location: (2.976,7.688)
  Legal location: (2.976,7.688)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U50 (AND2X1_RVT)
  Input location: (3.28,12.704)
  Legal location: (3.28,12.704)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U46 (AND2X1_RVT)
  Input location: (8.144,16.048)
  Legal location: (8.144,16.048)
  Displacement:   0.000 um ( 0.00 row height)
Cell: U73 (AND2X1_RVT)
  Input location: (2.216,2.672)
  Legal location: (2.216,2.672)
  Displacement:   0.000 um ( 0.00 row height)

Legalization succeeded.
Total Legalizer CPU: 0.049
Total Legalizer Wall Time: 0.075
-----------------------------------------------------------
Information: Ending   'legalize_placement' (FLW-8001)
Information: Time: 2024-07-11 14:15:58 / Session:  00:42:40 / Command:  00:00:00 / CPU:  00:00:00 / Memory: 954 MB (FLW-8100)
1
icc2_shell>
```

Result of Placement:



Report_design command:
It gives the report of the design that describes different types of cells and areas.

```
1
icc2_shell> report_design
****************************************
Report : design
Design : sub8bit
Version: V-2023.12
Date   : Thu Jul 11 14:19:44 2024
****************************************

Total number of std cells in library : 286
Total number of dont_use lib cells   : 85
Total number of dont_touch lib cells : 7
Total number of buffers              : 11
Total number of inverters            : 15
Total number of flip-flops           : 106
Total number of latches              : 12
Total number of ICGs                 : 12

Cell Instance Type  Count          Area
--------------------------------------
TOTAL LEAF CELLS       103       230.000
unit                   103       230.000
Standard cells         103       230.000
unit                   103       230.000
Hard macro cells         0         0.000
unit                   103       230.000
Soft macro cells         0         0.000
unit                   103       230.000
Always on cells          0         0.000
unit                   103       230.000
Physical only            0         0.000
unit                   103       230.000
Fixed cells              0         0.000
unit                   103       230.000
Moveable cells         103       230.000
```

Ishita Kumari

```
Hard macro cells          0          0.000
unit                    103        230.000
Soft macro cells          0          0.000
unit                    103        230.000
Always on cells           0          0.000
unit                    103        230.000
Physical only             0          0.000
unit                    103        230.000
Fixed cells               0          0.000
unit                    103        230.000
Moveable cells          103        230.000
unit                    103        230.000
Placed cells            103        230.000
unit                    103        230.000
Sequential                9         59.978
unit                    103        230.000
Buffer/inverter          30         38.122
unit                    103        230.000
ICG cells                 0          0.000
unit                    103        230.000

Logic Hierarchies                        : 0
Design Masters count                     : 8
Total Flat nets count                    : 122
Total FloatingNets count                 : 0
Total no of Ports                        : 28
Number of Master Clocks in design        : 1
Number of Generated Clocks in design     : 0
Number of Path Groups in design          : 7 (1 of them Non Default)
Number of Scan Chains in design          : 0
List of Modes                            : func
List of Corners                          : nom
List of Scenarios                        : func::nom

Core Area                                : 363.426
```

```
Logic Hierarchies                        : 0
Design Masters count                     : 8
Total Flat nets count                    : 122
Total FloatingNets count                 : 0
Total no of Ports                        : 28
Number of Master Clocks in design        : 1
Number of Generated Clocks in design     : 0
Number of Path Groups in design          : 7 (1 of them Non Default)
Number of Scan Chains in design          : 0
List of Modes                            : func
List of Corners                          : nom
List of Scenarios                        : func::nom

Core Area                                : 363.426
Chip Area                                : 443.730
Total Site Row Area                      : 363.426
Number of Blockages                      : 1
Total area of Blockages                  : 34.720
Number of Power Domains                  : 1
Number of Voltage Areas                  : 1
Number of Group Bounds                   : 0
Number of Exclusive MoveBounds           : 0
Number of Hard or Soft MoveBounds        : 0
Number of Multibit Registers             : 0
Number of Multibit LS/ISO Cells          : 0
Number of Top Level RP Groups            : 0
Number of Tech Layers                    : 71 (61 of them have unknown routing dir.)

Total wire length                        : 0.00 micron
Total number of wires                    : 0
Total number of contacts                 : 0
1
icc2_shell>
```

Report_timing command:
It gives the delay, timing path and slack of the design.

```
Total number of wires                    : 0
Total number of contacts                 : 0
1
icc2_shell> report_timing
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -report_by design
Design : sub8bit
Version: V-2023.12
Date   : Thu Jul 11 14:20:46 2024
****************************************

  Startpoint: B[1] (input port clocked by Clock)
  Endpoint: diff_reg[7] (rising edge-triggered flip-flop clocked by Clock)
  Mode: func
  Corner: nom
  Scenario: func::nom
  Path Group: **in2reg_default**
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------
  clock Clock (rise edge)                                 0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  input external delay                                    0.60       0.60 f
  B[1] (in)                                               0.00       0.60 f
  U53/Y (INVX0_RVT)                                       0.05       0.65 r
  U55/Y (OR2X1_RVT)                                       0.04       0.69 r
  U32/Y (INVX0_RVT)                                       0.01       0.71 f
  U56/Y (OR2X1_RVT)                                       0.03       0.74 f
  U58/Y (AND2X1_RVT)                                      0.04       0.77 f
```

```
File  Edit  View  Terminal  Tabs  Help
  B[1] (in)                                               0.00       0.60 f
  U53/Y (INVX0_RVT)                                       0.05       0.65 r
  U55/Y (OR2X1_RVT)                                       0.04       0.69 r
  U32/Y (INVX0_RVT)                                       0.01       0.71 f
  U56/Y (OR2X1_RVT)                                       0.03       0.74 f
  U58/Y (AND2X1_RVT)                                      0.04       0.77 f
  ctmTdsLR_1_2/Y (OR3X2_RVT)                              0.03       0.81 f
  ctmTdsLR_1_3/Y (AND3X1_RVT)                             0.04       0.85 f
  ctmTdsLR_1_4/Y (OR3X2_RVT)                              0.03       0.89 f
  U82/Y (AND2X1_RVT)                                      0.04       0.92 f
  U83/Y (AND2X1_RVT)                                      0.04       0.96 f
  ctmTdsLR_1_5/Y (OR3X2_RVT)                              0.03       0.99 f
  U93/Y (AND2X1_RVT)                                      0.03       1.03 f
  U94/Y (AND2X1_RVT)                                      0.03       1.06 f
  U20/Y (INVX0_RVT)                                       0.01       1.07 r
  U109/Y (AND2X1_RVT)                                     0.03       1.10 r
  diff_reg[7]/D (DFFX1_RVT)                               0.00       1.10 r
  data arrival time                                                  1.10

  clock Clock (rise edge)                                 1.00       1.00
  clock network delay (ideal)                             0.00       1.00
  diff_reg[7]/CLK (DFFX1_RVT)                             0.00       1.00 r
  clock uncertainty                                       1.00       2.00
  library setup time                                     -0.03       1.97
  data required time                                                 1.97
  -----------------------------------------------------------------------
  data required time                                                 1.97
  data arrival time                                                 -1.10
  -----------------------------------------------------------------------
  slack (MET)                                                        0.87

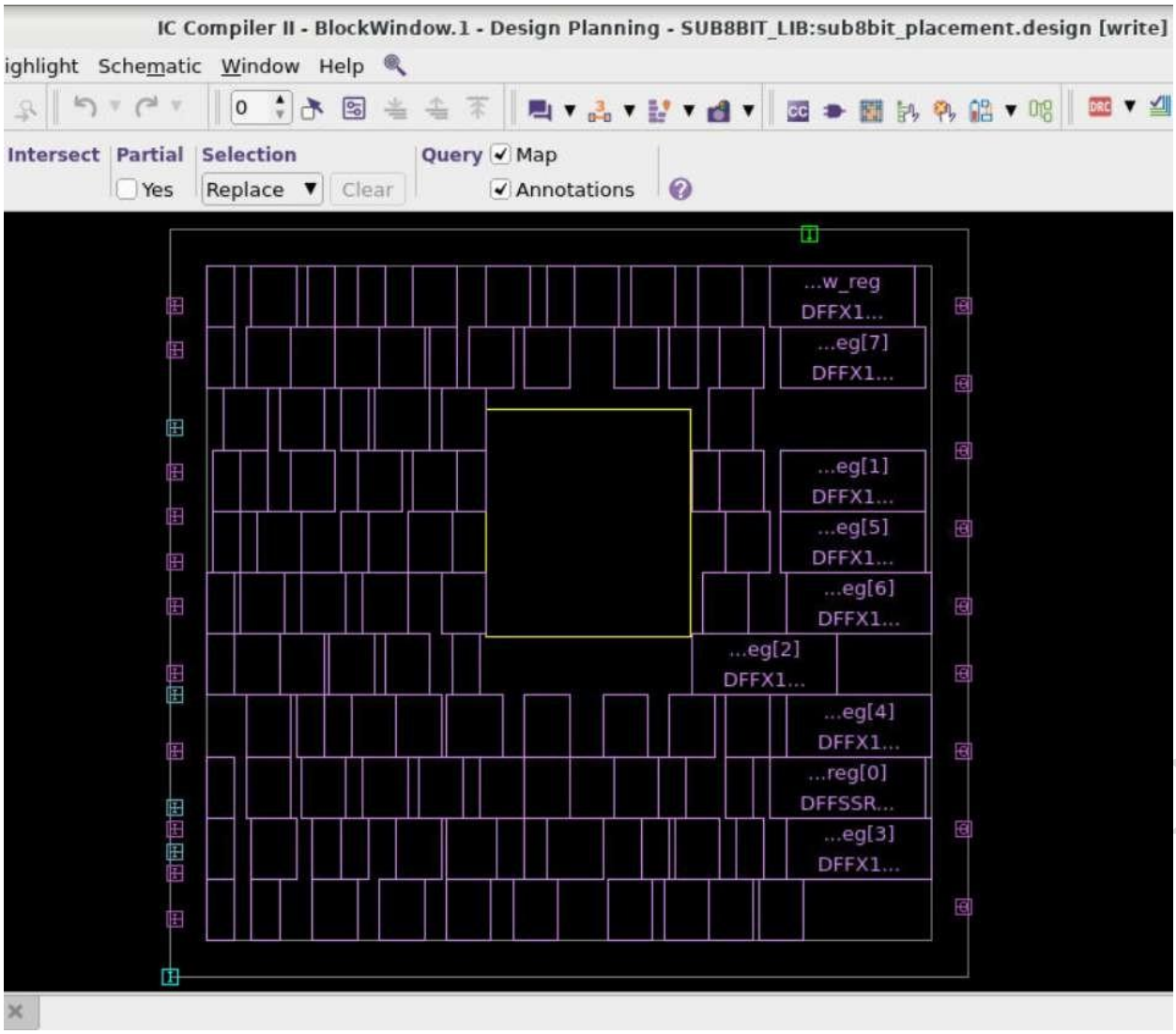

1
icc2_shell>
```

Commands for Placement:

```
save_lib
history
set PDK_PATH ./../ref
set PDK_PATH ./../ref
check_design -checks pre_placement_stage
current_mode
remove_modes -all; remove_corners -all; remove_scenarios -all
set mode1 "func"
set corner1 "nom"
set scenario1 "${mode1}::${corner1}"
create_mode $mode1
create_corner $corner1
create_scenario -name func::nom -mode func -corner nom
eport_scenarios
report_scenarios
source ./..CONSTRAINTS/sub8bit.sdc
source ./../CONSTRAINTS/sub8bit.sdc
source ./../CONSTRAINTS/sub8bit.sdc
set_dont_use [get_lib_cells */FADD*]
set_dont_use [get_lib_cells */HADD*]
set_dont_use [get_lib_cells */AO*]
set_dont_use [get_lib_cells */OA*]
set_dont_use [get_lib_cells */NAND*]
set_dont_use [get_lib_cells */XOR*]
set_dont_use [get_lib_cells */NOR*]
set_dont_use [get_lib_cells */XNOR*]
set_dont_use [get_lib_cells */MUX*]
set parasitic1 "p1"
set tluplus_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmax.tluplus"
set layer_map_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
set parasitic2 "p2"
set tluplus_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmin.tluplus"
set layer_map_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
read_parasitic_tech -tlup $tluplus_filep1 -layermap $layer_map_filep1 -name p1
read_parasitic_tech -tlup $tluplus_filep2 -layermap $layer_map_filep2 -name p2
```

```
set_dont_use [get_lib_cells */OA*]
set_dont_use [get_lib_cells */NAND*]
set_dont_use [get_lib_cells */XOR*]
set_dont_use [get_lib_cells */NOR*]
set_dont_use [get_lib_cells */XNOR*]
set_dont_use [get_lib_cells */MUX*]
set parasitic1 "p1"
set tluplus_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmax.tluplus"
set layer_map_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
set parasitic2 "p2"
set tluplus_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmin.tluplus"
set layer_map_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
read_parasitic_tech -tlup $tluplus_filep1 -layermap $layer_map_filep1 -name p1
read_parasitic_tech -tlup $tluplus_filep2 -layermap $layer_map_filep2 -name p2
set_parasitic_parameters -late_spec $parasitic1 -early_spec $parasitic2
set_app_options -name place.coarse.continue_on_missing_scandef -value true
place_pins -self
place_opt
legalize_placement
save_block -as sub8bit_placement
save_lib
report_design
report_timing
history
icc2_shell>
```

Result of Placement:



5. CTC

CLOCK TREE SYNTHESIS

- It distributes the clock to the entire circuit to ensure minimum skew and latency.
- It ensures signal integrity and performance all across the circuit.

After placement of the chip, we will start with CTS.
We will open clock.tcl file from the script directory of ICCII directory in other terminal and execute all the commands one by one.

report_design:

```
1
icc2_shell> report_design
****************************************
Report : design
Design : sub8bit
Version: V-2023.12
Date   : Thu Jul 11 15:01:24 2024
****************************************

Total number of std cells in library : 286
Total number of dont_use lib cells   : 85
Total number of dont_touch lib cells : 7
Total number of buffers              : 11
Total number of inverters            : 15
Total number of flip-flops           : 106
Total number of latches              : 12
Total number of ICGs                 : 12

Cell Instance Type  Count          Area
--------------------------------------
TOTAL LEAF CELLS       104       235.083
unit                   104       235.083
Standard cells         104       235.083
unit                   104       235.083
Hard macro cells         0         0.000
unit                   104       235.083
Soft macro cells         0         0.000
unit                   104       235.083
Always on cells          0         0.000
unit                   104       235.083
Physical only            0         0.000
unit                   104       235.083
Fixed cells              0         0.000
unit                   104       235.083
Moveable cells         104       235.083
```

```
File  Edit  View  Terminal  Tabs  Help
Fixed cells                0          0.000
unit                     104        235.083
Moveable cells           104        235.083
unit                     104        235.083
Placed cells             103        230.000
unit                     104        235.083
Sequential                 9         59.978
unit                     104        235.083
Buffer/inverter           31         43.204
unit                     104        235.083
ICG cells                  0          0.000
unit                     104        235.083

Logic Hierarchies                        : 0
Design Masters count                     : 9
Total Flat nets count                    : 123
Total FloatingNets count                 : 0
Total no of Ports                        : 28
Number of Master Clocks in design        : 1
Number of Generated Clocks in design     : 0
Number of Path Groups in design          : 7 (1 of them Non Default)
Number of Scan Chains in design          : 0
List of Modes                            : func
List of Corners                          : nom
List of Scenarios                        : func::nom

Core Area                                : 363.426
Chip Area                                : 443.730
Total Site Row Area                      : 363.426
Number of Blockages                      : 1
Total area of Blockages                  : 34.720
Number of Power Domains                  : 1
Number of Voltage Areas                  : 1
Number of Group Bounds                   : 0
Number of Exclusive MoveBounds           : 0
```

```
Logic Hierarchies                        : 0
Design Masters count                     : 9
Total Flat nets count                    : 123
Total FloatingNets count                 : 0
Total no of Ports                        : 28
Number of Master Clocks in design        : 1
Number of Generated Clocks in design     : 0
Number of Path Groups in design          : 7 (1 of them Non Default)
Number of Scan Chains in design          : 0
List of Modes                            : func
List of Corners                          : nom
List of Scenarios                        : func::nom

Core Area                                : 363.426
Chip Area                                : 443.730
Total Site Row Area                      : 363.426
Number of Blockages                      : 1
Total area of Blockages                  : 34.720
Number of Power Domains                  : 1
Number of Voltage Areas                  : 1
Number of Group Bounds                   : 0
Number of Exclusive MoveBounds           : 0
Number of Hard or Soft MoveBounds        : 0
Number of Multibit Registers             : 0
Number of Multibit LS/ISO Cells          : 0
Number of Top Level RP Groups            : 0
Number of Tech Layers                    : 71 (61 of them have unknown routing dir.)

Total wire length                        : 17.42 micron
Total number of wires                    : 17
Total number of contacts                 : 388
1
icc2_shell>
```

report_timing:

```
Total number of contacts              : 388
icc2_shell> report_timing
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -report_by design
Design : sub8bit
Version: V-2023.12
Date   : Thu Jul 11 15:02:06 2024
****************************************

  Startpoint: B[1] (input port clocked by Clock)
  Endpoint: diff_reg[7] (rising edge-triggered flip-flop clocked by Clock)
  Mode: func
  Corner: nom
  Scenario: func::nom
  Path Group: **in2reg_default**
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------
  clock Clock (rise edge)                                 0.00       0.00
```

```
  Path Group: **in2reg_default**
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------
  clock Clock (rise edge)                                 0.00       0.00
  clock network delay (propagated)                        0.04       0.04
  input external delay                                    0.60       0.64 f
  B[1] (in)                                               0.00       0.64 f
  U53/Y (INVX0_RVT)                                       0.05       0.68 r
  U55/Y (OR2X1_RVT)                                       0.04       0.73 r
  U32/Y (INVX0_RVT)                                       0.01       0.74 f
  U56/Y (OR2X1_RVT)                                       0.03       0.77 f
  U58/Y (AND2X1_RVT)                                      0.04       0.80 f
  ctmTdsLR_1_2/Y (OR3X1_RVT)                              0.03       0.84 f
  ctmTdsLR_1_3/Y (AND3X1_RVT)                             0.04       0.88 f
  ctmTdsLR_1_4/Y (OR3X1_RVT)                              0.03       0.91 f
  U82/Y (AND2X1_RVT)                                      0.03       0.94 f
  U83/Y (AND2X1_RVT)                                      0.04       0.98 f
  ctmTdsLR_1_5/Y (OR3X1_RVT)                              0.03       1.01 f
  U93/Y (AND2X1_RVT)                                      0.03       1.04 f
  U94/Y (AND2X1_RVT)                                      0.03       1.08 f
  U20/Y (INVX0_RVT)                                       0.01       1.09 r
  U109/Y (AND2X1_RVT)                                     0.03       1.12 r
  diff_reg[7]/D (DFFX1_RVT)                               0.00       1.12 r
  data arrival time                                                  1.12

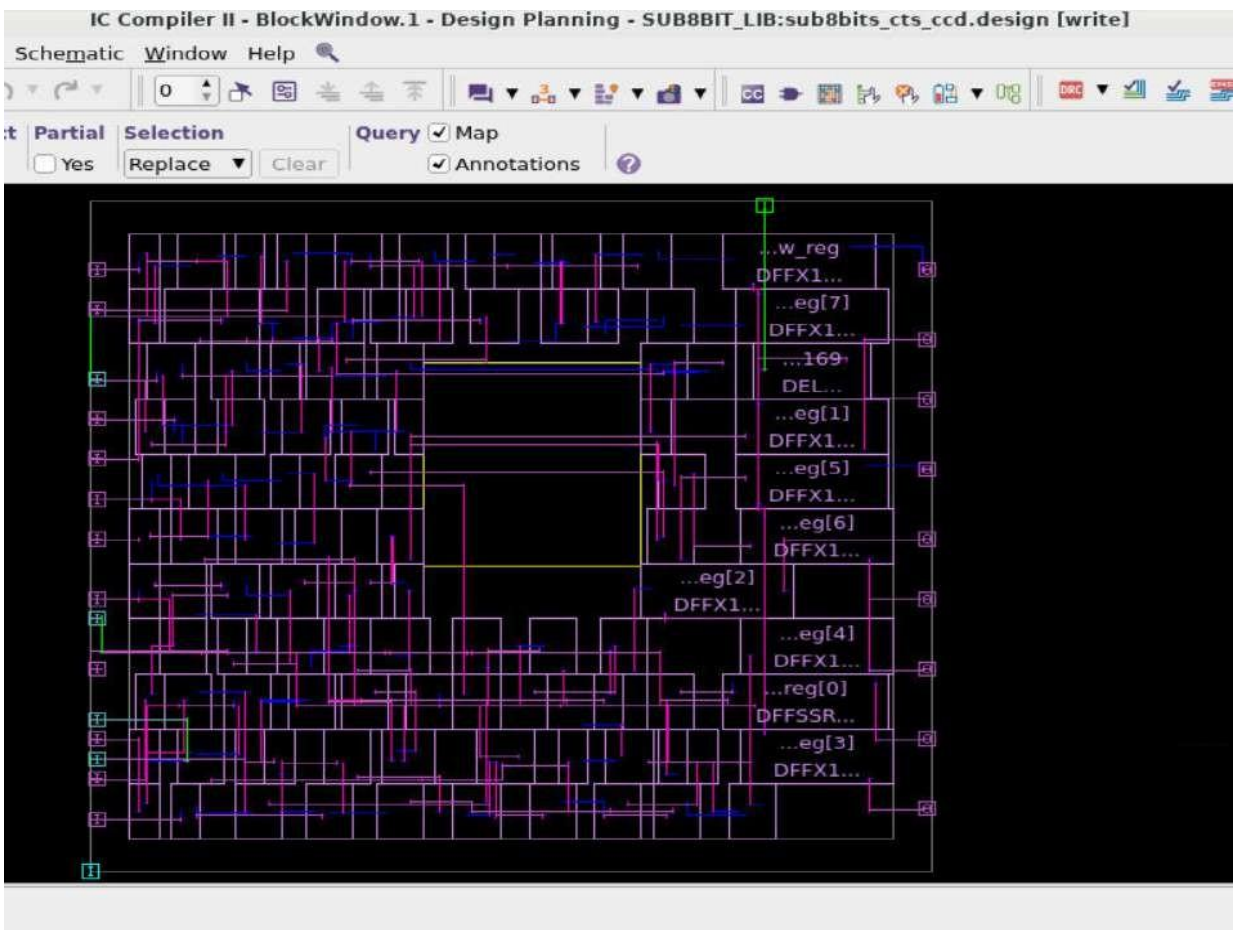
  clock Clock (rise edge)                                 1.00       1.00
  clock network delay (propagated)                        0.12       1.12
  diff_reg[7]/CLK (DFFX1_RVT)                             0.00       1.12 r
  clock uncertainty                                       1.00       2.12
  library setup time                                     -0.02       2.10
  data required time                                                 2.10
  -----------------------------------------------------------------------
  data required time                                                 2.10
```

```
  ctmTdsLR_1_2/Y (OR3X1_RVT)                          0.03      0.84 f
  ctmTdsLR_1_3/Y (AND3X1_RVT)                         0.04      0.88 f
  ctmTdsLR_1_4/Y (OR3X1_RVT)                          0.03      0.91 f
  U82/Y (AND2X1_RVT)                                  0.03      0.94 f
  U83/Y (AND2X1_RVT)                                  0.04      0.98 f
  ctmTdsLR_1_5/Y (OR3X1_RVT)                          0.03      1.01 f
  U93/Y (AND2X1_RVT)                                  0.03      1.04 f
  U94/Y (AND2X1_RVT)                                  0.03      1.08 f
  U20/Y (INVX0_RVT)                                   0.01      1.09 r
  U109/Y (AND2X1_RVT)                                 0.03      1.12 r
  diff_reg[7]/D (DFFX1_RVT)                           0.00      1.12 r
  data arrival time                                             1.12

  clock Clock (rise edge)                             1.00      1.00
  clock network delay (propagated)                    0.12      1.12
  diff_reg[7]/CLK (DFFX1_RVT)                         0.00      1.12 r
  clock uncertainty                                   1.00      2.12
  library setup time                                 -0.02      2.10
  data required time                                            2.10
  -------------------------------------------------------------------------
  data required time                                            2.10
  data arrival time                                            -1.12
  -------------------------------------------------------------------------
  slack (MET)                                                   0.98


1
icc2_shell>
```

Result of CTS:



Commands of CTS:

```
place_pins -self
place_opt
legalize_placement
save_block -as sub8bit_placement
save_lib
report_design
report_timing
history
check_design -checks pre_clock_tree_stage
synthesize_clock_tree
set_app_options -name cts.optimize.enable_local_skew -value true
set_app_options -name cts.compile.enable_local_skew -value true
set_app_options -name cts.compile.enable_global_route -value false
set_app_options -name clock_opt.flow.enable_ccd -value true
clock_opt
save_block -as sub8bits_cts_ccd
save_lib
report_design
report_timing
history
```

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6. ROUTING

- It involves creating connections in the chip between the placed components.
- It ensures signal integrity and meeting of design constraints.

After CTS process we will start with Routing.
First we will set all the necessary conditions from route.tcl file.

```
    69  history
set_app_options -name route.global.timing_driven -value true
route.global.timing_driven true
icc2_shell> set_app_options -name route.global.crosstalk_driven -value false
route.global.crosstalk_driven false
icc2_shell>
icc2_shell> set_app_options -name route.track.timing_driven -value true
route.track.timing_driven true
icc2_shell> set_app_options -name route.track.crosstalk_driven -value true
route.track.crosstalk_driven true
icc2_shell> set_app_options -name route.detail.timing_driven -value true
route.detail.timing_driven true
icc2_shell> set_app_options -name route.detail.force_max_number_iterations -valu
e false
route.detail.force_max_number_iterations false
icc2_shell> set_app_options -name route.detail.antenna -value true
route.detail.antenna true
icc2_shell> set_app_options -name route.detail.antenna_fixing_preference -value
use_diodes
route.detail.antenna_fixing_preference use_diodes
icc2_shell> set_app_options -name route.detail.diode_libcell_names -value */ANTE
NNA_RVT
route.detail.diode_libcell_names */ANTENNA_RVT
icc2_shell>
```

Route_details command:

```
[Track Assign: Done] Stage (MB): Used   -2  Alloctr   -2  Proc    0
[Track Assign: Done] Total (MB): Used    0  Alloctr    0  Proc 5044
icc2_shell> route_detail
Cell Min-Routing-Layer = M1
Cell Max-Routing-Layer = MRDL
Turn off antenna since no rule is specified
Information: Option route.detail.force_end_on_preferred_grid will be ignored since none of the layers have preferred grid. (ZRT-703)
Warning: Cannot find a default contact code for layer CO. (ZRT-022)
Warning: Port VDD of cell sub8bit
        is unplaced.  This may impact routing result. (ZRT-740)
Warning: Port VSS of cell sub8bit
        is unplaced.  This may impact routing result. (ZRT-740)
Warning: Ignore 2 top cell ports with no pins. (ZRT-027)
Info: number of net_type_blockage: 0
Information: Via ladder engine would be activated for pattern must join connection in certain commands. Please refer to man-page for the command list. (
ZRT-619)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 3.55 outside the layer range. (ZRT-707)
Information: When applicable Min-max layer allow_pin_connection mode will allow paths of length 3.55 outside the layer range on clock nets. (ZRT-718)
Information: When applicable layer based tapering will taper up to 0.00 in distance from the pin. (ZRT-706)
Loading timing information to the router from design
Timing information loaded to the router.
Printing options for 'route.common.*'
common.verbose_level                                  :        0

Printing options for 'route.detail.*'
detail.antenna                                        :        true
detail.antenna_fixing_preference                      :        use_diodes
detail.diode_libcell_names                            :        */ANTENNA_RVT
detail.force_max_number_iterations                    :        false
detail.timing_driven                                  :        true

Printing options for 'route.auto_via_ladder.*'
```

```
File  Edit  View  Terminal  Tabs  Help
detail.antenna                                        :        true
detail.antenna_fixing_preference                      :        use_diodes
detail.diode_libcell_names                            :        */ANTENNA_RVT
detail.force_max_number_iterations                    :        false
detail.timing_driven                                  :        true

Printing options for 'route.auto_via_ladder.*'

Information: RC layer preference is turned on for this design. (ZRT-613)
[Dr init] Elapsed real time: 0:00:00
[Dr init] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Dr init] Stage (MB): Used   29  Alloctr   29  Proc    0
[Dr init] Total (MB): Used   32  Alloctr   33  Proc 5044
Total number of nets = 123, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Information: Using 1 threads for routing. (ZRT-444)
Start DR iteration 0: uniform partition
Routed  1/4 Partitions, Violations =    0
Routed  2/4 Partitions, Violations =    0
Routed  3/4 Partitions, Violations =    1
Routed  4/4 Partitions, Violations =    0

DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0

[Iter 0] Elapsed real time: 0:00:00
[Iter 0] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[Iter 0] Stage (MB): Used   90  Alloctr   91  Proc    0
[Iter 0] Total (MB): Used   94  Alloctr   95  Proc 5044

End DR iteration 0 with 4 parts

Finish DR since reached 0 DRC

[DR] Elapsed real time: 0:00:00
```

```
File  Edit  View  Terminal  Tabs  Help
[Iter 0] Total (MB): Used   94  Alloctr   95  Proc 5044

End DR iteration 0 with 4 parts

Finish DR since reached 0 DRC

[DR] Elapsed real time: 0:00:00
[DR] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[DR] Stage (MB): Used   19  Alloctr   19  Proc    0
[DR] Total (MB): Used   22  Alloctr   23  Proc 5044
[DR: Done] Elapsed real time: 0:00:00
[DR: Done] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[DR: Done] Stage (MB): Used   19  Alloctr   19  Proc    0
[DR: Done] Total (MB): Used   22  Alloctr   23  Proc 5044

DR finished with 0 open nets, of which 0 are frozen

DR finished with 0 violations

DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0



Total Wire Length =                    538 micron
Total Number of Contacts =             506
Total Number of Wires =                510
Total Number of PtConns =              65
Total Number of Routed Wires =       502
Total Routed Wire Length =           531 micron
Total Number of Routed Contacts =       506
        Layer             M1 :         41 micron
        Layer             M2 :        225 micron
        Layer             M3 :        252 micron
        Layer             M4 :         10 micron
```

```
File  Edit  View  Terminal  Tabs  Help
Total Wire Length =                    538 micron
Total Number of Contacts =             506
Total Number of Wires =                510
Total Number of PtConns =              65
Total Number of Routed Wires =       502
Total Routed Wire Length =           531 micron
Total Number of Routed Contacts =       506
        Layer              M1 :         41 micron
        Layer              M2 :        225 micron
        Layer              M3 :        252 micron
        Layer              M4 :         10 micron
        Layer              M5 :          2 micron
        Layer              M6 :          0 micron
        Layer              M7 :          0 micron
        Layer              M8 :          0 micron
        Layer              M9 :          0 micron
        Layer            MRDL :          0 micron
        Via   VIA45SQ_C(rot) :          4
        Via        VIA34SQ_C :          7
        Via   VIA23SQ_C(rot) :        213
        Via        VIA12SQ_C :        252
        Via       VIA12BAR_C :         30


Redundant via conversion report:
--------------------------------

  Total optimized via conversion rate =  0.00% (0 / 506 vias)

    Layer VIA1        =  0.00% (0       / 282     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (282     vias)
    Layer VIA2        =  0.00% (0       / 213     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (213     vias)
```

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```
        Un-mapped    = 100.00% (282     vias)
    Layer VIA2        =  0.00% (0       / 213     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (213     vias)
    Layer VIA3        =  0.00% (0       / 7       vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (7       vias)
    Layer VIA4        =  0.00% (0       / 4       vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (4       vias)


Total number of nets = 123
0 open nets, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = antenna checking not active
Information: Routes in non-preferred voltage areas = 0 (ZRT-559)

Topology ECO not run, no qualifying violations or in frozen nets.
Updating the database ...
route_optl>
Information: Starting 'route_opt' (FLW-8000)
```

Route_opt command:

```
Terminal - ws2_26@ws2:~/SRM_Workshop/ICCII
File  Edit  View  Terminal  Tabs  Help

Route-opt timing update complete          CPU:   342 s (  0.09 hr )  ELAPSE:  6365 s (  1.77 hr )  MEM-PEAK:  1433 MB
INFO: Propagating Switching Activities
INFO: Switching Activity propagation took     0.00005 sec
INFO: Propagating Switching Activity for all power flows

Route-opt initial QoR
--------------------
Scenario Mapping Table
1: func::nom

Pathgroup Mapping Table
1: **default**
2: **async_default**
3: **clock_gating_default**
4: **in2reg_default**
5: **reg2out_default**
6: **in2out_default**
7: Clock

-------------------------------------------------------------------------------------------------------------------------------
-----
PATHGROUP QOR
-------------------------------------------------------------------------------------------------------------------------------
-----
Scene  PG      WNS        TNS    NSV      WHV        THV    NHV
    1   1   0.0000     0.0000      0   0.0000     0.0000      0
    1   2   0.0000     0.0000      0   0.0000     0.0000      0
    1   3   0.0000     0.0000      0   0.0000     0.0000      0
    1   4   0.0000     0.0000      0   0.0000     0.0000      0
    1   5   0.0000     0.0000      0   0.0000     0.0000      0
    1   6   0.0000     0.0000      0   0.0000     0.0000      0
    1   7   0.0000     0.0000      0   0.0000     0.0000      0
-------------------------------------------------------------------------------------------------------------------------------
--------------
```

```
    1   3   0.0000     0.0000      0   0.0000     0.0000      0
    1   4   0.0000     0.0000      0   0.0000     0.0000      0
    1   5   0.0000     0.0000      0   0.0000     0.0000      0
    1   6   0.0000     0.0000      0   0.0000     0.0000      0
    1   7   0.0000     0.0000      0   0.0000     0.0000      0
-------------------------------------------------------------------------------------------------------------------------------
--------------
SCENARIO QOR
-------------------------------------------------------------------------------------------------------------------------------
--------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   MaxTranC  MaxCapV    Leakage
    1   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0.0000        0  479266016
-------------------------------------------------------------------------------------------------------------------------------
--------------
DESIGN QOR
-------------------------------------------------------------------------------------------------------------------------------
--------------
Scene  PG      WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV   MaxTranC  MaxCapV    Leakage         Area    InstCnt
    *   *   0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0     0.0000        0  479266016       235.08        104
-------------------------------------------------------------------------------------------------------------------------------
--------------

Route-opt initial QoR Summary       WNS        TNS   R2RTNS    NSV      WHV        THV    NHV  MaxTrnV  MaxCapV    Leakage         Area    InstCnt
Route-opt initial QoR Summary    0.0000     0.0000   0.0000      0   0.0000     0.0000      0        0        0  479266016       235.08        104
Information: The netlist change observers are disabled for incremental extraction. (TIM-126)
INFO: using 1 threads
INFO: Cluster Analysis could not get worst dynamic scenario, ignored.
Route-opt initialization complete         CPU:   342 s (  0.10 hr )  ELAPSE:  6365 s (  1.77 hr )  MEM-PEAK:  1433 MB
Information: Initializing classic cellmap without advanced rules enabled and with PDC enabled
Information: The following app options are used in cellmap
```

```
Route-opt optimization summary          SETUP-COST    R2R-COST HOLD-COST LDRC-COST          AREA     LEAKAGE     INSTCNT            ELAPSE       MEM
INFO: place.legalize.enable_advanced_legalizer not set - need to revert CLO


Route-opt optimization summary          SETUP-COST    R2R-COST HOLD-COST LDRC-COST          AREA     LEAKAGE     INSTCNT            ELAPSE       MEM
Route-opt optimization Phase 2 Iter  1        0.00        0.00      0.00         -        235.08  479266016.00         104              1.77      1433

Route-opt optimization Phase 3 Iter  1        0.00        0.00      0.00         -        235.08  479266016.00         104              1.77      1433
INFO: New Levelizer turned on

INFO: New Levelizer turned on
Route-opt optimization Phase 4 Iter  1        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 4 Iter  2        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 4 Iter  3        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 4 Iter  4        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433


Route-opt optimization Phase 6 Iter  1        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  2        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  3        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  4        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  5        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  6        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  7        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  8        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  9        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter 10        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter 11        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter 12        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter 13        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433

Route-opt optimization Phase 7 Iter  1        0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
```

```
File  Edit  View  Terminal  Tabs  Help
Route-opt optimization Phase 6 Iter  1          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  2          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  3          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  4          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  5          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  6          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  7          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  8          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter  9          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter 10          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter 11          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter 12          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 6 Iter 13          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433

Route-opt optimization Phase 7 Iter  1          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 7 Iter  2          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433

Enable clock slack update
INFO: cellmap features:  adv-rules=(Y), pdc=(Y), clock-rules=(Y)
Route-opt optimization Phase 8 Iter  1          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
INFO: cellmap features:  adv-rules=(N), pdc=(Y), clock-rules=(Y)

Route-opt optimization Phase 9 Iter  1          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 9 Iter  2          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 9 Iter  3          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 9 Iter  4          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 9 Iter  5          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 9 Iter  6          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization Phase 9 Iter  7          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433
Route-opt optimization summary            SETUP-COST    R2R-COST HOLD-COST LDRC-COST          AREA     LEAKAGE     INSTCNT            ELAPSE       MEM
Route-opt optimization Phase 9 Iter  8          0.00        0.00      0.00         7        235.08  479266016.00         104              1.77      1433

Enable clock slack update
INFO: cellmap features:  adv-rules=(Y), pdc=(Y), clock-rules=(Y)
```

```
      Un-mapped     = 100.00% (213      vias)
  Layer VIA3        =  0.00% (0       / 7       vias)
      Un-optimized =  0.00% (0        vias)
      Un-mapped     = 100.00% (7        vias)
  Layer VIA4        =  0.00% (0       / 4       vias)
      Un-optimized =  0.00% (0        vias)
      Un-mapped     = 100.00% (4        vias)

Total double via conversion rate     =  0.00% (0 / 506 vias)

  Layer VIA1        =  0.00% (0       / 282     vias)
  Layer VIA2        =  0.00% (0       / 213     vias)
  Layer VIA3        =  0.00% (0       / 7       vias)
  Layer VIA4        =  0.00% (0       / 4       vias)

The optimized via conversion rate based on total routed via count =  0.00% (0 / 506 vias)

  Layer VIA1        =  0.00% (0       / 282     vias)
      Un-optimized =  0.00% (0        vias)
      Un-mapped     = 100.00% (282      vias)
  Layer VIA2        =  0.00% (0       / 213     vias)
      Un-optimized =  0.00% (0        vias)
      Un-mapped     = 100.00% (213      vias)
  Layer VIA3        =  0.00% (0       / 7       vias)
      Un-optimized =  0.00% (0        vias)
      Un-mapped     = 100.00% (7        vias)
  Layer VIA4        =  0.00% (0       / 4       vias)
      Un-optimized =  0.00% (0        vias)
      Un-mapped     = 100.00% (4        vias)
```

```
  Total optimized via conversion rate =  0.00% (0 / 506 vias)

    Layer VIA1        =  0.00% (0      / 282     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (282     vias)
    Layer VIA2        =  0.00% (0      / 213     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (213     vias)
    Layer VIA3        =  0.00% (0      / 7       vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (7       vias)
    Layer VIA4        =  0.00% (0      / 4       vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (4       vias)

  Total double via conversion rate    =  0.00% (0 / 506 vias)

    Layer VIA1        =  0.00% (0      / 282     vias)
    Layer VIA2        =  0.00% (0      / 213     vias)
    Layer VIA3        =  0.00% (0      / 7       vias)
    Layer VIA4        =  0.00% (0      / 4       vias)

  The optimized via conversion rate based on total routed via count =  0.00% (0 / 506 vias)

    Layer VIA1        =  0.00% (0      / 282     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (282     vias)
    Layer VIA2        =  0.00% (0      / 213     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (213     vias)
    Layer VIA3        =  0.00% (0      / 7       vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (7       vias)
```

```
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        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (4       vias)


Total number of nets = 123
0 open nets, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                 0 ports without pins of 0 cells connected to 0 nets
                                 0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = antenna checking not active
Information: Routes in non-preferred voltage areas = 0 (ZRT-559)

Total Wire Length =                    538 micron
Total Number of Contacts =             506
Total Number of Wires =                510
Total Number of PtConns =              65
Total Number of Routed Wires =       502
Total Routed Wire Length =           531 micron
Total Number of Routed Contacts =       506
        Layer             M1 :         41 micron
        Layer             M2 :        225 micron
        Layer             M3 :        252 micron
        Layer             M4 :         10 micron
        Layer             M5 :          2 micron
        Layer             M6 :          0 micron
        Layer             M7 :          0 micron
        Layer             M8 :          0 micron
        Layer             M9 :          0 micron
        Layer           MRDL :          0 micron
        Via   VIA45SQ_C(rot) :          4
        Via        VIA34SQ_C :          7
        Via   VIA23SQ_C(rot) :        213
        Via        VIA12SQ_C :        252
```

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```
    Layer VIA4       =  0.00% (0      / 4       vias)

  The optimized via conversion rate based on total routed via count =  0.00% (0 / 506 vias)

    Layer VIA1       =  0.00% (0      / 282     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (282     vias)
    Layer VIA2       =  0.00% (0      / 213     vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (213     vias)
    Layer VIA3       =  0.00% (0      / 7       vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (7       vias)
    Layer VIA4       =  0.00% (0      / 4       vias)
        Un-optimized =  0.00% (0       vias)
        Un-mapped    = 100.00% (4       vias)
```

```
Information: Time: 2024-07-11 15:19:24 / Session:  01:46:05 / Command:  00:00:01 / CPU:  00:00:01 / Memory: 1434 MB (FLW-8100)
1
icc2_shell> write_verilog ./results/sub8bit.routed.v
1
icc2_shell> write_sdc -output ./results/sub8bit.routed.sdc
Information: The command 'write_sdc' cleared the undo history. (UNDO-016)

Warning: Multiply cell derates are skipped!

Warning: Multiply net derates are skipped!
1
icc2_shell> write_parasitics -format spef -output ./results/sub8bit.spef
Information: Design sub8bit has 123 nets, 0 global routed, 121 detail routed. (NEX-024)
NEX: extract design sub8bit
Information: batch extract takes 0.00 seconds, elapse 0.00 seconds (NEX-015)
Information: The stitching and editing of coupling caps is turned OFF for design 'SUB8BIT_LIB:sub8bit.design'. (TIM-125)
NEX: write corner ID 0 parasitics to ./results/sub8bit.spef.p1_125.spef
spefName ./results/sub8bit.spef.p1_125.spef, corner name nom
NEX: write corner ID 1 parasitics to ./results/sub8bit.spef.p2_125.spef
spefName ./results/sub8bit.spef.p2_125.spef, corner name nom
NEX:Warning write_parasitics supports only Ohm and kOhm as user resistance unit not 1MOhm, we force to set it Ohm.NEX: write_parasitics command finished
icc2_shell> save_block
Information: Saving block 'SUB8BIT_LIB:sub8bit.design'
1
icc2_shell> save_lib
Saving library 'SUB8BIT_LIB'
1
icc2_shell>
```

Sub8bit.routed.sdc file:

```
##############################################################################
#
# Design name:  sub8bit
#
# Created by icc2 write_sdc on Thu Jul 11 15:28:23 2024
#
##############################################################################

set sdc_version 2.1
set_units -time ns -resistance MOhm -capacitance fF -voltage V -current uA

##############################################################################
#
# Units
# time_unit                : 1e-09
# resistance_unit          : 1000000
# capacitive_load_unit     : 1e-15
# voltage_unit             : 1
# current_unit             : 1e-06
# power_unit               : 1e-12
##############################################################################


# Mode: func
# Corner: nom
# Scenario: func::nom

# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 1
create_clock -name Clock -period 1 -waveform {0 0.5} [get_ports {Clock}]
set_propagated_clock [get_clocks {Clock}]
# Warning: Libcell power domain derates are skipped!

# Set latency for io paths.
```

```
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {Clock}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {A[7]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {A[6]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {A[5]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {A[4]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {A[3]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {A[2]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {A[1]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {A[0]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[7]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[6]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[5]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[4]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[3]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[2]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[1]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
```

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```
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[5]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[4]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[3]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[2]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[1]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {B[0]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 3
set_input_delay -clock [get_clocks {Clock}] -max 0.6 [get_ports {Clock}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 6
set_output_delay -clock [get_clocks {Clock}] -max 0.4 [get_ports {diff[7]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 6
set_output_delay -clock [get_clocks {Clock}] -max 0.4 [get_ports {diff[6]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 6
set_output_delay -clock [get_clocks {Clock}] -max 0.4 [get_ports {diff[5]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 6
set_output_delay -clock [get_clocks {Clock}] -max 0.4 [get_ports {diff[4]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 6
set_output_delay -clock [get_clocks {Clock}] -max 0.4 [get_ports {diff[3]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 6
set_output_delay -clock [get_clocks {Clock}] -max 0.4 [get_ports {diff[2]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 6
set_output_delay -clock [get_clocks {Clock}] -max 0.4 [get_ports {diff[1]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 6
set_output_delay -clock [get_clocks {Clock}] -max 0.4 [get_ports {diff[0]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 6
set_output_delay -clock [get_clocks {Clock}] -max 0.4 [get_ports {borrow}]
set_max_transition 0.25 [current_design]
set_max_transition 0.1 [get_clocks {Clock}] -clock_path
```

```
create_clock -name Clock -period 1 -waveform {0 0.5} [get_ports {Clock}]
set_propagated_clock [get_clocks {Clock}]
# Warning: Libcell power domain derates are skipped!

# Set latency for io paths.
# -origin useful_skew
set_clock_latency -min 0.0353813 [get_clocks {Clock}]
# -origin useful_skew
set_clock_latency -max 0.0365067 [get_clocks {Clock}]
# Set propagated on clock sources to avoid removing latency for IO paths.
set_propagated_clock  [get_ports {Clock}]
set_clock_uncertainty -1 [get_clocks {Clock}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {A[7]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {A[6]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {A[5]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {A[4]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {A[3]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {A[2]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {A[1]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {A[0]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {B[7]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
set_input_transition 0.15 [get_ports {B[6]}]
# /ve/ws_home/ws2_26/SRM_Workshop/CONSTRAINTS/sub8bit.sdc, line 4
```

Sub8bit.route.v file:

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```
// IC Compiler II Version V-2023.12 Verilog Writer
// Generated on 7/11/2024 at 15:27:41
// Library Name: SUB8BIT_LIB
// Block Name: sub8bit
// User Label:
// Write Command: write_verilog ./results/sub8bit.routed.v
module sub8bit ( A , B , Clock , diff , borrow ) ;
input  [7:0] A ;
input  [7:0] B ;
input  Clock ;
output [7:0] diff ;
output borrow ;

DFFX1_RVT borrow_reg ( .D ( N25 ) , .CLK ( ctosc_drc_0 ) , .Q ( borrow ) ) ;
DFFX1_RVT \diff_reg[7] ( .D ( N24 ) , .CLK ( ctosc_drc_0 ) , .Q ( diff[7] ) ) ;
DFFX1_RVT \diff_reg[6] ( .D ( N23 ) , .CLK ( ctosc_drc_0 ) , .Q ( diff[6] ) ) ;
DFFX1_RVT \diff_reg[5] ( .D ( N22 ) , .CLK ( ctosc_drc_0 ) , .Q ( diff[5] ) ) ;
DFFX1_RVT \diff_reg[4] ( .D ( N21 ) , .CLK ( ctosc_drc_0 ) , .Q ( diff[4] ) ) ;
DFFX1_RVT \diff_reg[3] ( .D ( N20 ) , .CLK ( ctosc_drc_0 ) , .Q ( diff[3] ) ) ;
DFFX1_RVT \diff_reg[2] ( .D ( N19 ) , .CLK ( ctosc_drc_0 ) , .Q ( diff[2] ) ) ;
DFFX1_RVT \diff_reg[1] ( .D ( N18 ) , .CLK ( ctosc_drc_0 ) , .Q ( diff[1] ) ) ;
DFFSSRX1_RVT \diff_reg[0] ( .D ( N7 ) , .SETB ( A[0] ) , .RSTB ( n90 ) ,
    .CLK ( ctosc_drc_0 ) , .Q ( diff[0] ) ) ;
OR2X1_RVT U11 ( .A1 ( n49 ) , .A2 ( n87 ) , .Y ( N25 ) ) ;
OR2X1_RVT U12 ( .A1 ( n86 ) , .A2 ( n85 ) , .Y ( n89 ) ) ;
AND2X1_RVT U13 ( .A1 ( n62 ) , .A2 ( n61 ) , .Y ( n64 ) ) ;
OR2X1_RVT U14 ( .A1 ( n51 ) , .A2 ( n50 ) , .Y ( n53 ) ) ;
OR2X1_RVT U15 ( .A1 ( n75 ) , .A2 ( n74 ) , .Y ( n77 ) ) ;
OR2X1_RVT U16 ( .A1 ( n67 ) , .A2 ( n68 ) , .Y ( n69 ) ) ;
OR2X1_RVT U17 ( .A1 ( n54 ) , .A2 ( n55 ) , .Y ( n56 ) ) ;
OR2X1_RVT U18 ( .A1 ( n79 ) , .A2 ( n78 ) , .Y ( n80 ) ) ;
INVX0_RVT U19 ( .A ( A[1] ) , .Y ( n11 ) ) ;
INVX0_RVT U20 ( .A ( n87 ) , .Y ( n88 ) ) ;
"sub8bit.routed.v" 125L, 6476C
```

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```
DFFX1_RVT \diff_reg[1] ( .D ( N18 ) , .CLK ( ctosc_drc_0 ) , .Q ( diff[1] ) ) ;
DFFSSRX1_RVT \diff_reg[0] ( .D ( N7 ) , .SETB ( A[0] ) , .RSTB ( n90 ) ,
    .CLK ( ctosc_drc_0 ) , .Q ( diff[0] ) ) ;
OR2X1_RVT U11 ( .A1 ( n49 ) , .A2 ( n87 ) , .Y ( N25 ) ) ;
OR2X1_RVT U12 ( .A1 ( n86 ) , .A2 ( n85 ) , .Y ( n89 ) ) ;
AND2X1_RVT U13 ( .A1 ( n62 ) , .A2 ( n61 ) , .Y ( n64 ) ) ;
OR2X1_RVT U14 ( .A1 ( n51 ) , .A2 ( n50 ) , .Y ( n53 ) ) ;
OR2X1_RVT U15 ( .A1 ( n75 ) , .A2 ( n74 ) , .Y ( n77 ) ) ;
OR2X1_RVT U16 ( .A1 ( n67 ) , .A2 ( n68 ) , .Y ( n69 ) ) ;
OR2X1_RVT U17 ( .A1 ( n54 ) , .A2 ( n55 ) , .Y ( n56 ) ) ;
OR2X1_RVT U18 ( .A1 ( n79 ) , .A2 ( n78 ) , .Y ( n80 ) ) ;
INVX0_RVT U19 ( .A ( A[1] ) , .Y ( n11 ) ) ;
INVX0_RVT U20 ( .A ( n87 ) , .Y ( n88 ) ) ;
INVX0_RVT U21 ( .A ( n82 ) , .Y ( n83 ) ) ;
INVX0_RVT U22 ( .A ( n78 ) , .Y ( n76 ) ) ;
INVX0_RVT U23 ( .A ( n71 ) , .Y ( n72 ) ) ;
INVX0_RVT U24 ( .A ( n68 ) , .Y ( n65 ) ) ;
INVX0_RVT U25 ( .A ( n58 ) , .Y ( n59 ) ) ;
INVX0_RVT U26 ( .A ( n55 ) , .Y ( n52 ) ) ;
OR3X1_RVT ctmTdsLR_1_2 ( .A1 ( n54 ) , .A2 ( n26 ) , .A3 ( n55 ) ,
    .Y ( n62 ) ) ;
INVX0_RVT U28 ( .A ( n18 ) , .Y ( n19 ) ) ;
INVX0_RVT U29 ( .A ( n23 ) , .Y ( n24 ) ) ;
INVX0_RVT U30 ( .A ( n4 ) , .Y ( n5 ) ) ;
INVX0_RVT U31 ( .A ( n32 ) , .Y ( n33 ) ) ;
INVX0_RVT U32 ( .A ( n13 ) , .Y ( n14 ) ) ;
INVX0_RVT U33 ( .A ( n8 ) , .Y ( n9 ) ) ;
INVX0_RVT U34 ( .A ( n42 ) , .Y ( n43 ) ) ;
INVX0_RVT U35 ( .A ( B[0] ) , .Y ( N7 ) ) ;
INVX0_RVT U36 ( .A ( A[3] ) , .Y ( n17 ) ) ;
AND3X1_RVT ctmTdsLR_1_3 ( .A1 ( n62 ) , .A2 ( n61 ) , .A3 ( n63 ) ,
    .Y ( n68 ) ) ;
INVX0_RVT U38 ( .A ( A[2] ) , .Y ( n22 ) ) ;
```

```
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INVX0_RVT U38 ( .A ( A[2] ) , .Y ( n22 ) ) ;
INVX0_RVT U39 ( .A ( A[5] ) , .Y ( n7 ) ) ;
INVX0_RVT U40 ( .A ( A[4] ) , .Y ( n31 ) ) ;
INVX0_RVT U41 ( .A ( B[3] ) , .Y ( n28 ) ) ;
INVX0_RVT U42 ( .A ( A[6] ) , .Y ( n41 ) ) ;
INVX0_RVT U43 ( .A ( A[7] ) , .Y ( n3 ) ) ;
OR3X1_RVT ctmTdsLR_1_4 ( .A1 ( n35 ) , .A2 ( n67 ) , .A3 ( n68 ) ,
    .Y ( n37 ) ) ;
INVX0_RVT U45 ( .A ( B[7] ) , .Y ( n48 ) ) ;
AND2X1_RVT U46 ( .A1 ( n48 ) , .A2 ( n3 ) , .Y ( n6 ) ) ;
OR2X1_RVT U47 ( .A1 ( n3 ) , .A2 ( n48 ) , .Y ( n4 ) ) ;
OR2X1_RVT U48 ( .A1 ( n6 ) , .A2 ( n5 ) , .Y ( n85 ) ) ;
INVX0_RVT U49 ( .A ( B[5] ) , .Y ( n38 ) ) ;
AND2X1_RVT U50 ( .A1 ( n38 ) , .A2 ( n7 ) , .Y ( n10 ) ) ;
OR2X1_RVT U51 ( .A1 ( n7 ) , .A2 ( n38 ) , .Y ( n8 ) ) ;
OR2X1_RVT U52 ( .A1 ( n10 ) , .A2 ( n9 ) , .Y ( n74 ) ) ;
INVX0_RVT U53 ( .A ( B[1] ) , .Y ( n12 ) ) ;
AND2X1_RVT U54 ( .A1 ( n12 ) , .A2 ( n11 ) , .Y ( n15 ) ) ;
OR2X1_RVT U55 ( .A1 ( n12 ) , .A2 ( n11 ) , .Y ( n13 ) ) ;
OR2X1_RVT U56 ( .A1 ( n15 ) , .A2 ( n14 ) , .Y ( n50 ) ) ;
OR2X1_RVT U57 ( .A1 ( A[0] ) , .A2 ( N7 ) , .Y ( n51 ) ) ;
AND2X1_RVT U58 ( .A1 ( n50 ) , .A2 ( n51 ) , .Y ( n55 ) ) ;
AND2X1_RVT U59 ( .A1 ( n12 ) , .A2 ( A[1] ) , .Y ( n54 ) ) ;
INVX0_RVT U60 ( .A ( B[2] ) , .Y ( n21 ) ) ;
AND2X1_RVT U61 ( .A1 ( n21 ) , .A2 ( A[2] ) , .Y ( n26 ) ) ;
OR3X1_RVT ctmTdsLR_1_5 ( .A1 ( n45 ) , .A2 ( n79 ) , .A3 ( n78 ) ,
    .Y ( n47 ) ) ;
DELLN1X2_RVT ctosc_drc_inst_169 ( .A ( Clock ) , .Y ( ctosc_drc_0 ) ) ;
AND2X1_RVT U64 ( .A1 ( n28 ) , .A2 ( n17 ) , .Y ( n20 ) ) ;
OR2X1_RVT U65 ( .A1 ( n17 ) , .A2 ( n28 ) , .Y ( n18 ) ) ;
OR2X1_RVT U66 ( .A1 ( n20 ) , .A2 ( n19 ) , .Y ( n63 ) ) ;
AND2X1_RVT U67 ( .A1 ( n21 ) , .A2 ( n22 ) , .Y ( n25 ) ) ;
OR2X1_RVT U68 ( .A1 ( n22 ) , .A2 ( n21 ) , .Y ( n23 ) ) ;
```

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OR2X1_RVT U68 ( .A1 ( n22 ) , .A2 ( n21 ) , .Y ( n23 ) ) ;
OR2X1_RVT U69 ( .A1 ( n25 ) , .A2 ( n24 ) , .Y ( n57 ) ) ;
OR2X1_RVT U70 ( .A1 ( n26 ) , .A2 ( n57 ) , .Y ( n61 ) ) ;
AND2X1_RVT U73 ( .A1 ( n28 ) , .A2 ( A[3] ) , .Y ( n67 ) ) ;
INVX0_RVT U74 ( .A ( B[4] ) , .Y ( n30 ) ) ;
AND2X1_RVT U75 ( .A1 ( n30 ) , .A2 ( A[4] ) , .Y ( n35 ) ) ;
AND2X1_RVT U78 ( .A1 ( n30 ) , .A2 ( n31 ) , .Y ( n34 ) ) ;
OR2X1_RVT U79 ( .A1 ( n31 ) , .A2 ( n30 ) , .Y ( n32 ) ) ;
OR2X1_RVT U80 ( .A1 ( n34 ) , .A2 ( n33 ) , .Y ( n70 ) ) ;
OR2X1_RVT U81 ( .A1 ( n35 ) , .A2 ( n70 ) , .Y ( n36 ) ) ;
AND2X1_RVT U82 ( .A1 ( n37 ) , .A2 ( n36 ) , .Y ( n75 ) ) ;
AND2X1_RVT U83 ( .A1 ( n74 ) , .A2 ( n75 ) , .Y ( n78 ) ) ;
AND2X1_RVT U84 ( .A1 ( n38 ) , .A2 ( A[5] ) , .Y ( n79 ) ) ;
INVX0_RVT U85 ( .A ( B[6] ) , .Y ( n40 ) ) ;
AND2X1_RVT U86 ( .A1 ( n40 ) , .A2 ( A[6] ) , .Y ( n45 ) ) ;
AND2X1_RVT U89 ( .A1 ( n40 ) , .A2 ( n41 ) , .Y ( n44 ) ) ;
OR2X1_RVT U90 ( .A1 ( n41 ) , .A2 ( n40 ) , .Y ( n42 ) ) ;
OR2X1_RVT U91 ( .A1 ( n44 ) , .A2 ( n43 ) , .Y ( n81 ) ) ;
OR2X1_RVT U92 ( .A1 ( n45 ) , .A2 ( n81 ) , .Y ( n46 ) ) ;
AND2X1_RVT U93 ( .A1 ( n47 ) , .A2 ( n46 ) , .Y ( n86 ) ) ;
AND2X1_RVT U94 ( .A1 ( n85 ) , .A2 ( n86 ) , .Y ( n87 ) ) ;
AND2X1_RVT U95 ( .A1 ( n48 ) , .A2 ( A[7] ) , .Y ( n49 ) ) ;
AND2X1_RVT U96 ( .A1 ( n53 ) , .A2 ( n52 ) , .Y ( N18 ) ) ;
OR2X1_RVT U97 ( .A1 ( n56 ) , .A2 ( n57 ) , .Y ( n60 ) ) ;
AND2X1_RVT U98 ( .A1 ( n57 ) , .A2 ( n56 ) , .Y ( n58 ) ) ;
AND2X1_RVT U99 ( .A1 ( n60 ) , .A2 ( n59 ) , .Y ( N19 ) ) ;
OR2X1_RVT U100 ( .A1 ( n64 ) , .A2 ( n63 ) , .Y ( n66 ) ) ;
AND2X1_RVT U101 ( .A1 ( n66 ) , .A2 ( n65 ) , .Y ( N20 ) ) ;
OR2X1_RVT U102 ( .A1 ( n69 ) , .A2 ( n70 ) , .Y ( n73 ) ) ;
AND2X1_RVT U103 ( .A1 ( n70 ) , .A2 ( n69 ) , .Y ( n71 ) ) ;
AND2X1_RVT U104 ( .A1 ( n73 ) , .A2 ( n72 ) , .Y ( N21 ) ) ;
AND2X1_RVT U105 ( .A1 ( n77 ) , .A2 ( n76 ) , .Y ( N22 ) ) ;
OR2X1_RVT U106 ( .A1 ( n80 ) , .A2 ( n81 ) , .Y ( n84 ) ) ;
```

```
File  Edit  View  Terminal  Tabs  Help
OR2X1_RVT U80 ( .A1 ( n34 ) , .A2 ( n33 ) , .Y ( n70 ) ) ;
OR2X1_RVT U81 ( .A1 ( n35 ) , .A2 ( n70 ) , .Y ( n36 ) ) ;
AND2X1_RVT U82 ( .A1 ( n37 ) , .A2 ( n36 ) , .Y ( n75 ) ) ;
AND2X1_RVT U83 ( .A1 ( n74 ) , .A2 ( n75 ) , .Y ( n78 ) ) ;
AND2X1_RVT U84 ( .A1 ( n38 ) , .A2 ( A[5] ) , .Y ( n79 ) ) ;
INVX0_RVT U85 ( .A ( B[6] ) , .Y ( n40 ) ) ;
AND2X1_RVT U86 ( .A1 ( n40 ) , .A2 ( A[6] ) , .Y ( n45 ) ) ;
AND2X1_RVT U89 ( .A1 ( n40 ) , .A2 ( n41 ) , .Y ( n44 ) ) ;
OR2X1_RVT U90 ( .A1 ( n41 ) , .A2 ( n40 ) , .Y ( n42 ) ) ;
OR2X1_RVT U91 ( .A1 ( n44 ) , .A2 ( n43 ) , .Y ( n81 ) ) ;
OR2X1_RVT U92 ( .A1 ( n45 ) , .A2 ( n81 ) , .Y ( n46 ) ) ;
AND2X1_RVT U93 ( .A1 ( n47 ) , .A2 ( n46 ) , .Y ( n86 ) ) ;
AND2X1_RVT U94 ( .A1 ( n85 ) , .A2 ( n86 ) , .Y ( n87 ) ) ;
AND2X1_RVT U95 ( .A1 ( n48 ) , .A2 ( A[7] ) , .Y ( n49 ) ) ;
AND2X1_RVT U96 ( .A1 ( n53 ) , .A2 ( n52 ) , .Y ( N18 ) ) ;
OR2X1_RVT U97 ( .A1 ( n56 ) , .A2 ( n57 ) , .Y ( n60 ) ) ;
AND2X1_RVT U98 ( .A1 ( n57 ) , .A2 ( n56 ) , .Y ( n58 ) ) ;
AND2X1_RVT U99 ( .A1 ( n60 ) , .A2 ( n59 ) , .Y ( N19 ) ) ;
OR2X1_RVT U100 ( .A1 ( n64 ) , .A2 ( n63 ) , .Y ( n66 ) ) ;
AND2X1_RVT U101 ( .A1 ( n66 ) , .A2 ( n65 ) , .Y ( N20 ) ) ;
OR2X1_RVT U102 ( .A1 ( n69 ) , .A2 ( n70 ) , .Y ( n73 ) ) ;
AND2X1_RVT U103 ( .A1 ( n70 ) , .A2 ( n69 ) , .Y ( n71 ) ) ;
AND2X1_RVT U104 ( .A1 ( n73 ) , .A2 ( n72 ) , .Y ( N21 ) ) ;
AND2X1_RVT U105 ( .A1 ( n77 ) , .A2 ( n76 ) , .Y ( N22 ) ) ;
OR2X1_RVT U106 ( .A1 ( n80 ) , .A2 ( n81 ) , .Y ( n84 ) ) ;
AND2X1_RVT U107 ( .A1 ( n81 ) , .A2 ( n80 ) , .Y ( n82 ) ) ;
AND2X1_RVT U108 ( .A1 ( n84 ) , .A2 ( n83 ) , .Y ( N23 ) ) ;
AND2X1_RVT U109 ( .A1 ( n89 ) , .A2 ( n88 ) , .Y ( N24 ) ) ;
INVX0_RVT ctmTdsLR_1_0 ( .A ( N7 ) , .Y ( tmp_net0 ) ) ;
OR2X1_RVT ctmTdsLR_2_1 ( .A1 ( A[0] ) , .A2 ( tmp_net0 ) , .Y ( n90 ) ) ;
endmodule
```

Sub8bit.spef p1 file:

Terminal - ws2_26@ws2:~/SRM_Workshop/ICCII/results

File Edit View Terminal Tabs Help

```
*SPEF "1481-1998"
*DESIGN "sub8bit"
*DATE "Thu Jul 11 15:29:21 2024"
*VENDOR "Synopsys, Inc."
*PROGRAM "icc2 /usr/synopsys/icc2/V-2023.12/linux64/nwtn/bin/icc2_exec"
*VERSION "V-2023.12 Nov 23, 2023"
*DESIGN_FLOW "ICC2 SPEF DR"
*DIVIDER /
*DELIMITER :
*BUS_DELIMITER [ ]
*T_UNIT 1 NS
*C_UNIT 1 FF
*R_UNIT 1 OHM
*L_UNIT 1 HENRY

// XY_UNIT 1 UM
// PARASITIC_TECH p1 at 125.000 degree

*NAME_MAP
*1 A[7]
*2 A[6]
*3 A[5]
*4 A[4]
*5 A[3]
*6 A[2]
*7 A[1]
*8 A[0]
*9 B[7]
*10 B[6]
*11 B[5]
*12 B[4]
*13 B[3]
*14 B[2]
```

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File Edit View Terminal Tabs Help

```
*14 B[2]
*15 B[1]
*16 B[0]
*17 Clock
*18 diff[7]
*19 diff[6]
*20 diff[5]
*21 diff[4]
*22 diff[3]
*23 diff[2]
*24 diff[1]
*25 diff[0]
*26 borrow
*27 VDD
*28 VSS
*29 borrow_reg
*30 diff_reg[7]
*31 diff_reg[6]
*32 diff_reg[5]
*33 diff_reg[4]
*34 diff_reg[3]
*35 diff_reg[2]
*36 diff_reg[1]
*37 diff_reg[0]
*38 U11
*39 U12
*40 U13
*41 U14
*42 U15
*43 U16
*44 U17
*45 U18
*46 U19
```

```
File  Edit  View  Terminal  Tabs  Help
1 *1:4 *1:3 1.0375
2 *1:5 *1:4 0.5
3 *1:3 *70:A 1
4 *1:7 *1:6 2.123214
5 *1:8 *1:7 0.5
6 *1:8 *1:5 1.604464
7 *1:6 *116:A2 1
8 *1:11 *1:10 9.747323
9 *1:12 *1:11 0.5
10 *1:13 *1:12 4.837501
11 *1:14 *1:13 0.5
12 *1:10 *1:9 0.5428572
13 *1:9 *1:8 0.8142857

*END

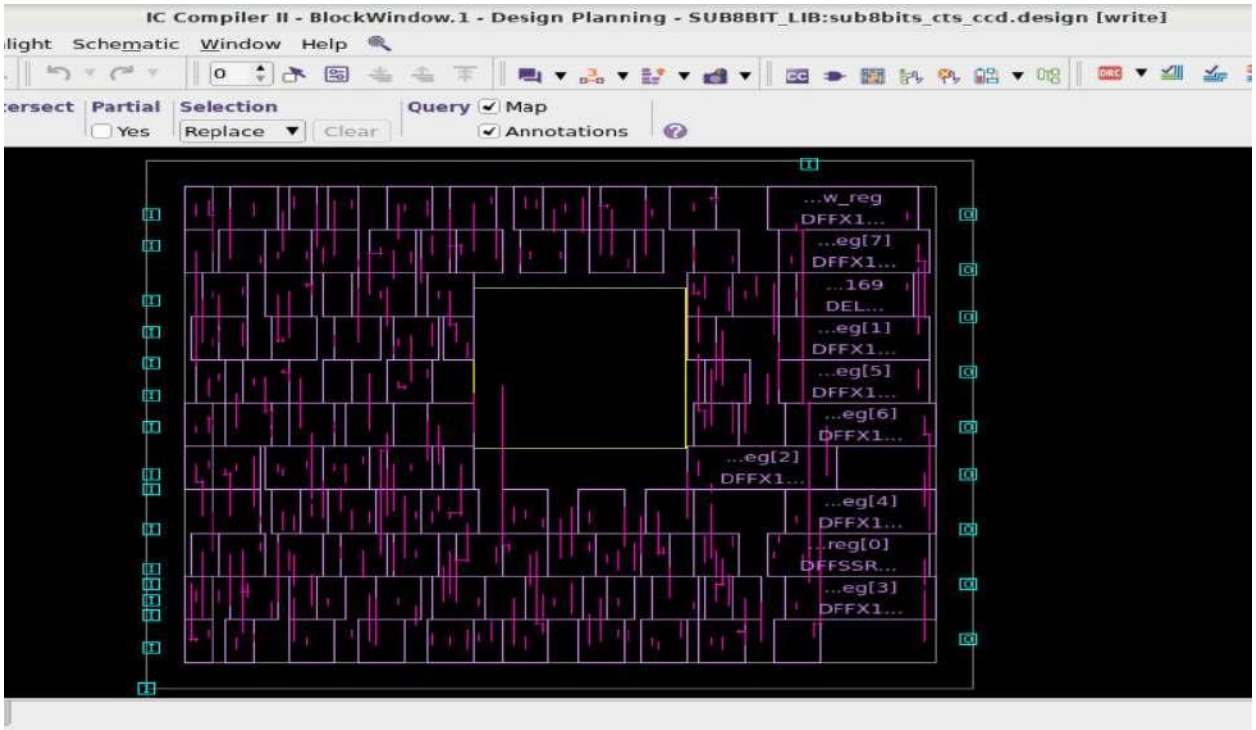
*D_NET *2 0.6612278 //LENGTH 7.947 LUMPCC 0 DR

*CONN
*P *2 I *L 0 *C 0.258 12.552
*I *69:A I *L 0.604022 *C 1.304 16.808
*I *109:A2 I *L 0.557409 *C 3.432 16.808
*N *2:3 *C 3.432 16.626
*N *2:4 *C 3.432 16.796
*N *2:5 *C 3.419 16.808
*N *2:6 *C 1.318 16.808
*N *2:7 *C 1.304 16.794
*N *2:8 *C 1.304 12.566
*N *2:9 *C 1.290 12.552

*CAP
0 *2 0.03661247
1 *69:A 0.001
```

Now, we will observe the different outputs in the gui by changing different parameters, mainly metal layers.

1.With all the parameters



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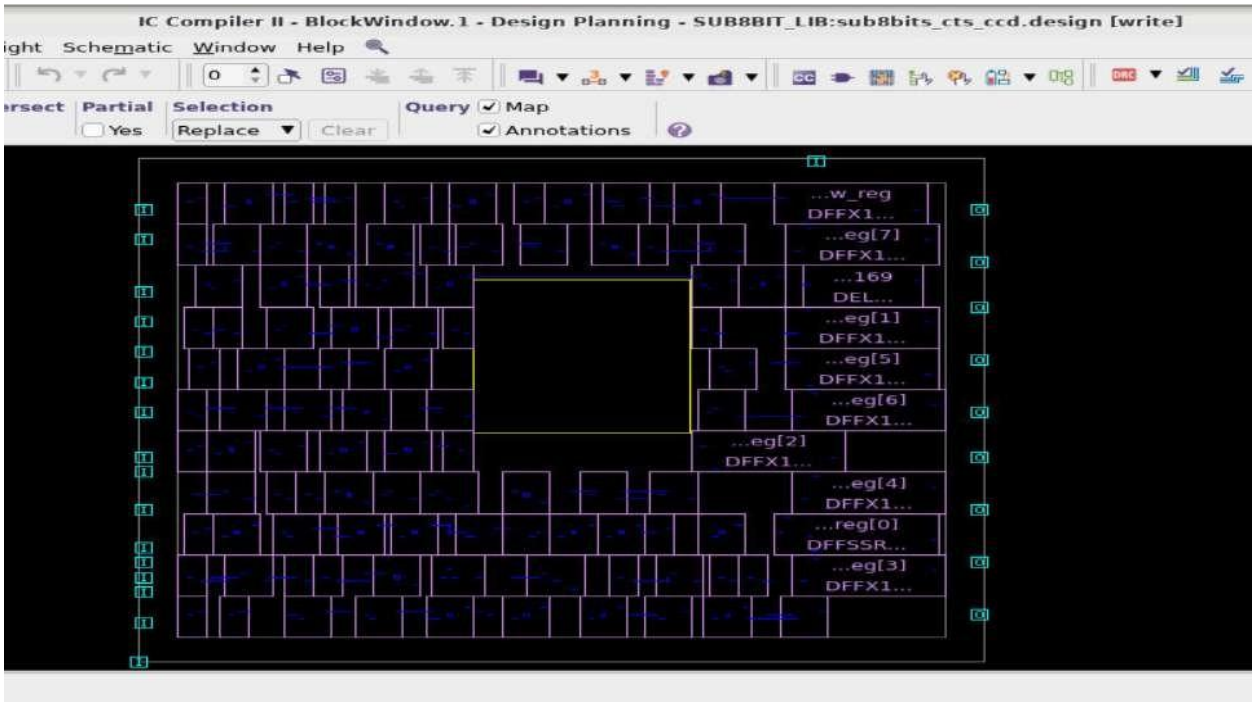
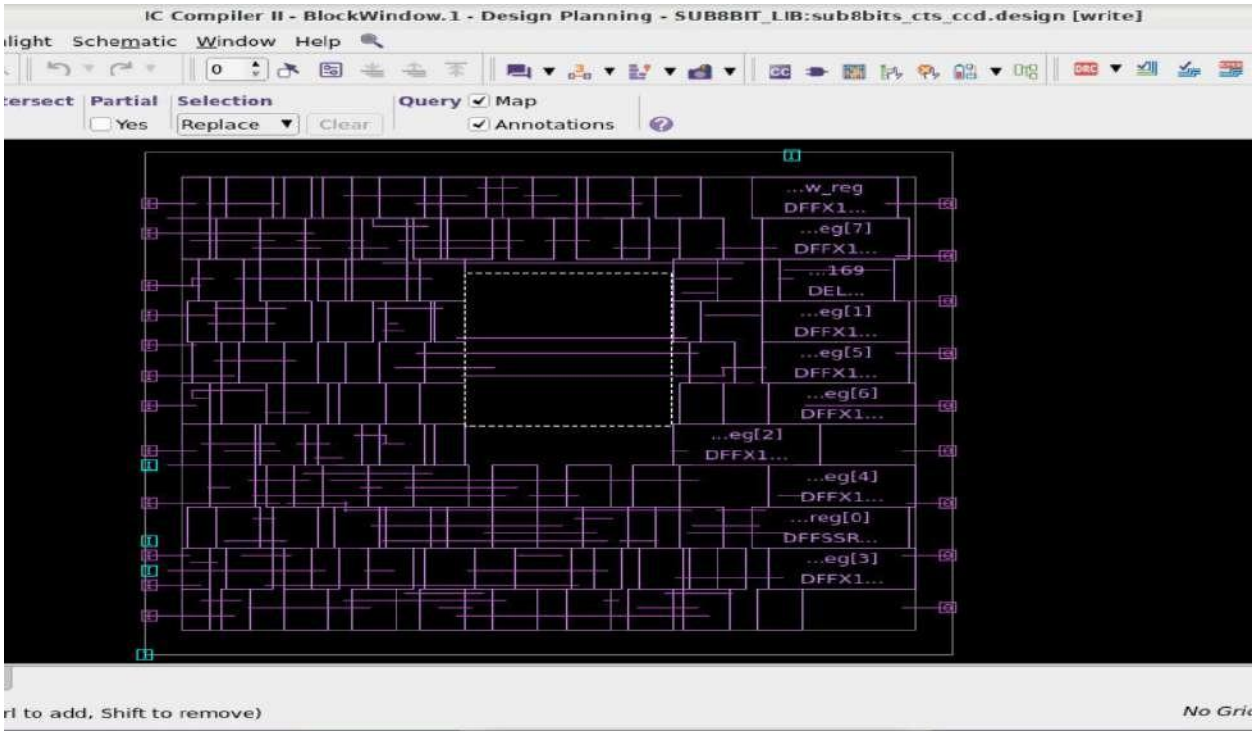
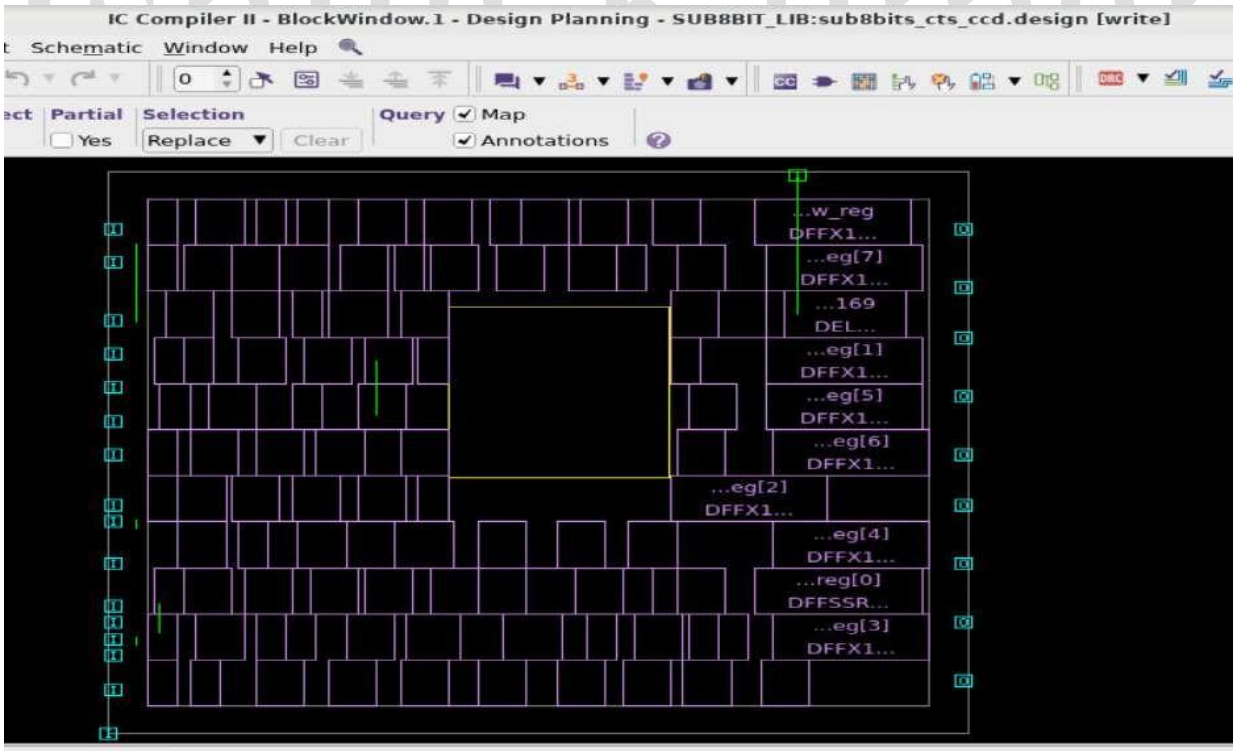
2. M1



3. M2



4. M3



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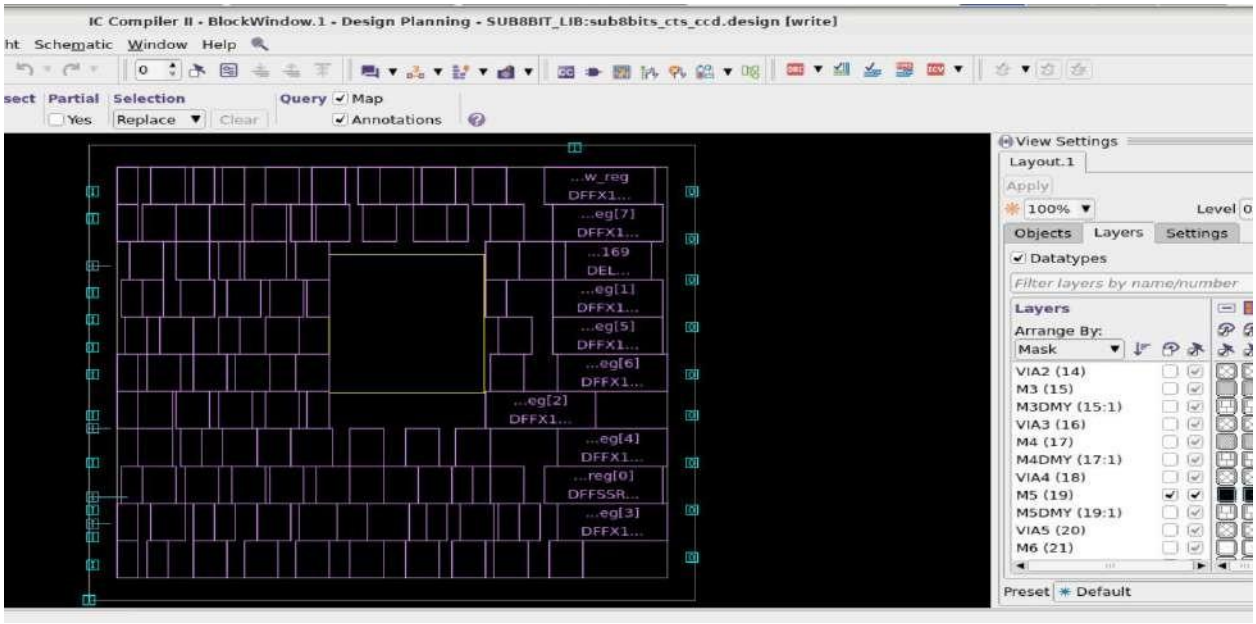
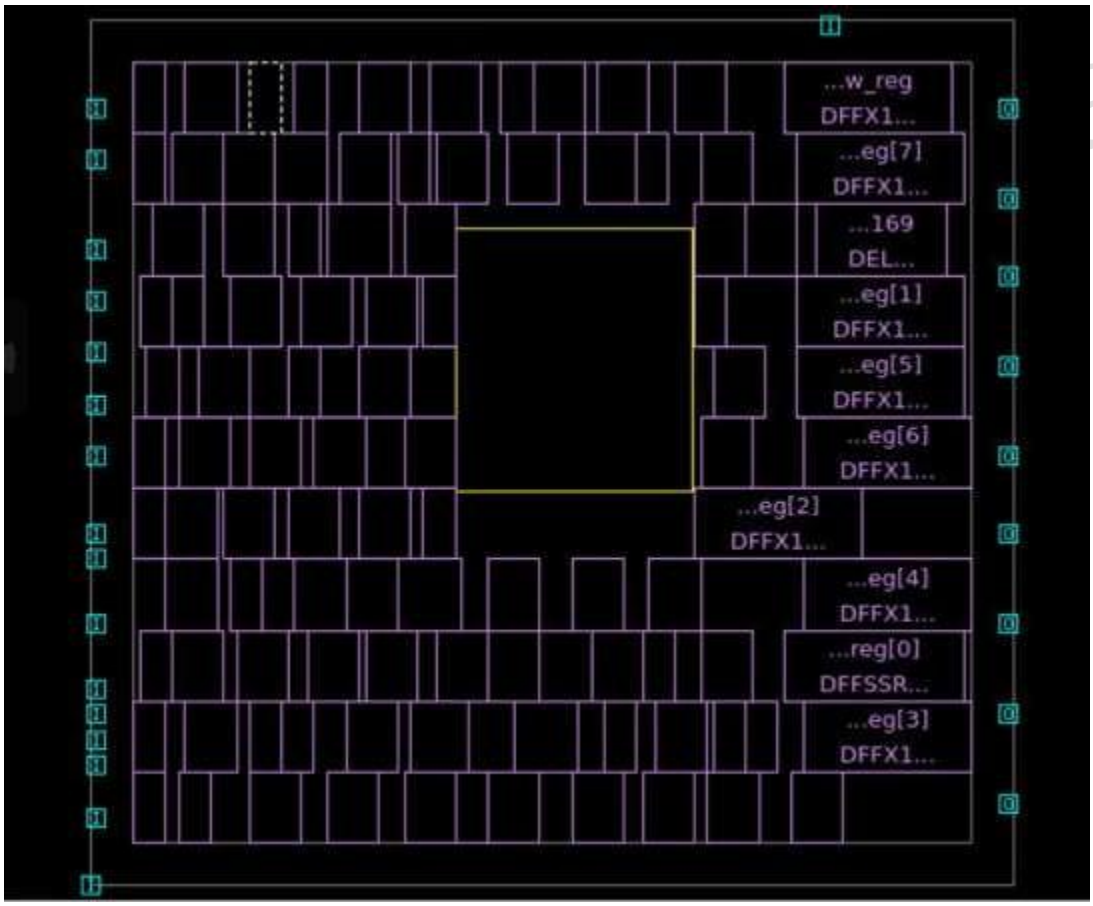
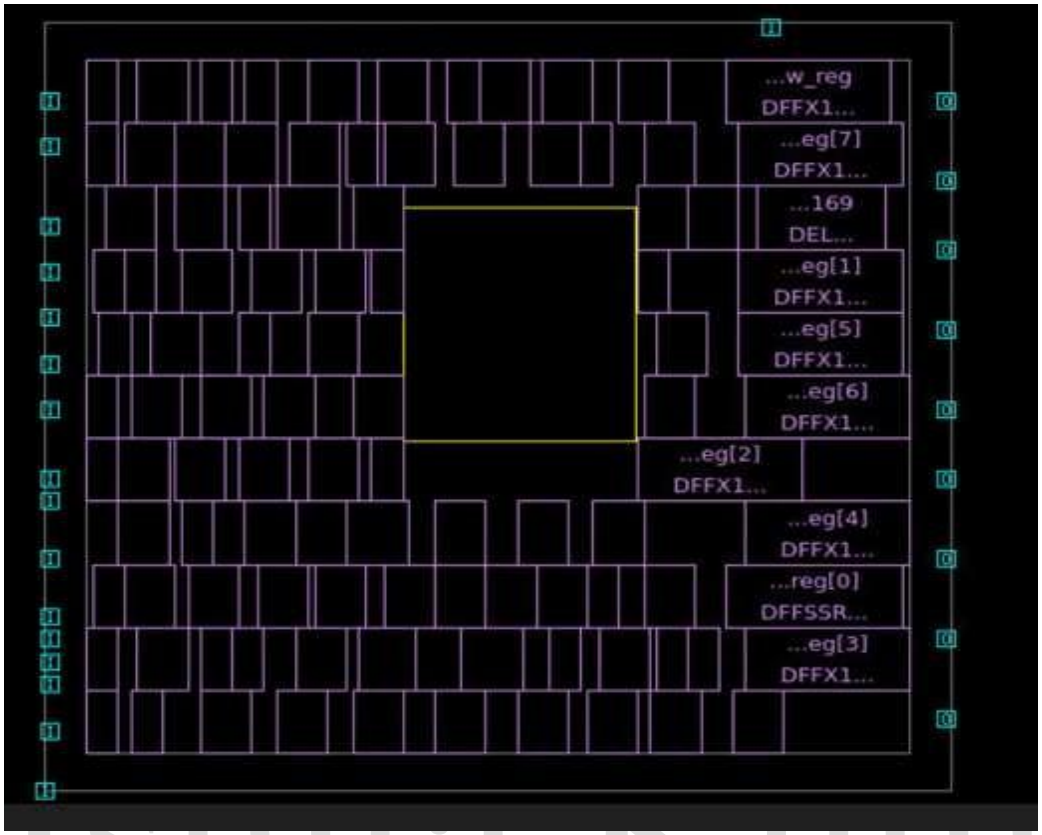
5. M4


IC Compiler II - BlockWindow.1 - Design Planning - SUB8BIT_LIB:sub8bits_cts_ccd.design [write]
Schematic Window Help
Partial Selection
Yes
Replace
Clear
Query
Map
Annotations
View Settings
Layout.1
Apply
100%
Level
Objects
Layers
Settings
Datatypes
Filter layers by name/number
Layers
Arrange By:
Mask
VIA2 (14)
M3 (15)
M3DMY (15:1)
VIA3 (16)
M4 (17)
M4DMY (17:1)
VIA4 (18)
M5 (19)
M5DMY (19:1)
VIA5 (20)
M6 (21)
Preset
Default
...w_reg
DFFX1...
...eg[7]
DFFX1...
...169
DEL...
...eg[1]
DFFX1...
...eg[5]
DFFX1...
...eg[6]
DFFX1...
...eg[2]
DFFX1...
...eg[4]
DFFX1...
...reg[0]
DFFSSR...
...eg[3]
DFFX1...

6. M5


...w_reg
DFFX1...
...eg[7]
DFFX1...
...169
DEL...
...eg[1]
DFFX1...
...eg[5]
DFFX1...
...eg[6]
DFFX1...
...eg[2]
DFFX1...
...eg[4]
DFFX1...
...reg[0]
DFFSSR...
...eg[3]
DFFX1...

7. M6



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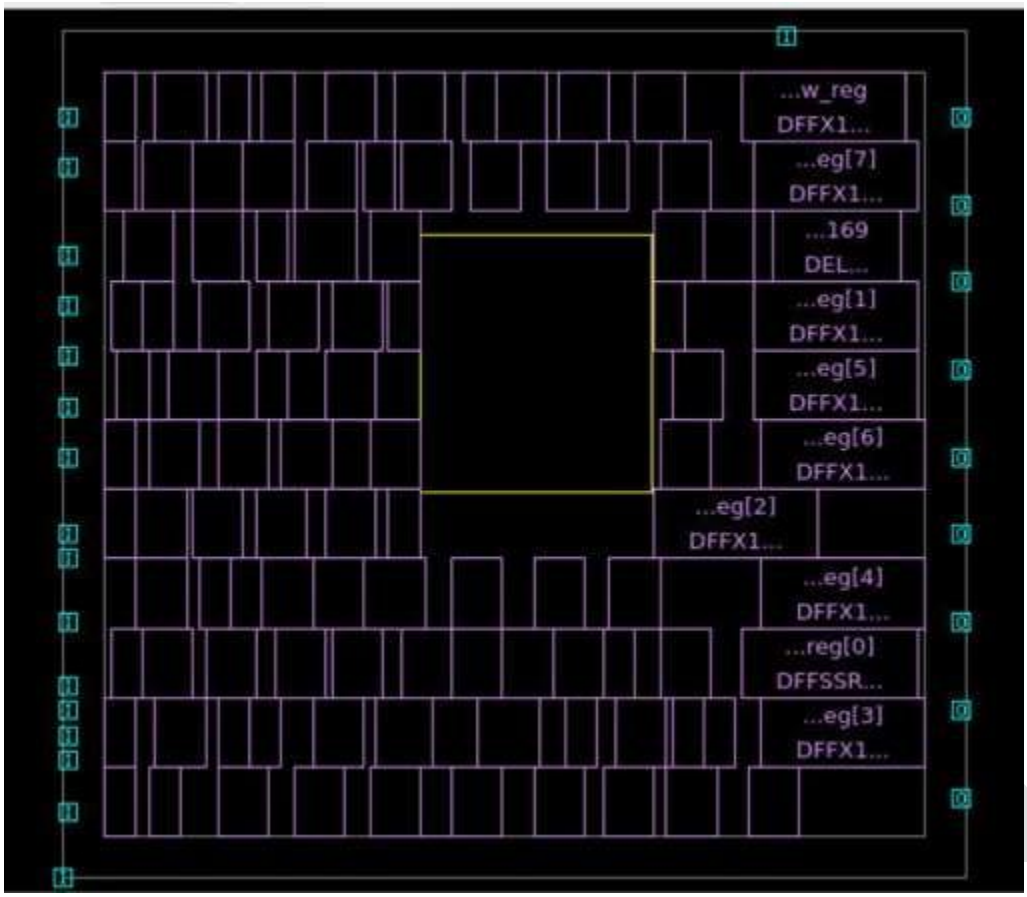
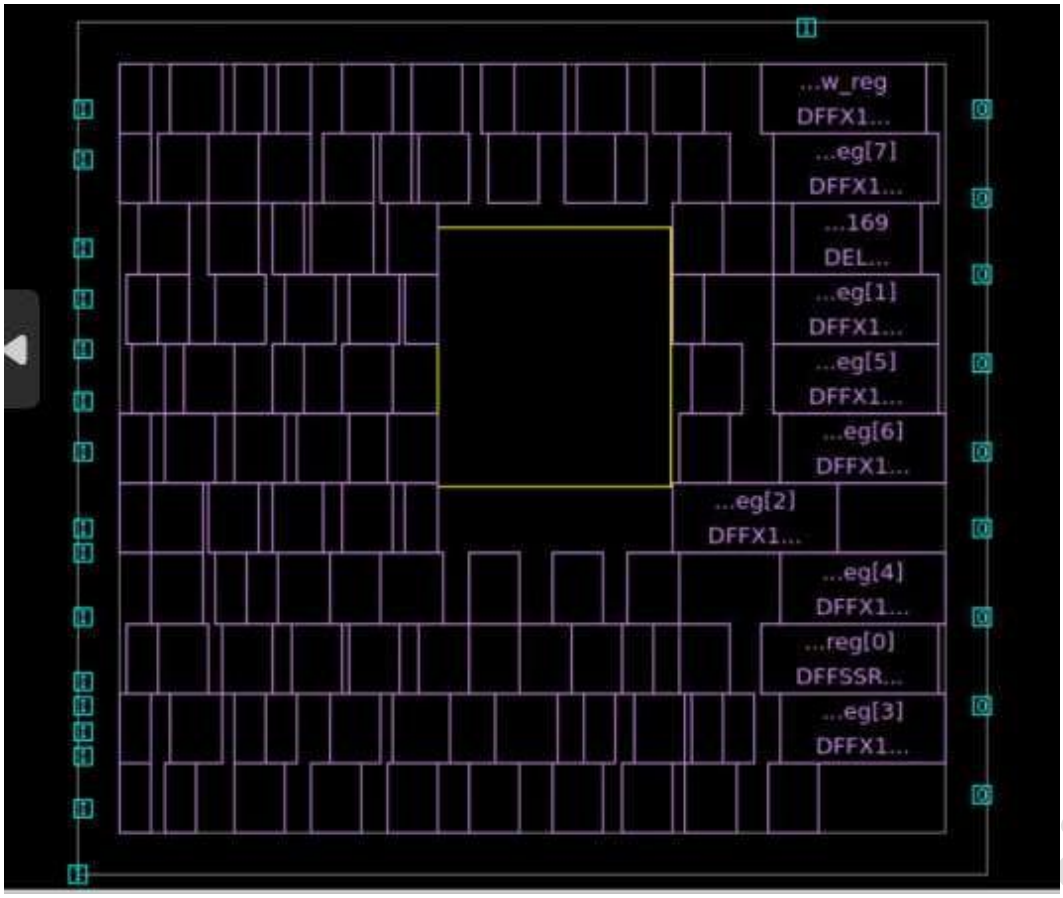
8. M7


...w_reg
DFFX1...
...eg[7]
DFFX1...
...169
DEL...
...eg[1]
DFFX1...
...eg[5]
DFFX1...
...eg[6]
DFFX1...
...eg[2]
DFFX1...
...eg[4]
DFFX1...
...reg[0]
DFFSSR...
...eg[3]
DFFX1...

9. M8


...w_reg
DFFX1...
...eg[7]
DFFX1...
...169
DEL...
...eg[1]
DFFX1...
...eg[5]
DFFX1...
...eg[6]
DFFX1...
...eg[2]
DFFX1...
...eg[4]
DFFX1...
...reg[0]
DFFSSR...
...eg[3]
DFFX1...

report_design

```
    88  history
icc2_shell> report_design
****************************************
Report : design
Design : sub8bit
Version: V-2023.12
Date   : Thu Jul 11 15:47:31 2024
****************************************

Total number of std cells in library : 286
Total number of dont_use lib cells   : 85
Total number of dont_touch lib cells : 7
Total number of buffers              : 11
Total number of inverters            : 15
Total number of flip-flops           : 106
Total number of latches              : 12
Total number of ICGs                 : 12

Cell Instance Type  Count         Area
----------------------------------------
TOTAL LEAF CELLS      104      235.083
unit                  104      235.083
Standard cells        104      235.083
unit                  104      235.083
Hard macro cells        0        0.000
unit                  104      235.083
Soft macro cells        0        0.000
unit                  104      235.083
Always on cells         0        0.000
unit                  104      235.083
Physical only           0        0.000
unit                  104      235.083
Fixed cells             0        0.000
unit                  104      235.083
Moveable cells        104      235.083
```

```
File  Edit  View  Terminal  Tabs  Help
Always on cells          0          0.000
unit                   104        235.083
Physical only            0          0.000
unit                   104        235.083
Fixed cells              0          0.000
unit                   104        235.083
Moveable cells         104        235.083
unit                   104        235.083
Placed cells           103        230.000
unit                   104        235.083
Sequential               9         59.978
unit                   104        235.083
Buffer/inverter         31         43.204
unit                   104        235.083
ICG cells                0          0.000
unit                   104        235.083

Logic Hierarchies                          : 0
Design Masters count                       : 8
Total Flat nets count                      : 123
Total FloatingNets count                   : 0
Total no of Ports                          : 28
Number of Master Clocks in design          : 1
Number of Generated Clocks in design       : 0
Number of Path Groups in design            : 7 (1 of them Non Default
Number of Scan Chains in design            : 0
List of Modes                              : func
List of Corners                            : nom
List of Scenarios                          : func::nom

Core Area                                  : 363.426
Chip Area                                  : 443.730
Total Site Row Area                        : 363.426
Number of Blockages                        : 1
Total area of Blockages                    : 34.720
```

```
Total FloatingNets count             : 0
Total no of Ports                    : 28
Number of Master Clocks in design    : 1
Number of Generated Clocks in design : 0
Number of Path Groups in design      : 7 (1 of them Non Default)
Number of Scan Chains in design      : 0
List of Modes                        : func
List of Corners                      : nom
List of Scenarios                    : func::nom

Core Area                            : 363.426
Chip Area                            : 443.730
Total Site Row Area                  : 363.426
Number of Blockages                  : 1
Total area of Blockages              : 34.720
Number of Power Domains              : 1
Number of Voltage Areas              : 1
Number of Group Bounds               : 0
Number of Exclusive MoveBounds       : 0
Number of Hard or Soft MoveBounds    : 0
Number of Multibit Registers         : 0
Number of Multibit LS/ISO Cells      : 0
Number of Top Level RP Groups        : 0
Number of Tech Layers                : 71 (61 of them have unknown routing dir.)

Total wire length                    : 537.63 micron
Total number of wires                : 575
Total number of contacts             : 506
1
icc2_shell>
```

report_timing:

```
icc2_shell> report_timing
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -report_by design
Design : sub8bit
Version: V-2023.12
Date   : Thu Jul 11 15:48:26 2024
****************************************

  Startpoint: B[1] (input port clocked by Clock)
  Endpoint: diff_reg[7] (rising edge-triggered flip-flop clocked by
  Mode: func
  Corner: nom
  Scenario: func::nom
  Path Group: **in2reg_default**
  Path Type: max

  Point                                                  Incr       Path
  -----------------------------------------------------------------------
  clock Clock (rise edge)                                0.00       0.00
  clock network delay (propagated)                       0.04       0.04
  input external delay                                   0.60       0.64 f
  B[1] (in)                                              0.00       0.64 f
  U53/Y (INVX0_RVT)                                      0.05       0.69 r
  U55/Y (OR2X1_RVT)                                      0.04       0.73 r
```

```
  B[1] (in)                                                0.00       0.64 f
  U53/Y (INVX0_RVT)                                        0.05       0.69 r
  U55/Y (OR2X1_RVT)                                        0.04       0.73 r
  U32/Y (INVX0_RVT)                                        0.01       0.74 f
  U56/Y (OR2X1_RVT)                                        0.03       0.77 f
  U58/Y (AND2X1_RVT)                                       0.04       0.80 f
  ctmTdsLR_1_2/Y (OR3X1_RVT)                               0.03       0.84 f
  ctmTdsLR_1_3/Y (AND3X1_RVT)                              0.04       0.88 f
  ctmTdsLR_1_4/Y (OR3X1_RVT)                               0.03       0.91 f
  U82/Y (AND2X1_RVT)                                       0.03       0.94 f
  U83/Y (AND2X1_RVT)                                       0.04       0.98 f
  ctmTdsLR_1_5/Y (OR3X1_RVT)                               0.03       1.01 f
  U93/Y (AND2X1_RVT)                                       0.03       1.04 f
  U94/Y (AND2X1_RVT)                                       0.03       1.08 f
  U20/Y (INVX0_RVT)                                        0.01       1.09 r
  U109/Y (AND2X1_RVT)                                      0.03       1.12 r
  diff_reg[7]/D (DFFX1_RVT)                                0.00       1.12 r
  data arrival time                                                   1.12

  clock Clock (rise edge)                                  1.00       1.00
  clock network delay (propagated)                         0.12       1.12
  diff_reg[7]/CLK (DFFX1_RVT)                              0.00       1.12 r
  clock uncertainty                                        1.00       2.12
  library setup time                                      -0.02       2.10
  data required time                                                  2.10
  -------------------------------------------------------------------------
  data required time                                                  2.10
  data arrival time                                                  -1.12
  -------------------------------------------------------------------------
  slack (MET)                                                         0.98


1
icc2_shell>
```

Commands for Routing:

```
  67  report_design
  68  report_timing
  69  history
  70  set_app_options -name route.global.timing_driven -value true
  71  set_app_options -name route.global.crosstalk_driven -value false
  72  set_app_options -name route.track.timing_driven -value true
  73  set_app_options -name route.track.crosstalk_driven -value true
  74  set_app_options -name route.detail.timing_driven -value true
  75  set_app_options -name route.detail.force_max_number_iterations -value false
  76  set_app_options -name route.detail.antenna -value true
  77  set_app_options -name route.detail.antenna_fixing_preference -value use_diodes
  78  set_app_options -name route.detail.diode_libcell_names -value */ANTENNA_RVT
  79  route_global
  80  route_track
  81  route_detail
  82  route_opt
  83  write_verilog ./results/sub8bit.routed.v
  84  write_sdc -output ./results/sub8bit.routed.sdc
  85  write_parasitics -format spef -output ./results/sub8bit.spef
  86  save_block
  87  save_lib
  88  history
icc2_shell>
```

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7. TIMING ANALYSIS

It checks the timing closure of the design to ensure all the proper specifications.

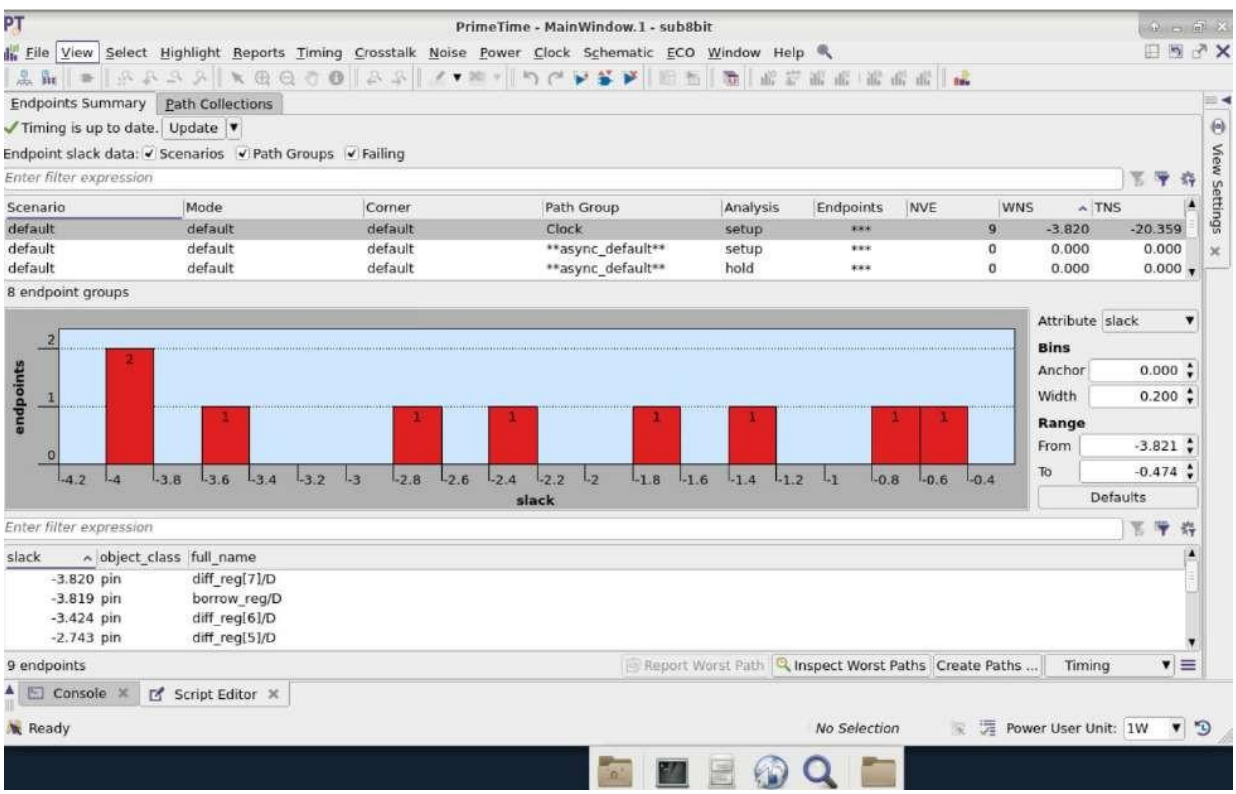
For this we need to invoke pt_shell. Open PT directory in SRM_WORKSHOP directory.

After that start gui and follow the commands:

```
 Inclusivity & Diversity - Visit SolvNetPlus to read the "Synopsys Statement on
            Inclusivity and Diversity" (Refer to article 000036315 at
                        https://solvnetplus.synopsys.com)
pt_shell> start_gui
pt_shell> set link_path "./../ref/lib/stdcell_rvt/saed32rvt_ss0p7vn40c.db"
./../ref/lib/stdcell_rvt/saed32rvt_ss0p7vn40c.db
pt_shell>
pt_shell> read_verilog "./../ICCII/results/sub8bit.routed.v"
1
pt_shell> link_design
Loading db file '/ve/ws_home/ws2_26/SRM_Workshop/ref/lib/stdcell_rvt/saed32rvt_s
s0p7vn40c.db'
Loading verilog file '/ve/ws_home/ws2_26/SRM_Workshop/ICCII/results/sub8bit.rout
ed.v'
Linking design sub8bit...
Information: 286 (97.28%) library cells are unused in library saed32rvt_ss0p7vn4
0c..... (LNK-045)
Information: total 286 library cells are unused (LNK-046)
Design 'sub8bit' was successfully linked.
Information: There are 131 leaf cells, ports, hiers and 121 nets in the design (
LNK-047)
1
pt_shell>
```

```
s0p7vn40c.db'
Loading verilog file '/ve/ws_home/ws2_26/SRM_Workshop/ICCII/results/sub8bit.rout
ed.v'
Linking design sub8bit...
Information: 286 (97.28%) library cells are unused in library saed32rvt_ss0p7vn4
0c..... (LNK-045)
Information: total 286 library cells are unused (LNK-046)
Design 'sub8bit' was successfully linked.
Information: There are 131 leaf cells, ports, hiers and 121 nets in the design (
LNK-047)
1
pt_shell> current_design sub8bit
{"sub8bit"}
pt_shell>
pt_shell> read_sdc ./../CONSTRAINTS/sub8bit.sdc

Reading SDC version 2.1...
Warning: Setting input delay on clock port (Clock) relative to a clock (Clock) d
efined at the same port. Command is ignored. (UITE-489)
Warning: Negative clock uncertainty specified: -1 (UITE-302)
Warning: Negative clock uncertainty specified: -1 (UITE-302)
1
1
pt_shell>
```



```
pt_shell> current_design sub8bit
{"sub8bit"}
pt_shell>
pt_shell> read_sdc ./../CONSTRAINTS/sub8bit.sdc

Reading SDC version 2.1...
Warning: Setting input delay on clock port (Clock) relative to a clock (Clock) d
efined at the same port. Command is ignored. (UITE-489)
Warning: Negative clock uncertainty specified: -1 (UITE-302)
Warning: Negative clock uncertainty specified: -1 (UITE-302)
1
1
pt_shell> read_parasitics "./../ICCII/results/sub8bit.spef.p1_125.spef"
Information: Log for 'read_parasitics command' will be generated in 'parasitics_
command.log'. (PARA-107)
Information: read_parasitics command is executed in background
1
pt_shell>
pt_shell> update_timing -full
Information: Using automatic max wire load selection group 'predcaps'. (ENV-003)
Information: Using automatic min wire load selection group 'predcaps'. (ENV-003)
Information: Building multi voltage information for entire design. (MV-022)
1
pt_shell> report_design
```

report_design:

```
pt_shell> report_design
****************************************
Report : design
Design : sub8bit
Version: V-2023.12
Date   : Thu Jul 11 16:16:39 2024
****************************************

Design Attribute                          Value
--------------------------------------------------------------
Operating Conditions:
  analysis_type                           on_chip_variation
  operating_condition_min_name            ss0p7vn40c
  process_min                             0.99
  temperature_min                         -40
  voltage_min                             0.7
  tree_type_min                           best_case

  operating_condition_max_name            ss0p7vn40c
  process_max                             0.99
  temperature_max                         -40
  voltage_max                             0.7
  tree_type_max                           best_case
```

```
File  Edit  View  Terminal  Tabs  Help
  operating_condition_min_name          ss0p7vn40c
  process_min                           0.99
  temperature_min                       -40
  voltage_min                           0.7
  tree_type_min                         best_case

  operating_condition_max_name          ss0p7vn40c
  process_max                           0.99
  temperature_max                       -40
  voltage_max                           0.7
  tree_type_max                         best_case

Wire Load:                              (use report_wire_load for more informa
ion)
  wire_load_mode                        enclosed
  wire_load_model_max                   8000
  wire_load_model_library_max           saed32rvt_ss0p7vn40c
  wire_load_selection_type_max          automatic-by-area
  wire_load_model_min                   8000
  wire_load_model_library_min           saed32rvt_ss0p7vn40c
  wire_load_selection_type_min          automatic-by-area
  wire_load_selection_group_max         predcaps
  wire_load_selection_group_min         predcaps
```

```
File  Edit  View  Terminal  Tabs  Help
  wire_load_model_max                   8000
  wire_load_model_library_max           saed32rvt_ss0p7vn40c
  wire_load_selection_type_max          automatic-by-area
  wire_load_model_min                   8000
  wire_load_model_library_min           saed32rvt_ss0p7vn40c
  wire_load_selection_type_min          automatic-by-area
  wire_load_selection_group_max         predcaps
  wire_load_selection_group_min         predcaps
  wire_load_min_block_size              0

esign Rules:
  max_capacitance                       --
  min_capacitance                       --
  max_fanout                            --
  max_transition                        0.25
  static_integrity                      --
  dynamic_integrity                     --
  max_coupled_transition                0.25
  max_area                              --

iming Ranges:
  early_factor                          --
  late_factor                           --
```

File Edit View Terminal Tabs Help

```
Design Rules:
  max_capacitance                          --
  min_capacitance                          --
  max_fanout                               --
  max_transition                           0.25
  static_integrity                         --
  dynamic_integrity                        --
  max_coupled_transition                   0.25
  max_area                                 --

Timing Ranges:
  early_factor                             --
  late_factor                              --

Pin Input Delays:
None specified.

Pin Output Delays:
None specified.
Fast Analysis:                             disabled

1
pt_shell>
```

report_timing:

```
1
pt_shell> report_timing
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -sort_by slack
Design : sub8bit
Version: V-2023.12
Date   : Thu Jul 11 16:17:45 2024
****************************************


  Startpoint: B[1] (input port clocked by Clock)
  Endpoint: diff_reg[7]
              (rising edge-triggered flip-flop clocked by Clock)
  Path Group: Clock
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock Clock (rise edge)                  0.00       0.00
```

```
  Point                                        Incr       Path
  -----------------------------------------------------------
  clock Clock (rise edge)                      0.00       0.00
  clock network delay (ideal)                  0.00       0.00
  input external delay                         0.60       0.60 f
  B[1] (in)                                    0.00 &     0.60 f
  U53/Y (INVX0_RVT)                            0.22 &     0.82 r
  U55/Y (OR2X1_RVT)                            0.28 &     1.10 r
  U32/Y (INVX0_RVT)                            0.09 &     1.19 f
  U56/Y (OR2X1_RVT)                            0.32 &     1.51 f
  U58/Y (AND2X1_RVT)                           0.30 &     1.81 f
  ctmTdsLR_1_2/Y (OR3X1_RVT)                   0.48 &     2.30 f
  ctmTdsLR_1_3/Y (AND3X1_RVT)                  0.42 &     2.71 f
  ctmTdsLR_1_4/Y (OR3X1_RVT)                   0.49 &     3.20 f
  U82/Y (AND2X1_RVT)                           0.33 &     3.53 f
  U83/Y (AND2X1_RVT)                           0.33 &     3.86 f
  ctmTdsLR_1_5/Y (OR3X1_RVT)                   0.47 &     4.33 f
  U93/Y (AND2X1_RVT)                           0.32 &     4.65 f
  U12/Y (OR2X1_RVT)                            0.38 &     5.03 f
  U109/Y (AND2X1_RVT)                          0.26 &     5.29 f
  diff_reg[7]/D (DFFX1_RVT)                    0.00 &     5.29 f
  data arrival time                                       5.29

  clock Clock (rise edge)                      1.00       1.00
```

```
  U12/Y (OR2X1_RVT)                                0.38 &     5.03 f
  U109/Y (AND2X1_RVT)                              0.26 &     5.29 f
  diff_reg[7]/D (DFFX1_RVT)                        0.00 &     5.29 f
  data arrival time                                           5.29

  clock Clock (rise edge)                          1.00       1.00
  clock network delay (ideal)                      0.00       1.00
  clock reconvergence pessimism                    0.00       1.00
  clock uncertainty                                1.00       2.00
  diff_reg[7]/CLK (DFFX1_RVT)                                 2.00 r
  library setup time                              -0.53       1.47
  data required time                                          1.47
  -------------------------------------------------------------------
  data required time                                          1.47
  data arrival time                                          -5.29
  -------------------------------------------------------------------
  slack (VIOLATED)                                           -3.82


1
pt_shell>
```

Here the stack is violated, so we need to fix it by tinkering .sdc file:

Ishita Kumari

```
File   Edit   View   Terminal   Tabs   Help
create_clock -period 1 [get_ports Clock]

set_input_delay -max 0.6 -clock Clock [all_inputs]
set_input_transition 0.15 [all_inputs]

set_output_delay -max 0.4 -clock Clock [all_outputs]

set_clock_uncertainty -setup -5.00 [get_clocks Clock]
set_clock_uncertainty -hold -5.00 [get_clocks Clock]
set_max_transition 0.250 [current_design]
set_max_transition -clock_path 0.1 [get_clocks Clock]

~
~
~
~
```

Report_design after fixing slack:

```
pt_shell> report_design
****************************************
Report : design
Design : sub8bit
Version: V-2023.12
Date   : Thu Jul 11 16:34:00 2024
****************************************

Design Attribute                          Value
--------------------------------------------------------------------------
Operating Conditions:
  analysis_type                           on_chip_variation
  operating_condition_min_name            ss0p7vn40c
  process_min                             0.99
  temperature_min                         -40
  voltage_min                             0.7
  tree_type_min                           best_case

  operating_condition_max_name            ss0p7vn40c
  process_max                             0.99
  temperature_max                         -40
  voltage_max                             0.7
  tree_type_max                           best_case

Wire Load:                                (use report_wire_load for more informat
ion)
  wire_load_mode                          enclosed
```

```
ion)
  wire_load_mode                          enclosed
  wire_load_model_max                     8000
  wire_load_model_library_max             saed32rvt_ss0p7vn40c
  wire_load_selection_type_max            automatic-by-area
  wire_load_model_min                     8000
  wire_load_model_library_min             saed32rvt_ss0p7vn40c
  wire_load_selection_type_min            automatic-by-area
  wire_load_selection_group_max           predcaps
  wire_load_selection_group_min           predcaps
  wire_load_min_block_size                0

Design Rules:
  max_capacitance                         --
  min_capacitance                         --
  max_fanout                              --
  max_transition                          0.25
  static_integrity                        --
  dynamic_integrity                       --
  max_coupled_transition                  0.25
  max_area                                --

Timing Ranges:
  early_factor                            --
  late_factor                             --

Pin Input Delays:
None specified.

Pin Output Delays:
None specified.
Fast Analysis:                            disabled

1
pt_shell>
```

Report_timing after fixing slack:

```
pt_shell> report_timing
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -sort_by slack
Design : sub8bit
Version: V-2023.12
Date   : Thu Jul 11 16:33:47 2024
****************************************


  Startpoint: B[1] (input port clocked by Clock)
  Endpoint: diff_reg[7]
              (rising edge-triggered flip-flop clocked by Clock)
  Path Group: Clock
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock Clock (rise edge)                  0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     0.60       0.60 f
  B[1] (in)                                0.00 &     0.60 f
  U53/Y (INVX0_RVT)                        0.22 &     0.82 r
  U55/Y (OR2X1_RVT)                        0.28 &     1.10 r
  U32/Y (INVX0_RVT)                        0.09 &     1.19 f
  U56/Y (OR2X1_RVT)                        0.32 &     1.51 f
  U58/Y (AND2X1_RVT)                       0.30 &     1.81 f
  ctmTdsLR_1_2/Y (OR3X1_RVT)               0.48 &     2.30 f
  ctmTdsLR_1_3/Y (AND3X1_RVT)              0.42 &     2.71 f
  ctmTdsLR_1_4/Y (OR3X1_RVT)               0.49 &     3.20 f
```

```
clock network delay (ideal)                    0.00        0.00
input external delay                           0.60        0.60 f
B[1] (in)                                      0.00 &      0.60 f
U53/Y (INVX0_RVT)                              0.22 &      0.82 r
U55/Y (OR2X1_RVT)                              0.28 &      1.10 r
U32/Y (INVX0_RVT)                              0.09 &      1.19 f
U56/Y (OR2X1_RVT)                              0.32 &      1.51 f
U58/Y (AND2X1_RVT)                             0.30 &      1.81 f
ctmTdsLR_1_2/Y (OR3X1_RVT)                     0.48 &      2.30 f
ctmTdsLR_1_3/Y (AND3X1_RVT)                    0.42 &      2.71 f
ctmTdsLR_1_4/Y (OR3X1_RVT)                     0.49 &      3.20 f
U82/Y (AND2X1_RVT)                             0.33 &      3.53 f
U83/Y (AND2X1_RVT)                             0.33 &      3.86 f
ctmTdsLR_1_5/Y (OR3X1_RVT)                     0.47 &      4.33 f
U93/Y (AND2X1_RVT)                             0.32 &      4.65 f
U12/Y (OR2X1_RVT)                              0.38 &      5.03 f
U109/Y (AND2X1_RVT)                            0.26 &      5.29 f
diff_reg[7]/D (DFFX1_RVT)                      0.00 &      5.29 f
data arrival time                                          5.29

clock Clock (rise edge)                        1.00        1.00
clock network delay (ideal)                    0.00        1.00
clock reconvergence pessimism                  0.00        1.00
clock uncertainty                              5.00        6.00
diff_reg[7]/CLK (DFFX1_RVT)                                6.00 r
library setup time                            -0.53        5.47
data required time                                         5.47
-------------------------------------------------------------------
data required time                                         5.47
data arrival time                                         -5.29
-------------------------------------------------------------------
slack (MET)                                                0.18
```

Isuna Kumari

Slack met with value 0.18.

Commands of timing analysis:

```
Terminal - ws2_26@ws2:~/SRM_Workshop/PT
File  Edit  View  Terminal  Tabs  Help
Pin Output Delays:
None specified.
Fast Analysis:                          disabled

1
check_timing -verbose > ./reports/check_timing/check_timing.p1_report
pt_shell> report_global_timing > ./reports/timing/report_global_timing.p1_report
pt_shell> report_clock -skew -attribute > ./reports/clock/report_clock.p1_report
pt_shell> report_analysis_coverage > ./reports/analysis_coverage/report_analysis_coverage.p1_report
pt_shell> report_timing -slack_lesser_than 0.0 -delay min_max -nosplit -input -net  > ./reports/timing/report_timing.p1_report
pt_shell>
pt_shell> save_block
Information: Checked out license 'ECO-APX' (PT-019)
Error: Required argument '-as' was not found (CMD-007)
pt_shell> history
    1  start
    2  start_gui
    3  set link_path "./../ref/lib/stdcell_rvt/saed32rvt_ss0p7vn40c.db"
    4  read_verilog "./../ICCII/results/sub8bit.routed.v"
    5  link_design
    6  current_design sub8bit
    7  read_sdc ./../CONSTRAINTS/sub8bit.sdc
    8  read_parasitics "./../ICCII/results/sub8bit.spef.p1_125.spef"
    9  update_timing -full
   10  report_timing
   11  report_design
   12  check_timing -verbose > ./reports/check_timing/check_timing.p1_report
   13  report_global_timing > ./reports/timing/report_global_timing.p1_report
   14  report_clock -skew -attribute > ./reports/clock/report_clock.p1_report
   15  report_analysis_coverage > ./reports/analysis_coverage/report_analysis_coverage.p1_report
   16  report_timing -slack_lesser_than 0.0 -delay min_max -nosplit -input -net  > ./reports/timing/report_timing.p1_report
   17  save_block
   18  history
```

CONCLUSION

The 8-bit subtractor designed with Synopsys tools meets all the required performance benchmarks for timing, size, and power use.

Both the synthesis and placement processes finished without issues, ensuring that the main timing challenges were well managed with no setup or hold time problems.

The layout was optimized effectively to use the silicon area efficiently, and power analysis showed low levels of power usage, both during operation and when idle.

Overall, the design stands robust and reliable, poised for further validation and potential fabrication.

Ishita Kumari

It has effectively fulfilled all specified operational requirements and constraints, validating its readiness for advanced testing and eventual production.