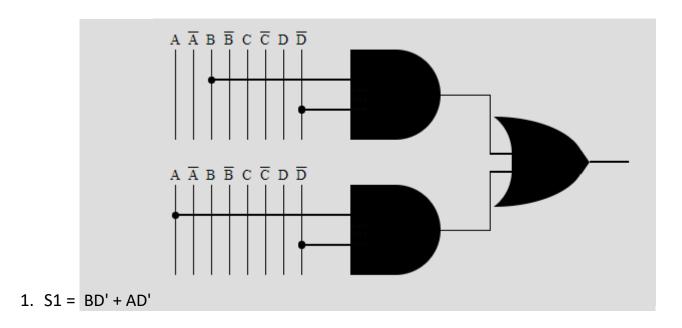
## Group - 9, Section - B1

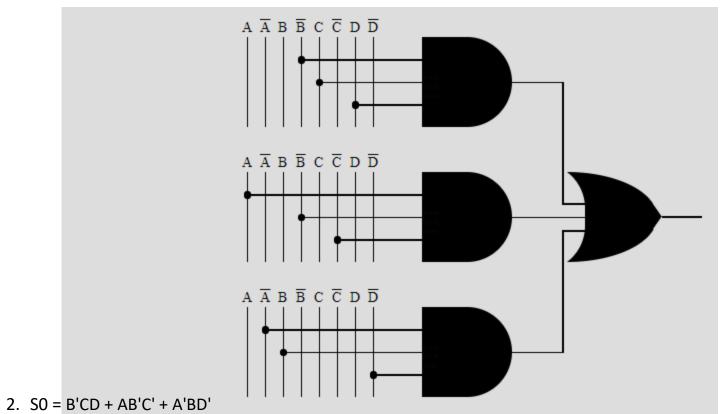
OPCODE				CODE	Operation	ALU	ALU Selection		RegDST	ALUSRC	MemToReg	RegWrite	MemRead	MemWrite	Branch	Jump
OP3	OP2	OP1	OP0	CODE	Operation	Operation	S1	S0	NEEDST	ALUSAC	ivieiiiToneg	vekwure	ivieiiinedu	ivieiiivviite	BIGIICII	Julip
0	0	0	1	I	lw	Add	0	0	0	1	1	1	1	0	0	0
0	0	1	0	J	SW	Add	0	0	Х	1	х	0	0	1	0	0
0	0	1	1	К	beq	Sub	0	1	Х	0	х	0	0	0	1	0
0	1	0	0	L	j	Х	Х	х	Х	Х	х	0	0	0	Х	1
0	1	0	1	С	addi	Add	0	0	0	1	0	1	0	0	0	0
0	1	1	0	Н	ori	OR	1	1	0	1	0	1	0	0	0	0
0	1	1	1	А	add	Add	0	0	1	0	0	1	0	0	0	0
1	0	0	0	G	or	OR	1	1	1	0	0	1	0	0	0	0
1	0	0	1	В	sub	Sub	0	1	1	0	0	1	0	0	0	0
1	0	1	0	E	and	AND	1	0	1	0	0	1	0	0	0	0
1	0	1	1	D	subi	Sub	0	1	0	1	0	1	0	0	0	0
1	1	0	0	F	andi	AND	1	0	0	1	0	1	0	0	0	0

## <u>ICs</u>

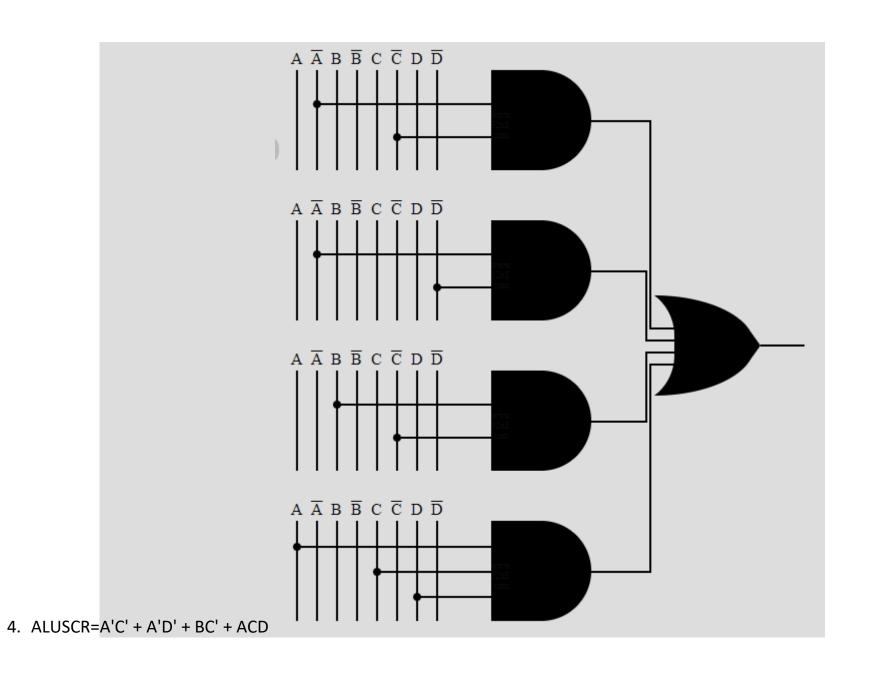
- 1. ALU IC74LS381
- 2. ROM IC2764
- 3.
- 4. 2114
- 5. 2732

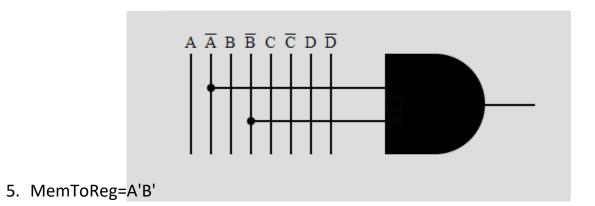
## **Functions**

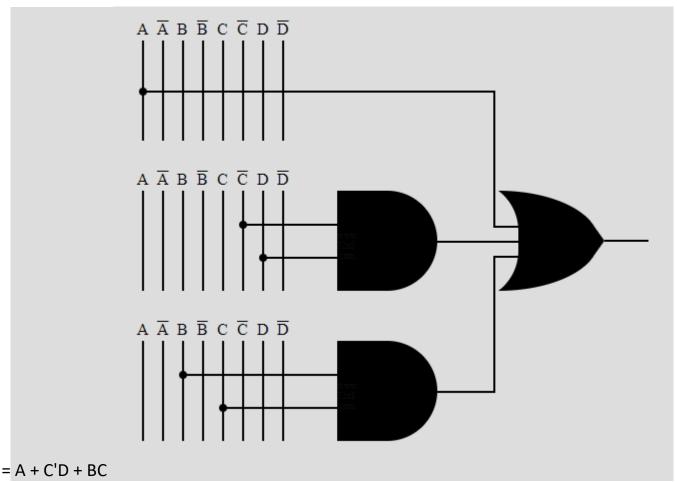




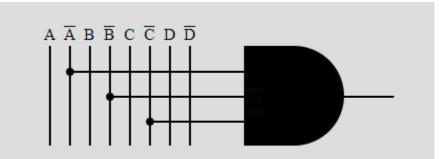
- 3. RegDST = B'D' + AB'C' + A'CD



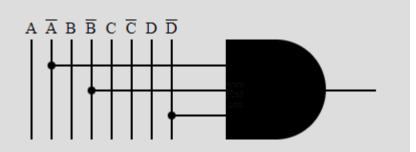




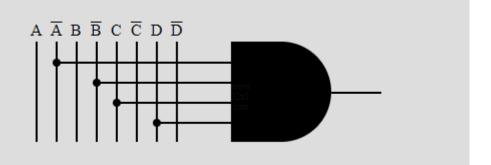
6. RegWrite = A + C'D + BC



7. MemRead =A'B'C'



8. MemWrite =A'B'D'



9. Branch = A'B'CD

