Fundamentals of ANALOG INTERFACING

Lecture 10a

MCT-236: Embedded Systems-I

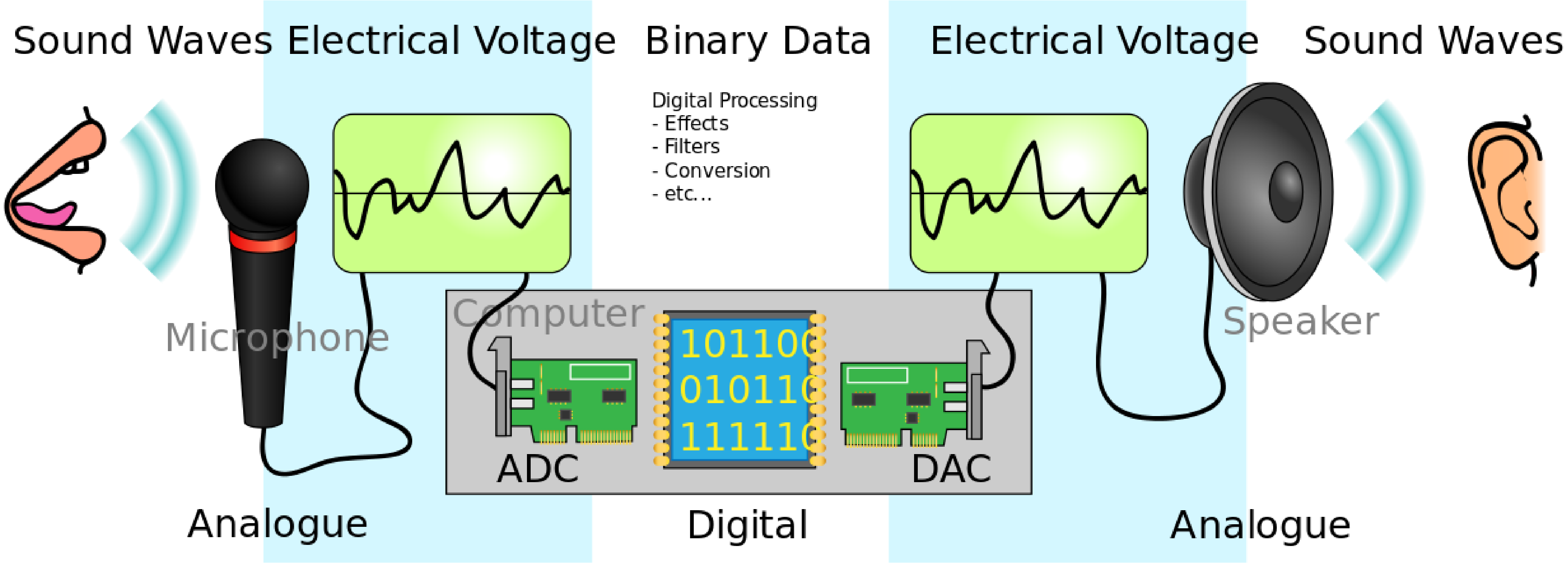
Agenda

- Why We Need Analog Interfacing?
- Digital Representation of Analog Signal
- Analog-to-Digital Converter Types

Why we need Analog Interfacing?

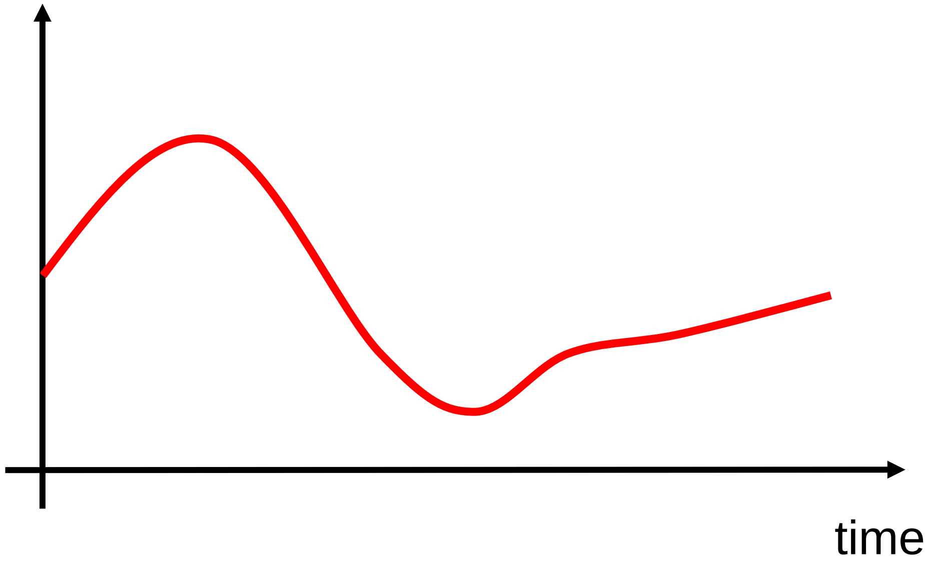
- Real world is analog by nature
- Analog signals are prone to noise – difficult to detect noise

Embedded System Example



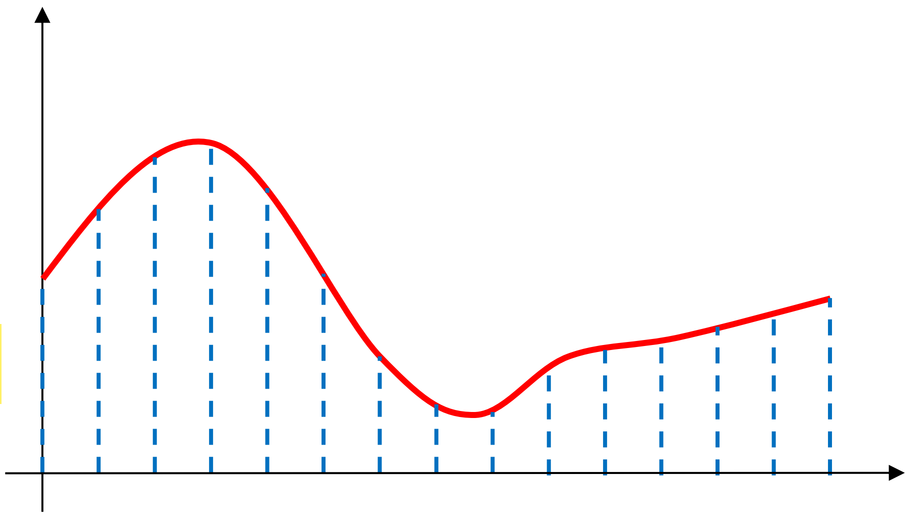
Digital Representation of Analog Signal

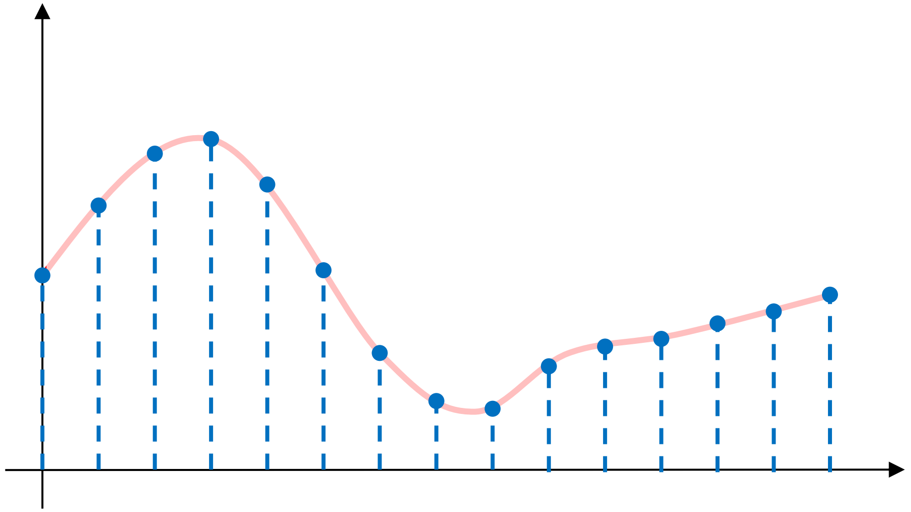
- Analog signal is continuous in both time and amplitude
- Analog-to-digital conversion is a 3 steps process:
  - Sampling
  - Quantization
  - Encoding



Sampling

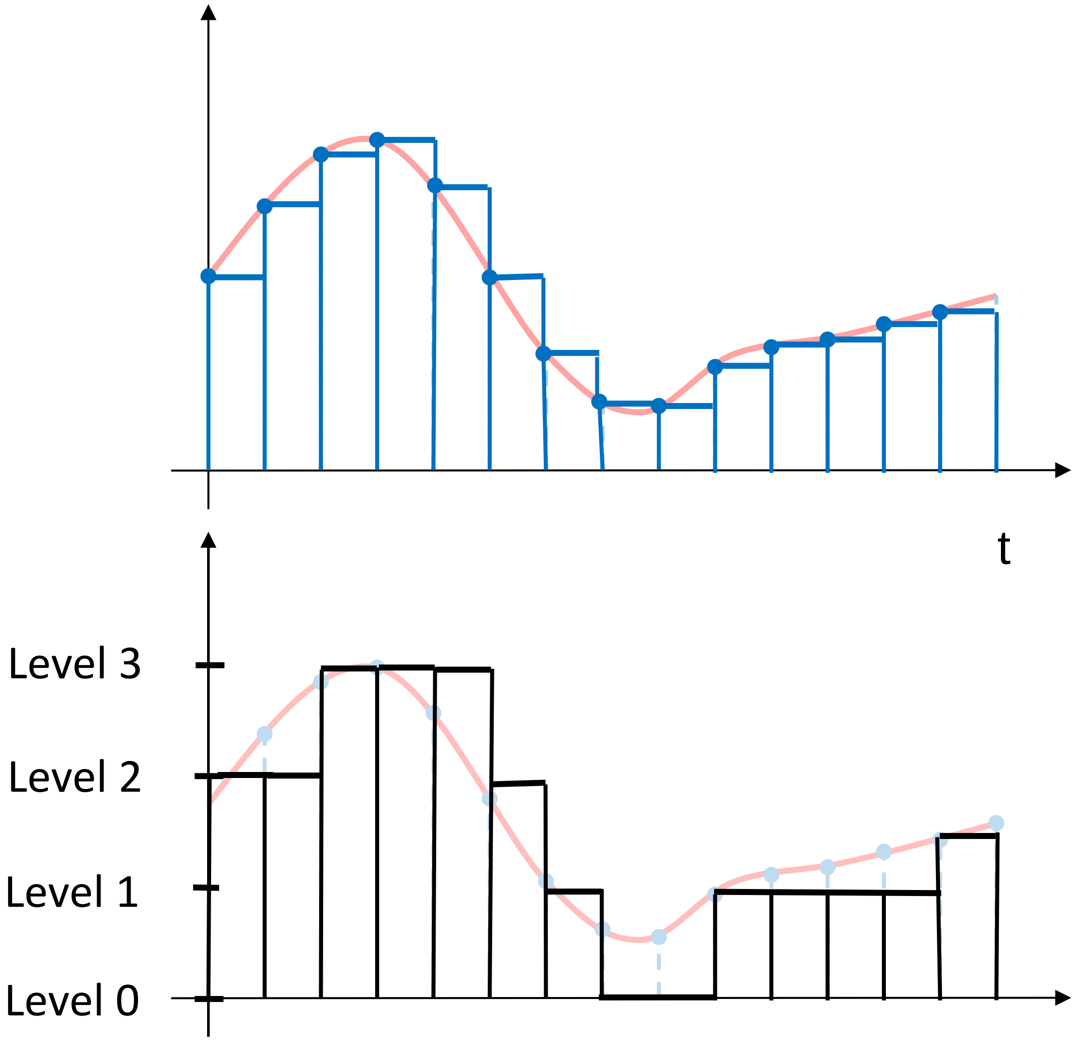
- Measuring analog signal at uniform time intervals
- Sampling converts and analog signal to discrete time signal, but amplitude remains continuous
- ***Nyquist Criterion:*** sampling rate must be greater than double the highest frequency to be sampled
- High sampling rate, more storage required
- ***Aliasing*** occurs when signal is changing much faster than the sample rate





Quantization

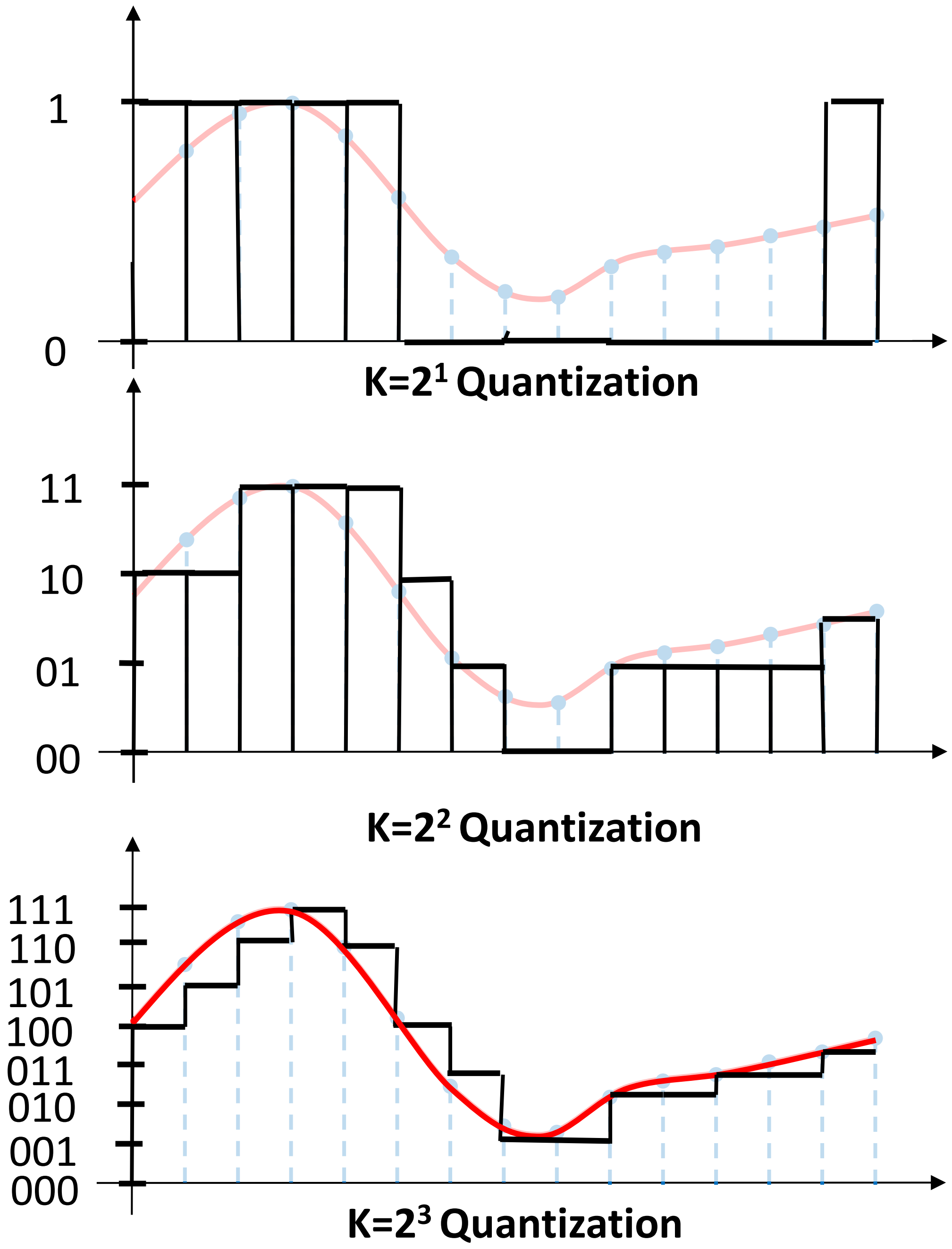
- ADC divide the total signal span into m distinct levels called ***Quantization Levels***
- Mapping a signal sample to the nearest quantization level is called **Quantization**
- Quantization results discrete time discrete amplitude signal i.e. ***Digital Signal***
- ***Resolution***: no. of bits used to represent the analog value
- For n-bit ADC, 2^n quantization levels
- Optimize the resolution to avoid information loss



$K=2^2$ Quantization

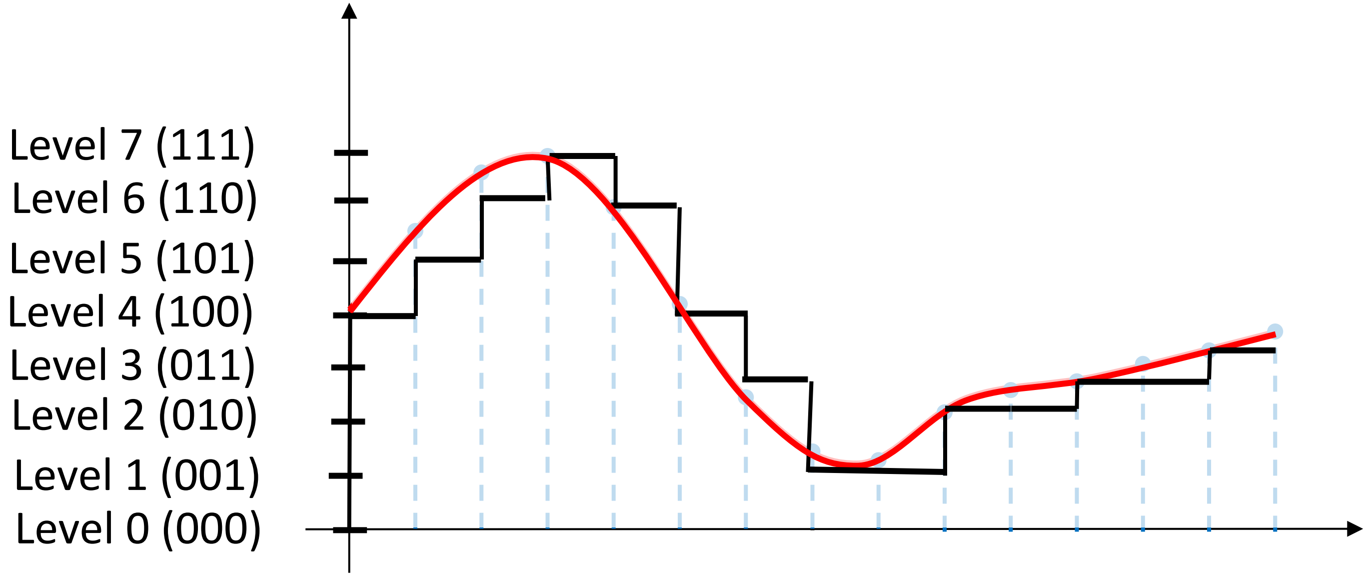
Quantization

- Better resolution required for better representation, but more storage required
- Quantization Error is less with greater quantization levels
- 16-bit representation will require twice the storage space as compared to 8-bit, but quality will be far better



Encoding

- Different quantized levels can be corresponded by using binary encoding
- Using a 3-bit ADC, a sample quantized to level 5 will have binary coded value 101

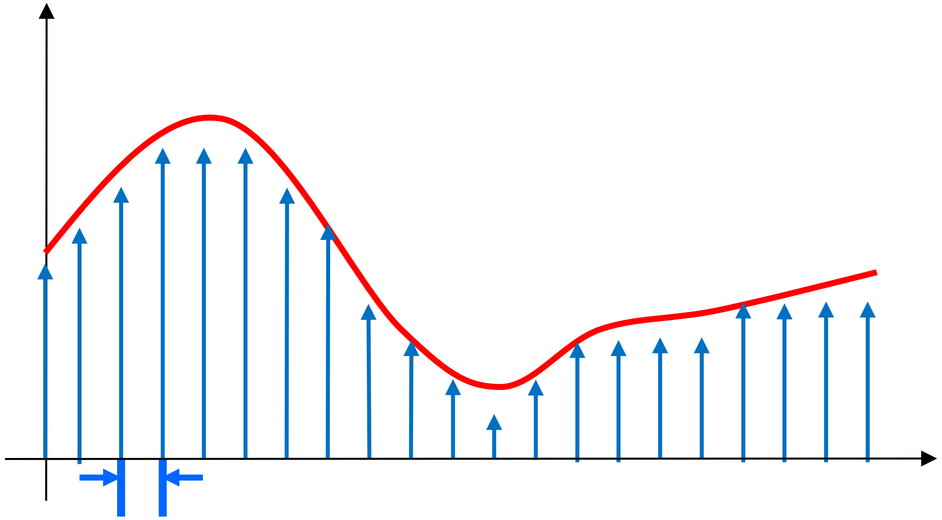


K=2^3 Quantization

ADC Accuracy can be improved by increase

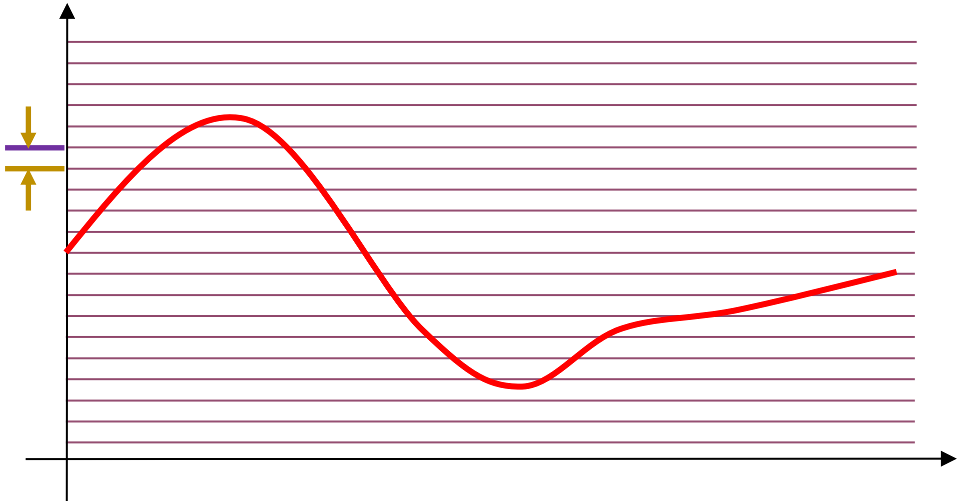
Sampling Rate, Ts

- Based on number of steps required in the conversion process
- Increases the maximum frequency that can be measured

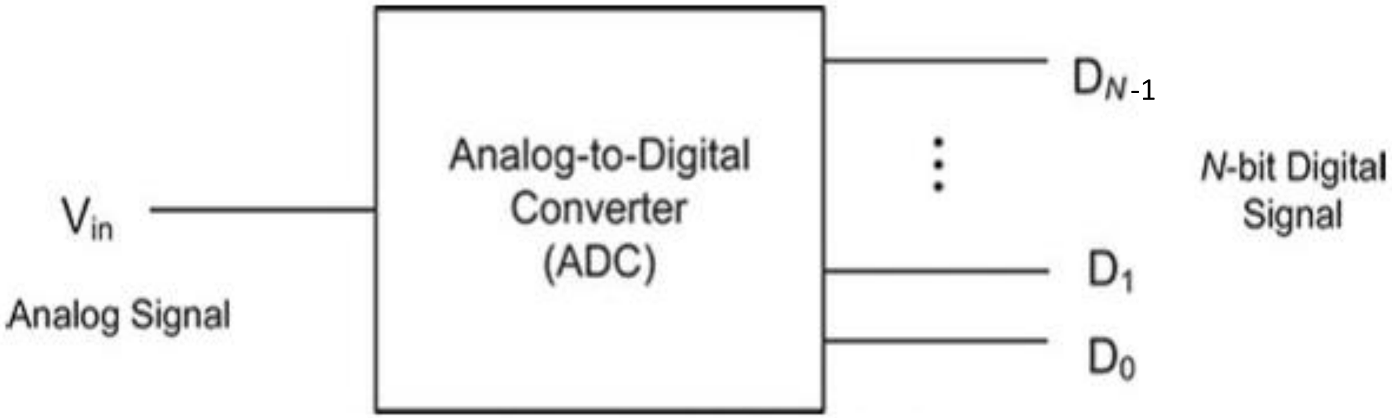


Resolution, Q

- Improves accuracy in measuring amplitude of analog signal



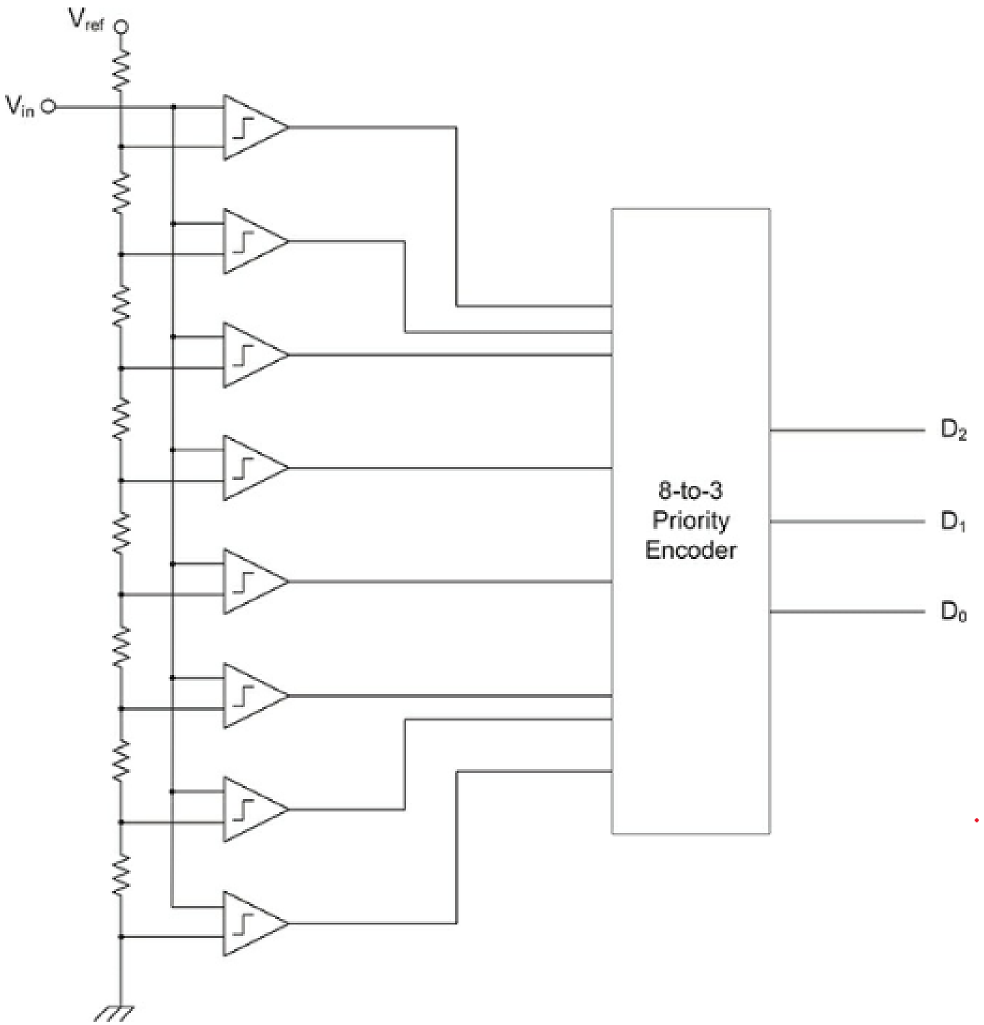
Analog-to-Digital Converter Types



- ADC Design falls into four broad categories
  - Parallel Design
  - DAC based Design
  - Integrator Based Design
  - Sigma Delta Design

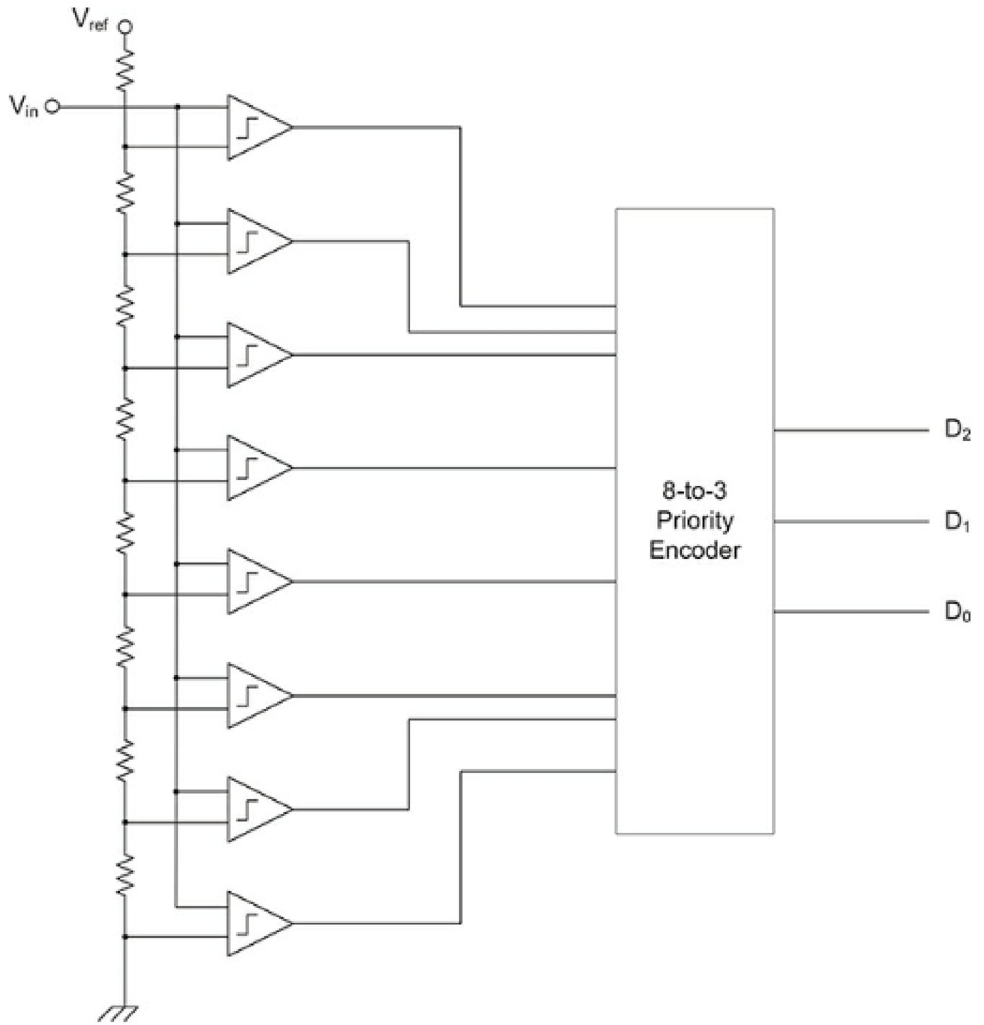
Parallel Design

- Voltage Comparators (Op-Amps) and a Priority Encoder are main components
- Compares input signal against a reference and generates output accordingly
- Parallel, also known as Flash, Design is simple and fastest ADC type
- 2^N comparators required for N-bit ADC



Parallel Design

Truth Table of 8-to-3 Priority Encoder										
Digital Inputs								Binary Out		
V7	V6	V5	V4	V3	V2	V1	V0	D2	D1	D0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	X	0	0	1
0	0	0	0	0	1	X	X	0	1	0
0	0	0	0	1	X	X	X	0	1	1
0	0	0	1	X	X	X	X	1	0	0
0	0	1	X	X	X	X	X	1	0	1
0	1	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	1	1	1

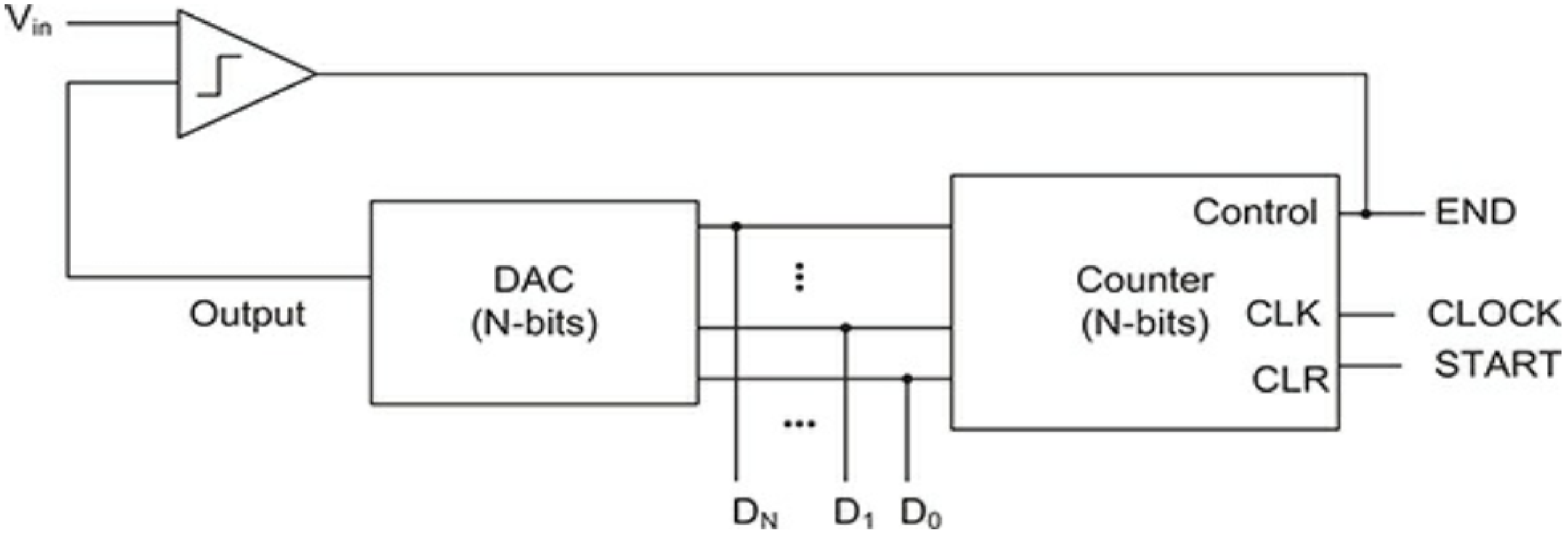


DAC Based ADC Design

- Two well-known DAC based ADC design are
  - Ramp Counter Based ADC
  - Successive Approximation Based ADC

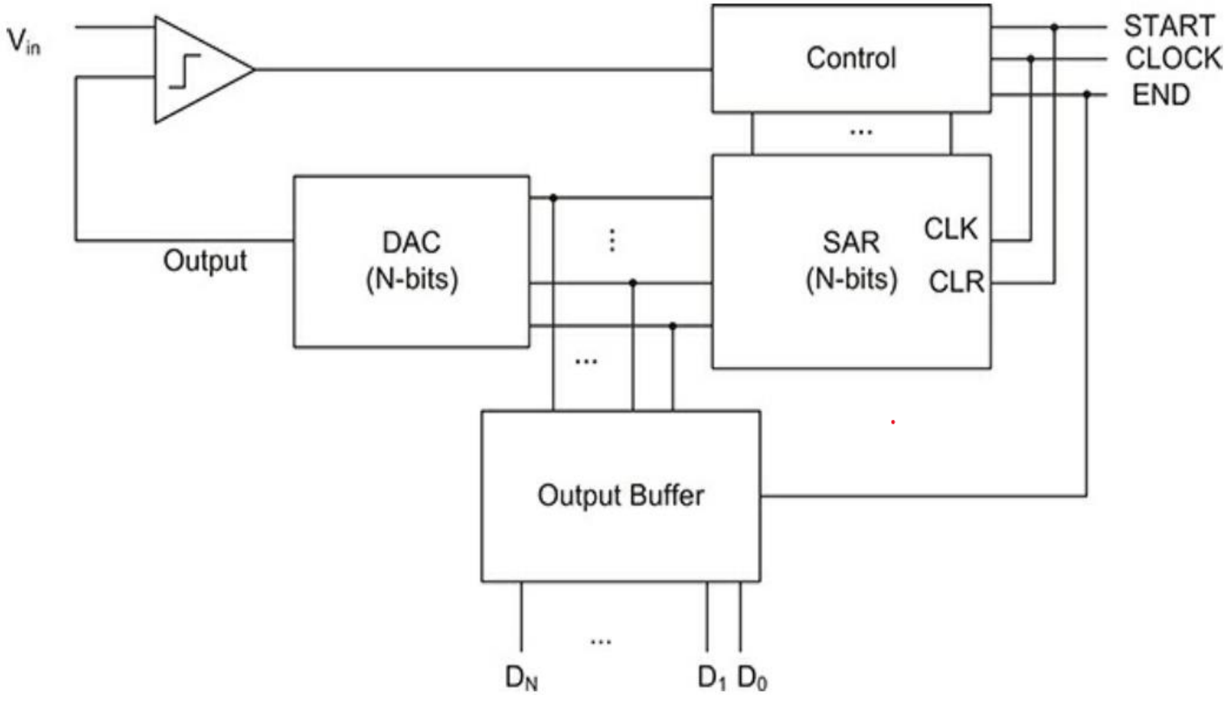
Ramp Counter Based ADC

- Counter starts counting from 0 toward maximum possible value of $2^N – 1$, until finds correct digital equivalent for input
- Really slow technique, at most $2^N – 1$ clock cycles required to convert a sample



Successive Approximation Based ADC

- Most widely used ADC Design
- Conversion starts by setting MSB of ADC and comparing DAC output with input
- The op-amp output will update the control unit if this bit should remain set to 1 or should be updated to 0
- The process continues until we reach LSB
- Fast technique as it requires only N clock cycles to convert a sample
- Also suitable for converting multiple analog signals using multiplexing

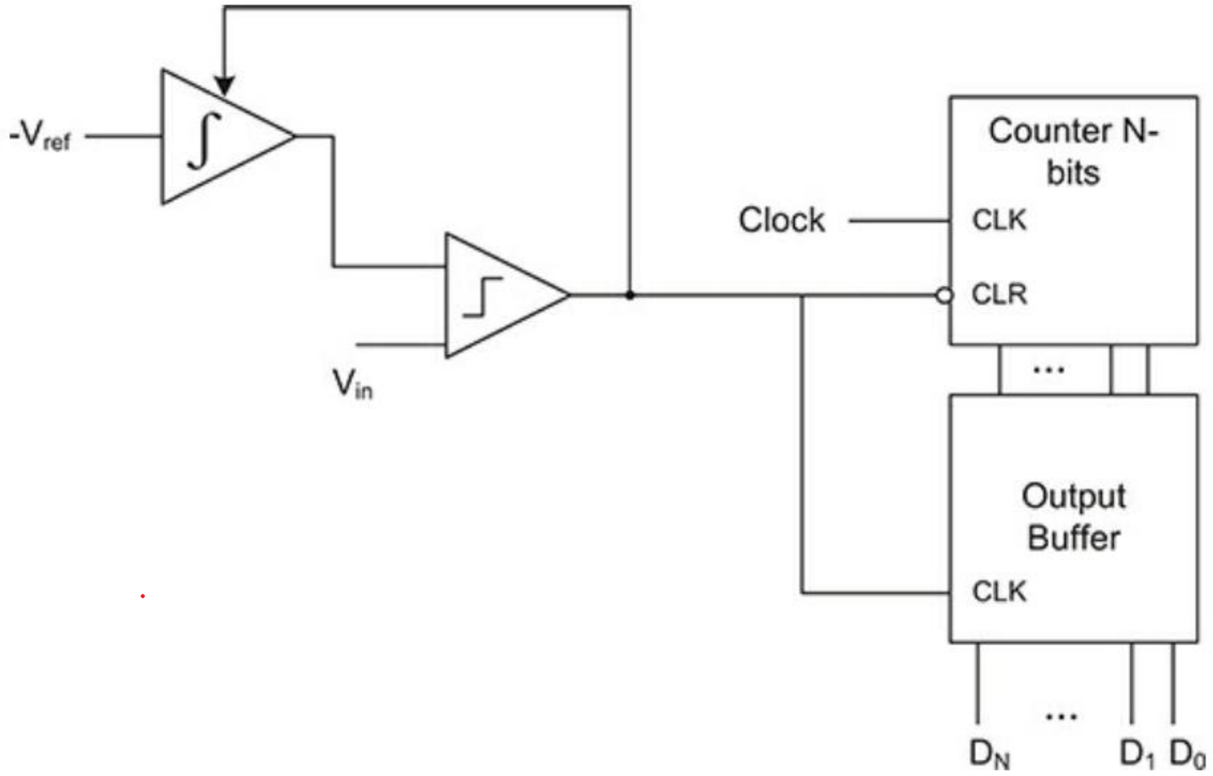


Integrator Based ADC Design

- Can achieve high resolution at the expense of speed even at moderate sampling rates
- Two widely used integrator based ADC design are
  - Single Slope ADC
  - Dual Slope ADC

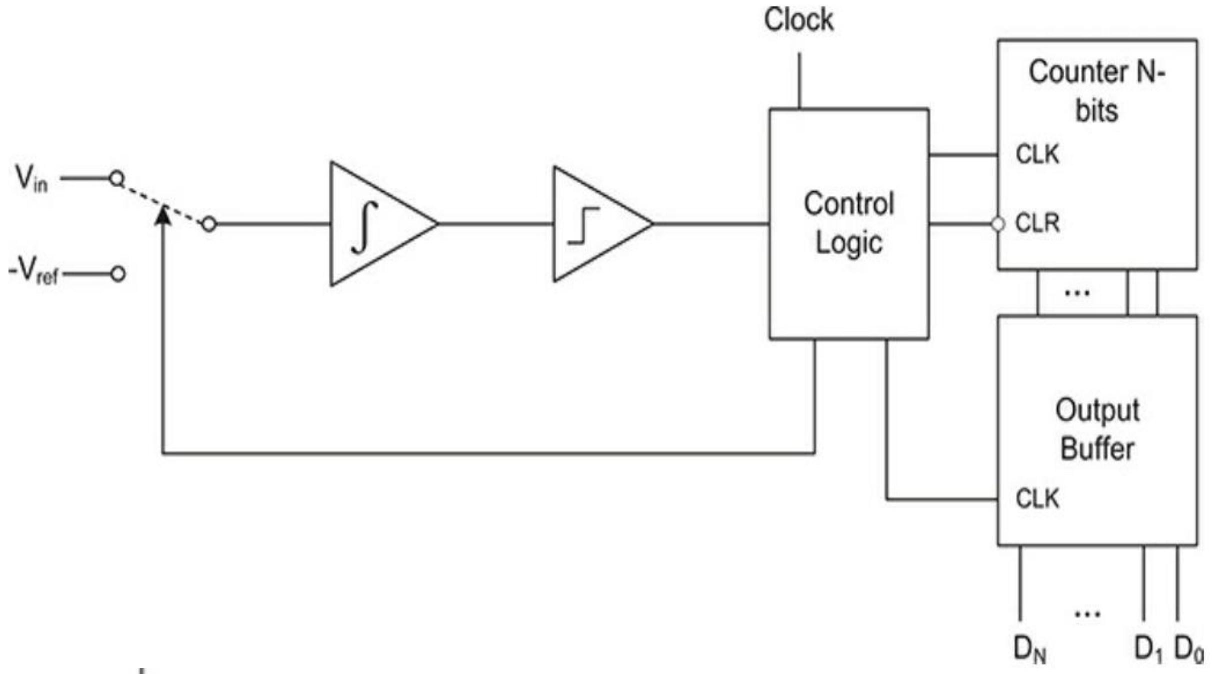
Single Slope ADC

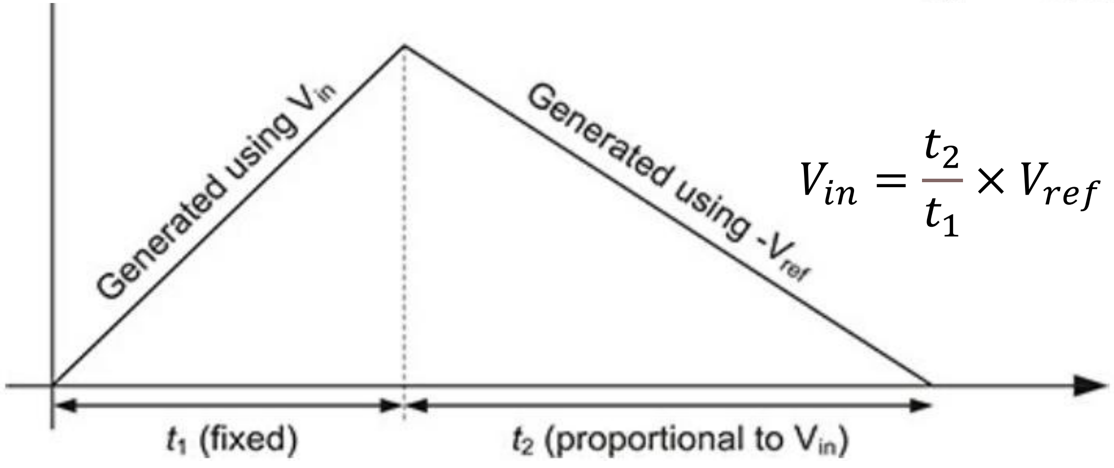
- Comparator compares the input against integrator output, which is 0 initially
- Counter starts counting from 0 to $2^N – 1$, until input and integrator output become equal
- Counter stores output values to Output Buffer and comparator output resets the counter to allow start conversion for next sample
- Slow technique, at most $2^N – 1$ clock cycles required to convert a sample
- Integrator is sensitive to RC tolerances values and may cause drift in ADC output



Dual Slope ADC

- Resolves the issue of output drift of Single Slope ADC
- Initially, input signal is applied to integrator for a fixed time interval, t_1, resulting a ramp
- Then $-V_{ref}$ is applied to integrator and counter starts counting till time t_2 when integrator output becomes 0
- Output buffer is latched, and counter is reset for next conversion cycle
- Increasing binary counter clock signal frequency can increase the resolution of ADC

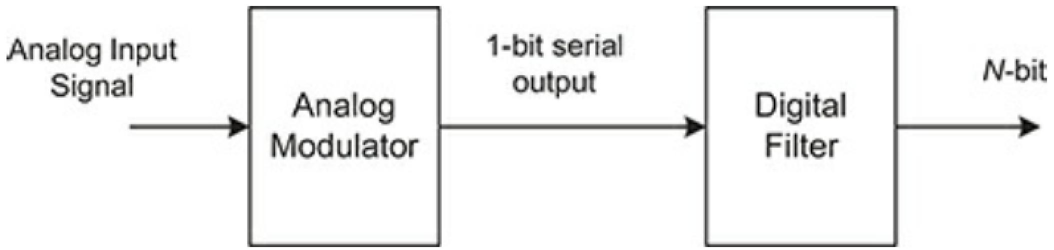


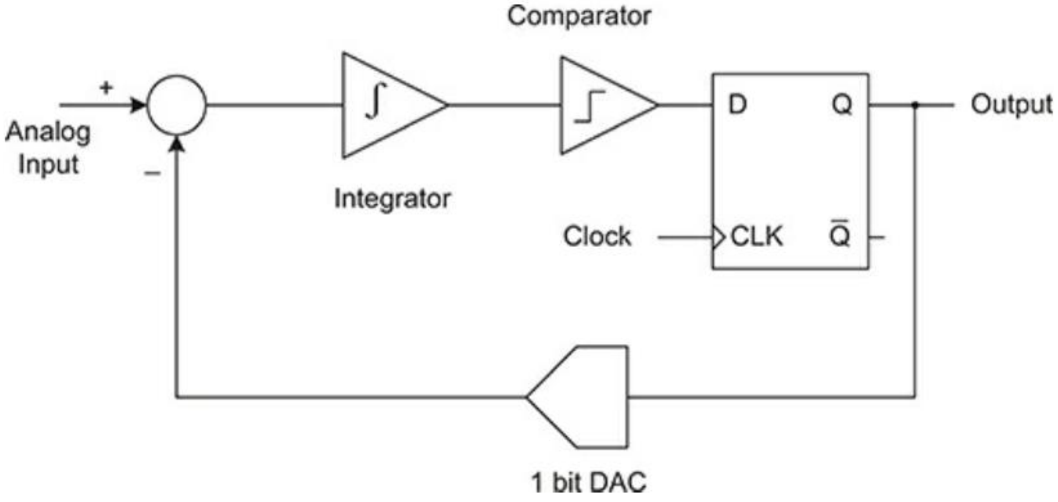


$$V_{in} = \frac{t_2}{t_1} \times V_{ref}$$

Sigma-Delta ADC

- Also called Delta-Sigma ADC, 1-bit ADC or Oversampling ADC
- Suitable for low bandwidth and high-resolution applications
- For ***1st Order Modulator***, difference between Input and 1-bit DAC is applied to integrator whose output is compared with a reference value
- Output of comparator is converted to1-bit serial data stream at a high frequency using D-type Flip Flop
- Flip Flop clock rate is selected K times higher than the actual sampling rate, where K is called ***Oversampling Ratio***
- Very efficient in reducing quantization noise i.e. better SQNR. Higher Order Modulators can further improve the SQNR value





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