Ishvik Kumar Singh

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EDUCATION

University of Illinois Urbana-Champaign **Jan 2025 - Present**
PhD in Electrical and Computer Engineering GPA: 4.0/4.0

Indian Institute of Technology Delhi **Jul 2018 - Jun 2022**
Bachelor of Technology in Electrical Engineering GPA: 9.015/10

RESEARCH INTERESTS

I have a broad interest in systems and computer architecture. I am currently exploring systems for machine learning, with a particular focus on prefill/decode disaggregation in LLM inference.

RESEARCH WORK

Rearchitecting Storage Stacks for Host Interconnect Bottlenecks **Jan 2025 - Present**
Guide: Prof. Saksham Agarwal (UIUC) & Prof. Rachit Agarwal (Cornell)

- Developed a contention-detection mechanism to detect host-interconnect bottlenecks, particularly memory-interconnect contention—resulting in throughput degradation and latency inflation.
- Rearchitected the Linux block layer to dynamically regulate in-flight I/O requests based on observed contention levels, achieving improved overall throughput and latency.

Fast and Safe I/O Memory Protection in Virtual Environments **Jan 2025 - Present**
Guide: Prof. Saksham Agarwal (UIUC), Prof. Rachit Agarwal (Cornell) & Prof. Tianyin Xu (UIUC)

- Analyzing I/O memory-protection overheads in virtualized environments targeting terabit-scale I/O devices.
- Redesigning virtualization stacks to provide high performance without compromising safety guarantees.

WORK EXPERIENCE

Intel Corporation **Jul 2022 - Dec 2024**
Pre-Silicon Validation Engineer, Network and Edge (NEX) Group Hyderabad, India

- Member of emulation team, responsible for building FPGA-friendly models and validation of SoC features.
- Developed and debugged PM and security validation scenarios in Sapphire Rapids & Granite Rapids projects.
  - Power Management (PM): Hardware-Controlled Performance States, CPU Idle state transitions.
  - Security: Software Guard Extensions (SGX), Multi-Key Total Memory Encryption (MKTME).
- Led the core validation activity in 12-core edge server (Bartlett Lake) project, taped-out on Intel 7 process.
  - Stress-tested CPU microarchitecture components using random instruction workloads.
  - Covered multi-core validation scenarios including coherency, memory ordering, etc.
- Developed signal-tracker modules for specific signal transitions and model-specific register (MSR) reads/writes.

TECHNICAL SKILLS

- **Programming Languages & HDLs:** C/C++, Python, Shell, Assembly (x86), Verilog
- **Tools & Technologies:** Linux Kernel, Make, perf, Intel PCM, CUDA, Nvidia Nsight (Nsys & Ncu), vLLM

RELEVANT COURSEWORK

UIUC: Modern Cloud Infrastructure, Storage Systems, Applied Parallel Computing, Computer Networks.
IIT Delhi: Computer Architecture, Operating Systems, AI and Machine Learning, Digital Image Processing, Introduction to VLSI Design, Applied Cryptography, Probability and Stochastic Processes, Signals and Systems.