Ishwar Singh Bhati

Research Scientist, Intel Labs, Bangalore, (December 2015 -)
PhD, University of Maryland, College Park (May, 2014)
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Education

PhD in Computer Engineering — Spring, 2014
University of Maryland, College Park, MD — GPA: 4.0/4.0
Advisor: Prof. Bruce Jacob (http://www.ece.umd.edu/~blj/)

B.Tech in Electronics and Communication Engineering — Spring, 2005
Indian Institute of Technology (IIT), Guwahati, India — GPA: 8.6/10

Areas of Interest

Computer Architecture, Machine Learning, Deep Learning Architecture, Memory Systems, Energy Efficient Architectures, Non-volatile Memory (PCM & SSD), High-Performance Computing, Distributed Systems

Technical Skills

Programming Languages: Verilog, VHDL, SystemC, C/C++, SystemVerilog, Perl, Linux/Unix based Shell Scripting (bash, tcsh), OpenMP, MPI
CAD Tools: Xilinx Synthesis Technology (ISE), Cadence Tools (Ncverilog, Simvision), Synopsis DesignWare Verification IP
Architectural Simulators: DRAMSim, MARSSx86 (PTLSim+QEMU), DiskSim

Research Summary

Emerging Architecture Research

- Working efficient compute and memory architecture for emerging applications like Deep Learning.

Micro-architecture Research

- NVM based LLC: Proposed novel techniques to mitigate long NVM write latency (featured in ISCA-2018)
- Memory aware reordered source (MARS): to reshape the memory traffic for efficient memory bandwidth (filed patent)
- Adaptive Width Aware Core (AWAC): we used simple heuristics to intelligently provision resources in the core dynamically (part of work featured in IEDM'2017)
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Graduate Research Assistant: University of Maryland, Department of ECE, College Park (Sep 2010 – May 2014)

My research focused on designing scalable and energy-efficient memory systems. As DRAM device gets bigger, we quantified and analyzed that the refresh operations pose a serious problem. To address refresh scalability, energy-efficiency and performance penalty, we proposed several practical methods to enable refresh reduction with available auto-refresh commands and coordinate the scheduling of refresh and low power modes to simultaneously improve energy and performance. These schemes require no or small changes in the DRAM device.

Scalable DRAM Refresh:

- Comprehensive evaluation and survey of DRAM refresh mechanisms, trade-offs, and penalties. We also clarify prevalent confusions with refresh options and timings available in JEDEC specified DDR devices. This study published in Transactions on Computers, 2015 (Weblink).
- Proposed simple modification in DRAM device to enable *refreshes reduction* with optimized auto-refresh commands rather than in-efficient row-level refresh commands. This work published in ISCA'15 (Weblink).

Energy Efficient Memory:

- Proposed novel techniques to simultaneously minimize two important types of DRAM energy components: *background and refresh*. Our novel schemes called "*Coordinated Refresh*" schedule refresh operations and power down modes in such a way that energy consumption is reduced while improving performance. This work accepted in ISLPED'13 for presentation (Weblink).

High Capacity Memory:

- Co-designed *parameterized simulation* infrastructure to study various emerging Non-volatile Memory (NVM) technologies, organization, and latencies. We simulated a range of workloads to understand performance tradeoffs when NVM used as part of the memory hierarchy. This study published in Intel Technology Journal (ITJ'13) (Weblink) as well as in a Tech report (Weblink).

Accurate Memory Simulations:

- Designed a set of techniques when applied in a full-system simulator gives *reliable, accurate and fewer variable* results. Our techniques implemented on MARSSx86 integrated with DRAMSim2 for case study to show reduce variability in simulations. This work published in a Tech report (Weblink).

Work Experience

Research Scientist, Intel Labs (Now in Parallel Computing Lab, PCL), Intel, Bangalore (December 2015 --)

- Focusing on Architectures for newer applications like Deep Learning

Senior Hardware Engineer, Oracle (formerly SUN Microsystem), Santa Clara (June 2014 – December 2015)

- Worked on performance modeling, projection and design space exploration of SPARC processors
- Responsible for modeling and maintaining memory-controller and database-accelerator modules
- Architectural explorations for future processors and debugging performance issues during bring-up

Research Assistant, Memory Systems Research Lab, Dept. of ECE, in University of Maryland (Sep 2010 – May 2014)

- DRAM low power modes and refresh mechanisms
- Novel applications of persistent memory
- Reliable full-system simulation infrastructure

Graduate Intern, Intel Corporation, Hillsboro, USA (June 2013 – August 2013)

- Quantified speed versus accuracy tradeoffs in memory modeling at several levels of abstraction (constant, analytical, queue-based, detailed etc.)
- Implemented and integrated a memory model, which is 10x faster than the cycle accurate DRAMSim2 and is within 10% of accuracy
- These models are targeted to obtain approximate timing and power behavior of a system early in its design phase
- Technical Mentor: Emily Shriver, Strategic CAD Labs (SCL)

Senior ASIC Engineer, LSI Corporation, India (Jan 2009 - July 2010)

- Co-implemented DDR2/3 *memory controller* and its PHY layer at 65nm process technology.
- Developed the crucial and challenging part of the optimized *DDR3 training sequence* and write leveling algorithm.
- Created *SystemVerilog and VMM* based automated test benches.

ASIC Design and Verification Engineer, Nevis Networks, India (July 2005 - June 2006, May 2007-Jan 2009)

- Involved in design and verification of DRAM Control module in a 96-core Network Processor Chip.
- Performed entire *FPGA prototyping* of memory controller using Xilinx's Vertex-4 based board and created synthesizable verification code.
- Led the SystemC modeling and Full-Chip Verification environment integration

Design Engineer, STMicroelectronics, India (June 2006 - May 2007)

- Responsible for modeling, *RTL, and verification* of a couple of modules in Wireless USB Medium Access Control (MAC) Chip design.

Summer Intern, Kyungpook National University (KNU), Daegu, South Korea (May 2004 - July 2004)

- Studied various *speech enhancements* and speech recognition techniques, and implemented Dynamic Time Warping (DTW) on TI-DSK 6711 using Simulink

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Graduate Class Projects

CMSC714 (High-Performance Computing):

- Accelerated scientific codes up to 20x times on 64 core distributed cluster, using OpenMP and MPI constructs.
- Implemented 4 parallel versions of an irregular graph algorithm (BFS) and compared their performance on real computer vision application

CMSC818B (Distributed File System):

- Designed in memory and client-server based file system from scratch by using FUSE calls.
- Developed database files systems using SQLite, added file/directory versioning.
- Implemented PAXOS and Authentication algorithms

Other Projects

- ENEE645 (Compiler Optimization): Implemented Loop Forward Propagation optimization in LLVM
- ENEE699 (Parallel Algorithms): Developed parallel versions of several graphs, sorting and tree algorithms
- ENEE644 (Computer Aided Design): Designed a CAD tool to manipulate and synthesize sequential circuits represented by Finite State Machines (FSM).

Publications

Ishwar Bhati, Udit Dhawan, Jayesh Gaur, Sreenivas Subramoney, and Hong Wang, "MARS: Memory Aware Reordered Source" arXiv:1808.03518, August 2018.

Kunal Korgaonkar, Ishwar Bhati, Huichu Liu, Jayesh Gaur, Sasikanth Manipatruni, Sreenivas Subramoney, Tanay Karnik, Steven Swanson, Ian A. Young, and Hong Wang, "Density Tradeoffs of Non-Volatile Memory as a Replacement for SRAM based Last Level Cache," *Proc. 45th International Symposium on Computer Architecture (ISCA 2018). Los Angeles, CA, June 2018.*

Kaushik Vaidyanathan, Daniel H Morris, Uygar E Avci, Ishwar S. Bhati, Lavanya Subramanian, Jayesh Gaur, Huichu Liu, Sreenivas Subramoney, Tanay Karnik, Hong Wang, and Ian A Young. "Overcoming interconnect scaling challenges using novel process and design solutions to improve both high-speed and low-power computing modes," *Electron Devices Meeting (IEDM), 2017 IEEE International*

Ishwar Bhati, Zeshan Chishti, Shih-Lien Lu, and Bruce Jacob, "Flexible auto-refresh: Enabling scalable and energy-efficient DRAM refresh reductions," *Proc. 42nd International Symposium on Computer Architecture (ISCA 2015)*. Portland, OR, June 2015.

Ishwar Bhati, Mu-Tien Chang, Zeshan Chishti, Shih-Lien Lu, and Bruce Jacob, "DRAM Refresh Mechanisms, Penalties, and Trade-Offs," *IEEE Transactions on Computers*, vol. 64, 2015.

Ishwar Bhati, Zeshan Chishti, and Bruce Jacob, "Coordinated refresh: Energy efficient techniques for DRAM refresh scheduling," *Proc. 2013 International Symposium on Low Power Electronics and Design (ISLPED 2013)*. Beijing China, September 2013.

Jim Stevens, Paul Tschirhart, Mu-Tien Chang, Ishwar Bhati, Peter Enns, James Greensky, Zeshan Chishti, Shih-Lien Lu, and Bruce Jacob, "An Integrated Simulation Infrastructure for the Entire Memory Hierarchy: Cache, DRAM, Nonvolatile Memory, and Disk," *Intel Technology Journal (ITJ)*, vol. 17, no. 1, 2013.

Patents

Ishwar Bhati and Zeshan Chishti, "Coordinating Power Mode Switching and Refresh Operations in a Memory Device," US patent granted, 2015

Ishwar Bhati, Zeshan Chishti, and Shih-Lien L. Lu, "Techniques to Reduce Memory Cell Refreshes for a Memory Device", US patent granted, 2016

Ishwar Bhati, Udit Dhawan, Jayesh Gaur and Sreenivas Subramoney, "Techniques to Reduce Memory Cell Refreshes for a Memory Device", US patent granted, 2018

Two other patents filed in the US PTO

Ph.D. Thesis

Ishwar Bhati, "Scalable and Energy-Efficient DRAM Refresh Techniques,"Ph.D. thesis, May 2014.

Technical Reports

B. Jacob, Ishwar Bhati, M.-T. Chang, P. Rosenfeld, J. Stevens, P. Tschirhart, Z. Chishti, S.-L. Lu, J. Ang, D. Resnick, and A. Rodrigues, "A Journaled, NAND-flash main-memory system," University of Maryland Systems and Computer Architecture Group Technical Report, 2014.

Mu-Tien Chang, Ishwar Bhati, Jim Stevens, Paul Tschirhart, Peter Enns, Daniel Gerzhoy, Zeshan Chishti, James Greensky, Shih-Lien Lu, and Bruce Jacob, "Producing Reliable Full-System Simulation Results: A Case Study of CMP with Very Large Caches," Institute for Systems Research (ISR) Technical Report UMD-ISR-TR-2012-07, 2012.

Relevant Graduate Courses

Computer Architecture (A+), Algorithms (A), Computer Aided Design (A), Compiler Optimizations (A+), High Performance Computing (A), Distributed File Systems (A), Distributed Systems (A+), Parallel Algorithms (A), CMOS VLSI Design (A), Exascale Computing (A)

Honors and Awards

- Jacob K. Goldhaber Travel award to attend LPDDR3 and DDR4 workshops organized by JEDEC, Sep 2012
- Merit Scholarship, granted to one student per year, ECE deptt., IIT Guwahati, August 2003

Activities

- Volley Ball Team, Inter-IIT (2002 - 2003)
- Student volunteer for SPIC MACAY and IIT Guwahati's Technical festival "Techniche".

Personal Information

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