EXAMINATION PAPER

FACULTY	**:**	**COMPUTER SCIENCE AND MULTIMEDIA**		
COURSE	**:**	**BACHELOR OF INFORMATION TECHNOLOGY (HONS)**		
YEAR/ SEMESTER	**:**	**FIRST YEAR / SEMESTER TWO**		
MODULE TITLE	**:**	**DIGITAL LOGIC**		
CODE	**:**	**BIT 126**		
DATE	**:**	**25 – SEPTEMBER, 2019, WEDNESDAY**		
TIME ALLOWED	**:**	**3 HOURS**		
START	**:**	**1:00 PM**	**FINISH**	**: 4:00 PM**

Instruction to candidates

1. This question paper has THREE (3) Sections.
2. Answer **ALL** questions in Section A, MCQ.
3. Answer **5** questions in Section B, MSAQ.
4. Answer **2** questions in Section C, MEQ.
5. No scripts or answer sheets are to be taken out of the Examination Hall.
6. For Section A, answer in the OMR form provided.

Do not open this question paper until instructed

(Candidates are required to give their answers in their own words as far as practicable)

SECTION A
Multiple Choice Questions
Attempt All Questions **[30×1=30]**

1. **Analog system is:**
   A. More immune to noise
   B. Continuous signals
   C. Discrete signals
   D. Both ‘A’ and ‘B’

2. **The output of an AND gate is HIGH when:**
   A. Any input is high
   B. All inputs are high
   C. No inputs are high
   D. Both ‘A’ and ‘B’

3. **The number of select inputs for 32x1 MUX is:**
   A. 4
   B. 5
   C. 16
   D. 6

4. **Which gate gives low output only when both inputs are high?**
   A. OR gate
   B. AND gate
   C. NAND gate
   D. NOR gate

5. **ASCII stands for:**
   A. Asian Standard code for Information Interchange
   B. American Standard code for Information Interchange
   C. American Standard code for Interchanging Information
   D. Armenian Standard code for Information Interchange

6. **On a K map, a grouping of 0’s produces:**
   A. A POS expressions
   B. A SOP expressions
   C. A don’t care conditions
   D. AND-OR logic

7. (r-1)'s complement of $(2B)_{16}$ is :

A. D4
B. D5
C. E4
D. E5

8. A BCD-to-7 segment decoder has 0100 on its input. The active outputs are:

A. a,c,f,g
B. b,c,f,g
C. b,c,e,f
D. b,d,e,g

9. Max terms are:

A. x+y+z
B. x'y'z'
C. Both 'A' and 'B'
D. None of the above

10. Which one of the following is NOT a valid rule of Boolean Algebra?

A. A+1=1
B. A+A'=0
C. A.A=A
D. A.A'=0

11. $(1111)_{gray} = (?)_2$

A. 1010
B. 1001
C. 1110
D. 1100

12. The output of X-NOR gate is:

A. A'B+AB'
B. A+B
C. (A'B).(AB')
D. AB+A'B'

13. How many cells are there in a 5-variable K-map?

A. 16
B. 5
C. 32
D. 8

14. The minimum number of NOR gates required to implement OR gate is:

A. 2
B. 4
C. 5
D. 6

15. The decimal equivalent of (A2F) 16 is:

A. 2608
B. 2600
C. 2607
D. 2601

16. Integrated circuit:

A. Is highly reliable
B. Needs limited power supply
C. Both ‘A’ and ‘B’
D. None of the above

17. Which of the following is self-complementing code?

A. 2421 code
B. 84-2-1 code
C. BCD
D. Both ‘A’ and ‘B’

18. A ROM is a:

A. Combinational circuit
B. Sequential circuit
C. Both ‘A’ and ‘B’
D. None of the above

19. The output of 3-to-8 decoder is:

A. 3*8
B. 3
C. 3+8
D. 8

20. Register is a type of:

A. Combinational circuit
B. Sequential circuit
C. CPU
D. Latches

21. SSI stands for:

A. Small Scale Inverter
B. Small Service Implementation
C. Small Scale Integration
D. Small Service Integration

22. The number of cells or square for the output of K map in 3 bit parity generator circuit is:

A. 4
B. 16
C. 32
D. 8

23. Multiplexer has:

A. One data input, several data outputs and selection inputs
B. One data input, one data outputs and one selection input
C. Several data inputs, several data outputs and selection inputs
D. Several data inputs, one data output and selection inputs

24. EBCDIC has _____characters.

A. 128
B. 127
C. 256
D. 255

25. Which is the correct order of sequence for representing the input values in K-map?

A. 00,01,10,11
B. 00,01,11,10
C. 00,11,01,11
D. None of the above

26. Gray code is also known as:

A. Reflected code
B. Cyclic code
C. Self-complementing code
D. Both ‘A’ and ‘B’

27. B+B’ equals to:

A. 1
B. 0
C. B
D. B’

28. Half adder requires two binary:

A. Inputs
B. Outputs
C. Digits
D. Both ‘A’ and ‘B’

29. The characteristics equation of D flip flop implies that :

A. The next state is dependent of previous state
B. The next state is dependent of present state
C. The next state is independent of previous state
D. The next state is independent of present state

30. What is the bit storage binary information capacity of any flip flop?

A. 1 bit
B. 2 bits
C. 16 bits
D. None of the above

SECTION B

Short Answers Questions

Answer any five (5) questions out of eight (8) questions [5×6=30]

1. Define PLA. Implement $F_1(A,B,C)=\sum(3,5,6,7)$ and $F_2(A,B,C)=\sum(0,2,4,7)$ using PLA. [1+5]

2. Discuss about Registers and Counters. Explain any two of the counters. [2+2+2]

3. Define clock pulse. Differentiate between flip flop and latch. [1+5]

4. Why is NAND & NOR gates called Universal gates? Implement AND, OR and NOR Gates using NAND gates only. [4×1.5]

5. Discuss the different Types of ROM. Also Implement $F_1(A,B)=\sum(1,2,3)$ and $F_2(A,B)=\sum(0,2)$ using ROM. [3+3]

6. Define Magnitude Comparator. Explain about the BCD Adder in detail. [2+4]

7. Write short notes on: [3+3]
- **A.** Integrated Circuit
- **B.** IC Digital logic families

8. Difference between :[3+3]
- **A.** ROM and PLA
- **B.** SOP and POS

SECTION C

Long Answer Questions

Attempt any two (2) questions out of three (3) questions [2×20=40]

1.

A. Explain about EBCDIC. Perform subtraction of following decimal numbers in BCD using 10's complement: [3+7]

i. 2321-8301

B. Explain with an example about don't care conditions.
Simplify F(A,B,C,D)=∑(0,6,8,13,14) & d(A,B,C,D)=∑(2,4,10) in SOP and POS form. [2+8]

2.

A. Implement F= xy+x'y'+yz' using NOT and OR gates only. Find the complement of F=x+y'z, Also prove F.F'= 0 and F+F'= 1. [5+5]

B. Explain about Full subtractor in brief. Construct a full adder using two half Adders. Also verify your answer. [3+7]

3.

A. Define Magnitude Comparator. Introduce a 1-bit magnitude comparator in short. Draw a logic circuit for 4-bit magnitude comparator. [1+3+6]

B. Design a circuit that converts BCD to excess-3 code. [10]

******BEST OF LUCK******