





# Isidor Kaplan

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## Education

**Bachelor of Applied Science**, Computer Engineering | University of Toronto

- **4.0/4.0 cGPA / 96.1%** Cumulative Average (3 years) **2019 - 2024**

## Professional Experience

**FPGA Fabric Architect Intern** | Intel

**May 2022 - August 2023**

- FPGA Fabric Architecture PEY Intern with Intel PSG

**Teaching Assistant** | University of Toronto

**Sept 2021 - May 2022**

- **ECE243 Computer Organization**: Introduce processor design in Verilog and assembly programming in ARM A9 Assembly.
- **ECE244 Programming Fundamentals**: Introduce OOP, Data Structures, Computational Complexity, and the C++ Programming Language.

**Software Developer Intern** | Rocscience Inc

**Summer 2021**

- Reimplemented CPillar: MFC C++ commercial software for stability analysis.
- Surveyed state of the art Unsupervised Machine Learning Image Segmentation.

**Academic Researcher** | iQua Research Group

**Summer 2020**

- Applied deep reinforcement learning to networking problems, such as congestion control, edge computing and network-adaptive coding.

## Publications

- **Ivory: Learning Network Adaptive Streaming Codes**  
Salma Emara, Fei Wang, *Isidor Kaplan*, Baochun Li. **IWQoS 2022**
- **Hybrid Algorithm Based on Machine Learning and Deep Learning to Identify Ceramic Insulators and Detect Physical Damages**,  
Youssef El Haj, Ruth Milman, *Isidor Kaplan*, Ali Ashasi. **CEIDP 2021**

## Engineering Projects

See all projects at: <https://www.linkedin.com/in/isidorjkaplan/details/projects/>

**CPillar** | Rocscience Inc

- Refactored CPillar from the ground-up in C++ / MFC allowing for first major update in years.
- Update Notes (5.005): <https://www.rocscience.com/support/cpillar/release-notes>

**Deep Reinforcement Learning Framework** | iQua Research Group

- Designed PyTorch DRL framework used for research papers at iQua Research Group
- Project GitHub: <https://github.com/isidorjkaplan/DRL>

**Processor Design Project** | Project

- Designed System-Verilog 16-bit, 8-register, interrupt-enabled and pipelined processors.
- Version 1: <https://github.com/isidorjkaplan/ProcessorPublic>
- Version 2: <https://github.com/isidorjkaplan/PipelinedProcessor>

**Realtime Online-Learning Deep Video Compression** | Project

- Designed video compression scheme that learns in real-time with ~23x compression
- Project GitHub: <https://github.com/isidorjkaplan/OVAL>

**Mapper Project** | Project

- Implemented large-scale Google-maps inspired program in C++
- Project GitHub: <https://github.com/isidorjkaplan/MapperPublic>

## Awards

Edward S. Rogers Sr.  
Department of Electrical  
and Computer Engineering  
Top Student Award (**2021**)

BFMI Sesquicentennial  
Trust Scholarship (**2021**)

Deans List (**2019-2021**)

In-Course  
Scholarship (**2020**)

First-Year Fellowship (**2020**)

## Technical Skills

### Technical Tools

- C / C++
- Python
- Rust
- Java
- ARM Assembly
- System Verilog / RTL
- Quartus / ModelSim
- MATLAB

### Industry Knowledge

- Operating Systems
- Reinforcement Learning
- Computer Vision
- Software Design
- Embedded Systems
- FPGA System Design