Isidor Kaplan

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About Me

Computer engineer specializing in FPGA design, low-latency trading systems, and high-performance C++ software. Currently an FPGA Engineer at Headlands Technologies, with prior experience at Hudson River Trading and Intel developing production-grade hardware and software. Experienced in full-lifecycle FPGA and embedded systems design, with award-winning academic performance and top recognition in Computer Engineering at the University of Toronto.

Experience

Headlands Technologies June 2024 – Present
FPGA Engineer *Chicago, IL*

- Engineered low-latency trading infrastructure, improving stability, scalability, and system performance
- Full-lifecycle FPGA design: specification, implementation, testing, verification, and deployment
- Developed high-performance software drivers and testing/verification frameworks for trading applications

Hudson River Trading June 2023 – August 2023
Software Engineer (Intern) *New York, NY*

- Design modern C++ multi-threaded, high-performance, networked, timing-accurate market-simulation tools
- Extend proprietary C++ exception-handling framework with improved stack-tracing capabilities

Intel May 2022 – May 2023
FPGA Engineer (Intern) *Toronto, ON*

- Optimized next-generation FPGA routing architecture improving simulations results in VPR and Quartus
- Developed high-performance C++ graph tools to operate on FPGA routing architecture representations
- Developed Python tool for automated complex data visualization, reducing analysis time for experiments

University Of Toronto Sept 2021 – April 2024
Teaching Assistant *Toronto, ON*

- TA for *Operating Systems*, *Computer Organization*, *Programming Fundamentals*, and *Software Comm & Design*, covering concurrency, memory, CPU design, Verilog, embedded programming, C++, and data structures.

Rocscience May 2021 – August 2021
Software Engineer (Intern) *Toronto, ON*

- Redesigned CPillar, a $995/license C++ geological analysis software, enabling the first major update in years

University Of Toronto – iQua Research Group May 2020 – August 2020
ML/AI Researcher (Intern) *Toronto, ON*

- Developed advanced reinforcement learning models using PyTorch, applied to congestion control, edge computing, and network-adaptive coding, resulting in the publication of two conference research papers

Education

University Of Toronto Sept 2019 – June 2024
B.A.Sc in Computer Engineering *Toronto, ON*

- Obtained *4.0/4.0* Cumulative GPA and *95.3%* Cumulative Average
- Awarded the *Adel S. Sedra Gold Medal* for highest grades in Computer Engineering, Class of 2024
- Awarded Annual *Top Student Award* from Dept of Electrical and Computer Engineering (2020-21 and 2021-22)
- Awarded Charles Edwin Trim (2022), BFMI Sesquicentennial Trust (2021), and In-Course (2020) *Scholarships*

Technical Skills

Languages & Tools: System Verilog, Modern C++, C, Python, Vivado, Quartus, Java, Assembly
Systems & Concepts: Low-latency, concurrency, FPGA design, CPU design, embedded programming
Algorithms & Math: Data structures, linear algebra, probability, control theory, multivariate calculus, ML/AI

Publications

Multi-Agent Deep Reinforcement Learning for Cooperative Edge Caching *IEEE ICC-SAC 2023*
Ivory: Learning Network Adaptive Streaming Codes *IEEE IWQoS 2022*
Deep Learning to Identify Ceramic Insulators and Detect Physical Damages *IEEE CEIDP 2021*