Isidor Kaplan

isidor.kaplan@utoronto.ca
linkedin.com/in/isidorjkaplan
github.com/isidorjkaplan
isidorkaplan.ca/transcript.pdf

Education

Bachelor of Applied Science, Computer Engineering | University of Toronto ***2019 - 2024***

- **4.0/4.0** Cumulative GPA / **96.1%** Cumulative Average / Ranking #1 (2021-21, 2021-22)

Professional Experience

FPGA Fabric Architect Intern | **Intel Corporation** ***May 2022 - Present***

- Design and research next-generation routing architecture for Intel high-performance FPGAs

Teaching Assistant | **University of Toronto** ***Sept 2021 - April 2022***

- **ECE243** *Computer Organization*: Introduce processor design in Verilog and assembly programming in ARM A9 Assembly.
- **ECE244** *Programming Fundamentals*: Introduce OOP, Data Structures, Computational Complexity, and the C++ Programming Language.

Software Developer Intern | **Rocscience Inc** ***May 2021 - August 2021***

- Reimplemented a Major legacy C++ commercial software for stability analysis from scratch.
- Surveyed state of the art Unsupervised Machine Learning Image Segmentation.

Academic Researcher | **iQua Research Group** ***May 2020 - August 2020***

- Applied deep reinforcement learning to networking problems, such as congestion control, edge computing and network-adaptive coding.

Engineering Projects

See all projects at: https://www.linkedin.com/in/isidorjkaplan/details/projects/

Processor Design Project | **Project**

- Designed System-Verilog 16-bit, 8-register, interrupt-enabled and pipelined processors.

Version 1: https://github.com/isidorjkaplan/ProcessorPublic

Version 2: https://github.com/isidorjkaplan/PipelinedProcessor

CPillar | **Rocscience Inc**

- Refactored CPillar from the ground-up in C++ / MFC allowing for first major update in years.

Update Notes (5.005): https://www.rocscience.com/support/cpillar/release-notes

Deep Reinforcement Learning Framework | **iQua Research Group**

- Designed PyTorch DRL framework used for research papers at iQua Research Group

Project GitHub: https://github.com/isidorjkaplan/DRL

Realtime Online-Learning Deep Video Compression | **Project**

- Designed video compression scheme that learns in real-time with ~23x compression

Project GitHub: https://github.com/isidorjkaplan/OVAL

Map Project | **Project**

- Implemented large-scale Google-maps inspired UI / backend program in C++
- Developed simulated-annealing based heuristics for NP-C graphing problems.

Publications

- **Ivory: Learning Network Adaptive Streaming Codes**
  Salma Emara, Fei Wang, *Isidor Kaplan*, Baochun Li. **IWQoS 2022**
- **Hybrid Algorithm Based on Machine Learning and Deep Learning to Identify Ceramic Insulators and Detect Physical Damages**,
  Youssef El Haj, Ruth Milman, *Isidor Kaplan*, Ali Ashasi. **CEIDP 2021**

Awards

Edward S. Rogers Sr. Department of Electrical and Computer Engineering *Top Student Award* (**2020-21**, **2021-22**)

Charles Edwin Trim *Scholarship* (**2022**)

BFMI Sesquicentennial Trust *Scholarship* (**2021**)

In-Course *Scholarship* (**2020**)

First-Year *Fellowship* (**2020**)

Deans List (**2019 - Present**)

Technical Skills

Technical Tools

- C / C++
- Python
- Rust
- Java
- ARM Assembly
- System Verilog / RTL
- Quartus / ModelSim
- MATLAB

Industry Knowledge

- Operating Systems
- Reinforcement Learning
- Computer Vision
- Software Design
- Embedded Systems
- FPGA System Design