Question-1:

Our input bit number is 8.

Now for the first bit addition we only need only one half-adder circuit. as there is no carry on the 1st bit addition.

2 bit adition gate calculations: (Half-Adder)

let, a_0, b_0 be our input bit.

Then, Let, S_1 be the sum bit and

C_1 be the carry bit.

So,

$$S_1 = a_0 \oplus b_0 \quad \text{and}$$

$$C_1 = a_0 b_0.$$

i.e. $S_1 = a_0 b_0' + a_0' b_0.$

and $C_1 = a_0 b_0$

For S_1 we need # AND GATE = 2
OR " = 1
NOT " = 2

C_1 we need # AND GATE = 1

So, for a half adder we need

2 NOT GATE
3 AND GATE
1 OR GATE.

2 bit addition with carry bit gate Calculations:-

let, a_1, b_1 two input bit and C_1 be the carry bit. Then,

$$S_2 = a_1 \oplus b_1 \oplus C_1 = a_1 b_1' C_1 + a_1' b_1 C_1' + a_1' b_1' C_1 + a_1 b_1 C_1$$

and $$C_2 = a_1 b_1 + a_1 C_1 + b_1 C_1$$

AND GATE = 8 + 3 = 11
OR " = 3 + 2 = 5
NOT " = 3

So, for one full adder we need 11 AND GATE and 5 OR GATE.

Now, for 8 bit addition we need one half-adder and 7 full adder.

Hence,

Total # AND GATE = $3 \times 1 + 7 \times 11 = 80$
" # OR " = $1 \times 1 + 7 \times 5 = 36$
" # NOT " = $2 \times 1 + 7 \times 3 = 22$

(Ans)

Now for substraction:

We know that, in 2's compliment

$$\bar{B} + 1 = -B.$$

Therefore, $A - B = A + \bar{B} + 1$

Therfore, substraction of A and B is nothing but the addition with intial carry 1.

To perform substraction for 8 bit number we need 8 full adder and for calculation $\overline{B}$ we need 8 NOT GATE.

So, in total. #AND GATE = 8 X 11 = 88
#OR " = 8X 5 = 40
#NOT " = 8X 3 + 8 = 32

(Ans)

- The above gate count is for sequential logic circuit.

Question-2:

We have 8 bit input.

In CLA there are two function generate (G) and propagate (P) function.

For the i-th bit.

$$g_i = A_i B_i$$
$$P_i = A_i \oplus B_i$$

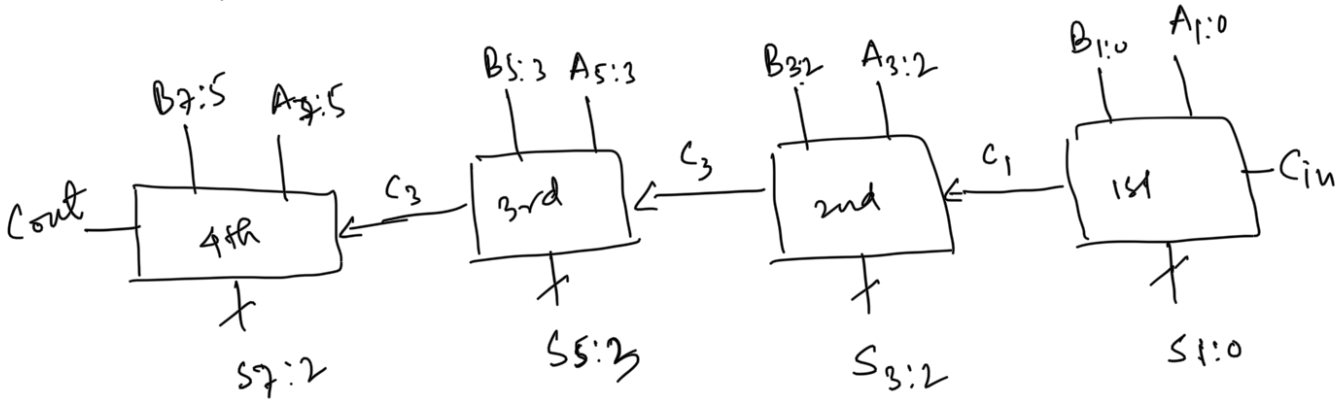
and $C_i = A_i B_i + (A_i + B_i) C_{i-1}$
$= g_i + P_i C_{i-1}$.

Now for 8 bit input we devide the block of size 2.

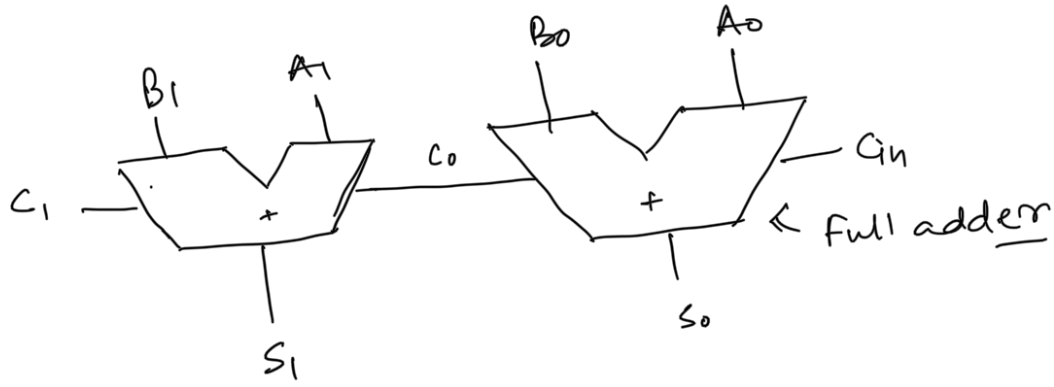
block of 2 bits.

So, there will be 4 blocks.

Now for one block.



1st block



This is for the sumbit calculation

Now

$$C_0 = g_0 + P_0 \cdot C_{in}.$$

$$C_1 = g_1 + P_1 \cdot C_0$$

$$= g_1 + P_1 \cdot (g_0 + P_1 \cdot C_{in})$$

$$= (g_1 + P_1 \cdot g_0) + P_0 P_1 \cdot C_{in}.$$

$$= G_{1:0} + P_{1:0} C_{in}.$$

In the first block the,

$$C_1 = G_{1:0} + P_{1:0} C_{in}.$$

where,

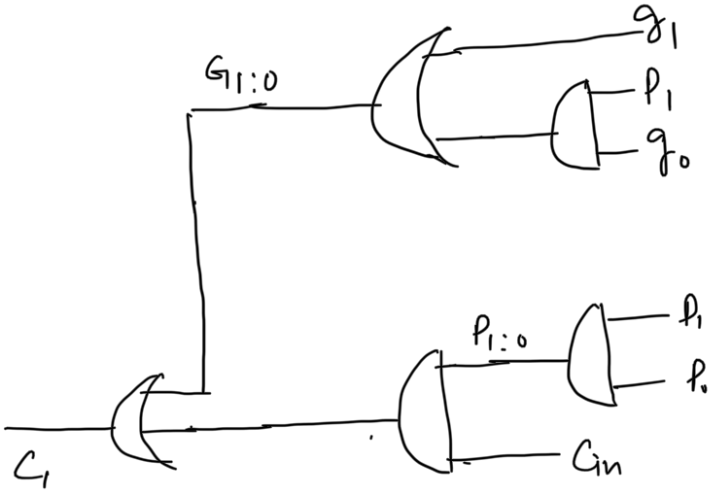
$$G_{1:0} = g_1 + P_1 \cdot g_0$$

$$P_{1:0} = P_1 P_0$$

where, $g_i = A_i B_i$, $P_i = A_i \oplus B_i$

If we know A_i, B_i then we can easily calculate $G_{1:0}$ and $P_{1:0}$ and from these two we can find Cout

So, for the first block the carry bit circuit is



So, for each block:

For sum bit calculation we need two full adder,

and one block carry finding circuit.

So, Total # AND GATE = $11 \times 2 + 3 = 25$
OR GATE = $5 \times 2 + 2 = 12$
NOT GATE = $3 \times 2 = 6$

So, total.

AND := $25 \times 4 = 100$
OR := $12 \times 4 = 48$
NOT := $6 \times 4 = 24$

Comparisom:

In the question one. we use only the sequential adder circuit. and its takes $O(n)$ time.

Here. it only need $O(\sqrt{n})$ times. as we calculate the sum bit and carry bit for each block parallad.

Though the 2nd case we need more gates in counts but it is faster enough.

Question. 3: