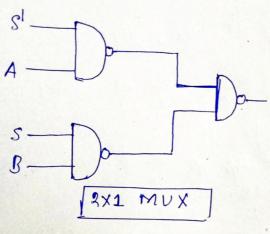
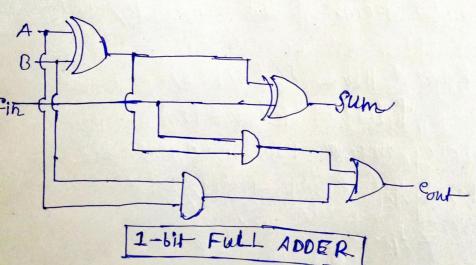
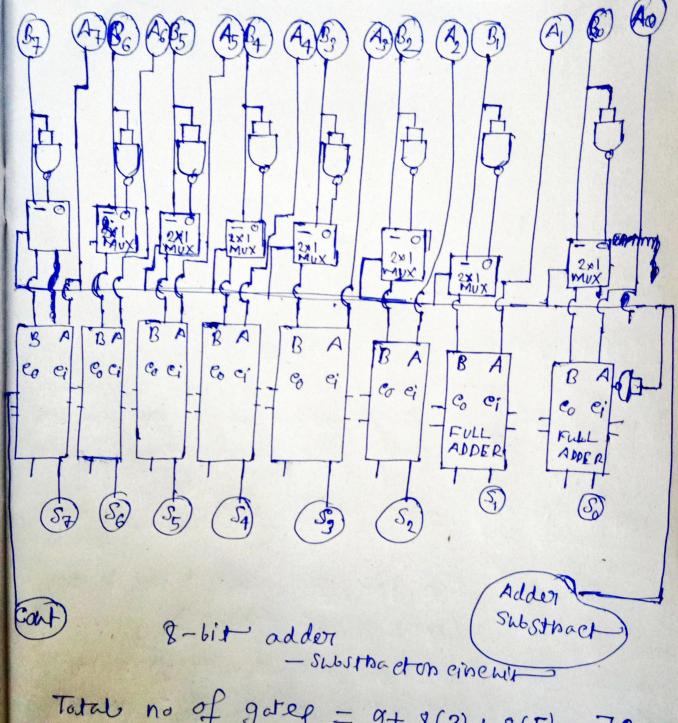
Design an adder substractors & bit cinquit win any 2-input gates, and count the number of gates required of the delay of the cinquit.

> we first draw the bagic circuit of then the fall circuit.





Number of gates in a 2×1 Multiploper = 3 Number of gates in a 1-bit Forther FULL-ADDER = 5.



Total no of gates = 9+8(3)+8(5) = 73.