Question:-

Design an adder - substractor 8 bit circuit using any 2-input gates and count the number of gates required and the delay of the circuit

Ans:- Our input bit number is 8
Now for 1st bit addition we only need only one half adder circuit as there is no carry on the 1st bit addition.

2-bit addition gate calculation: (Half adder)

Let a_0, b_0 be our input bit, Then let S_1 be the sum bit and C_1 be the carry bit.

So, $S_1 = a_0 \oplus b_0$ and $C_1 = a_0 b_0$

i.e, $S_1 = a_0 b_0' + a_0' b_0$ & $C_1 = a_0 b_0$

So for S_1 we need 2 AND GATE
1 OR GATE
and 2 NOT GATE

for C_1 we need 1 AND gate.

So for a half adder we need 2 NOT gate.
3 AND gate.
1 or gate.

2 bit addition with carry bit gate calculation:-

Let, a_1, b_1 be two input bit and C_1 be the carry bit then

$S_2 = a_1 \oplus b_1 \oplus C_1 = a_1 b_1' C_1' + a_1' b_1 C_1' + a_1' b_1' C_1 + a_1 b_1 C_1$

and $C_2 = a_1 b_1 + a_1 C_1 + b_1 C_1$

So required number of AND gate = 11
OR gate = 5
NOT gate = 3

So, for one full adder we need 11 AND gate & 5 OR gate.

Now for 8 bit addition we need one half adder and 7 full adder. There fore total number of

AND gate = $3 \times 1 + 7 \times 11 = 80$
OR gate = $1 \times 1 + 7 \times 5 = 36$
NOT gate = $2 \times 1 + 7 \times 3 = 22$

Now for substruction, we know that, in 2's Complement $\bar{B} + 1 = -B$ So, $A - B = A + \bar{B} + 1$
Therefore, substruction of A & B is nothing the addition with initial Carry 1

To perform Substruction for 8 bit number. We need 8 full adder and for calculating $\bar{B}$ we need 8 more NOT gate.

So Total Number of required gate is

AND gate is = $8 \times 11 = 88$
OR gate is = $8 \times 5 = 40$
NOT gate is = $8 \times 3 + 8 = 32$

This is the gate calculation for Sequential logic Circuit.

For using Carry look Ahead Adder (CLA) there are two function one is generateing function (G) and another is probagatting function (P)

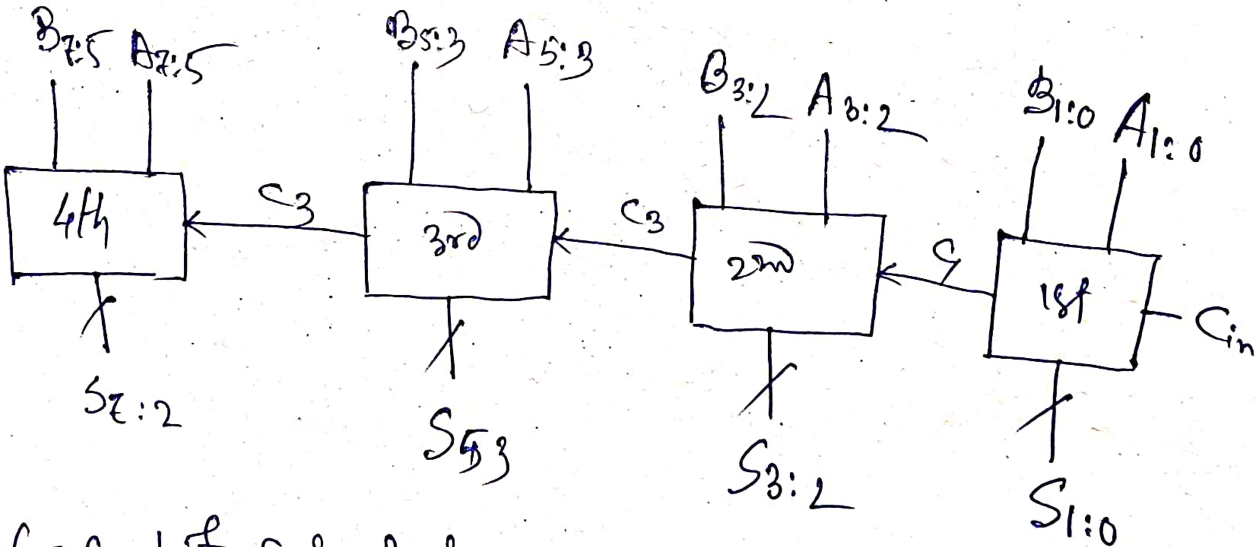
For i^{th} bit $g_i = A_i B_i$

$P_i = A_i \oplus B_i$

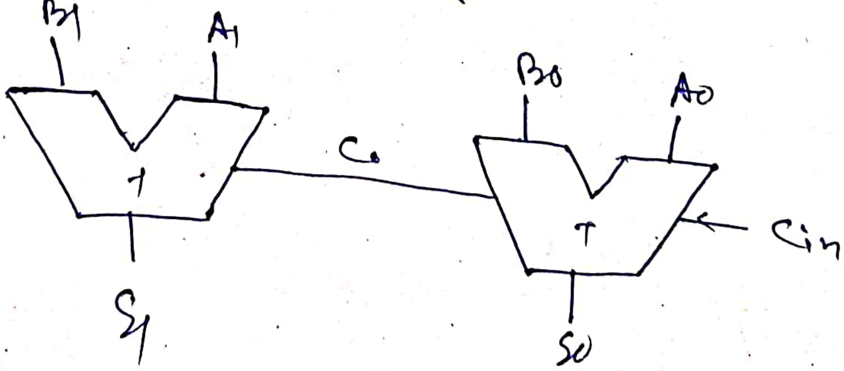
and $C_i = A_i B_i + (A_i + B_i) C_{i-1} = g_i + P_i C_{i-1}$

So for 8 bit input we ~~define~~ devide the block of size 2.

No for one block



1st Block for sum bit calculation.



Now $C_0 = g_0 + P_0 \cdot C_{in}$

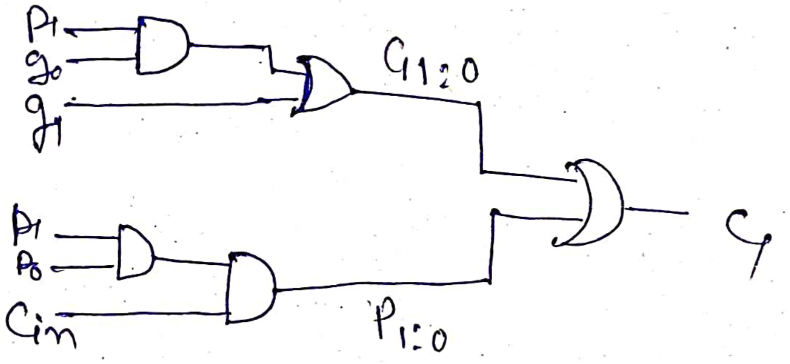
$C_1 = g_1 + P_1 \cdot C_0 = g_1 + P_1(g_0 + P_1 C_{in})$

$= (g_1 + P_1 g_0) + P_0 P_1 C_{in}$

$= G_{1:0} + P_{1:0} C_{in}$

where $g_i = A_i B_i$, $P_i = A_i \oplus B_i$

If we know A_i, B_i then we can easyly calculate $G_{1:0}$ and $P_{1:0}$ and from these two we can find Cout
So, for the 1st block the carry bit the circuit is:



~~So for each sum bit calculation we need two full adder and one block~~

So Total number of Gate counts required for each block is

AND Gate = 11×2+3 = 25
OR Gate = 5×2+2 = 12
NOT Gate = 3×2 = 6

So Total number is

AND Gate = 25×4 = 100
OR Gate = 12×4 = 48
NOT Gate = 6×4 = 25

Comparison :-

So far using sequential adder circuit ~~at~~ it takes $O(n)$ times.

But for the 2^{nd} part we need only $O(\sqrt{n})$ times as we calculate this sum bit and carry bit for each block parallel.

Although the 2^{nd} part we need more gates in counts but it is faster enough.