Digital Systems Design with FPGAs: Lab-1

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***Abstract*— Lab 1 consist of varies modules working on the FPGA and programing it in Verilog Systems,**

I. Introduction

It Is an Introduction to Verilog and Digital Logics with FPGA. This paper will put light on five different projects which are described as below.

II. Ease of Use

All of the Five projects consist of Screenshots of the wave formation in simulation and the video recording of them running on the Board DE1_SoE. The details are as below.

1.3 Mux4_1 Circuit

The Mux4_1 consist of 4 inputs, 1 output and 2 select lines. We construct Mux4_1 by using three Mux2_1. Which further consist of only 2 inputs, 1 output and one select line. The select line will help us to decide which input will goes to output.

In Mux4_1, the 4 inputs are 01, 01, 10 and 11. Output is Out and Select lines are sel0 and sel1. Sel0 holds the input of first two Mux2_1 and Sel1 holds the output of first two mux's output as an input to the third Mux.

The Representation of the Mux's, Input and Output is represented as below.

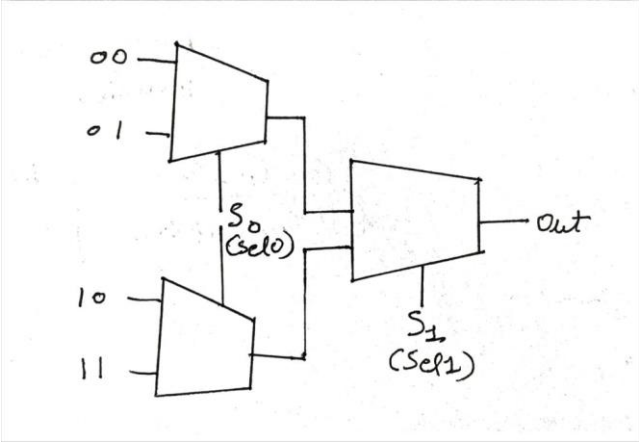


Fig: Mux4_1 from Mux2_1

The waveform of the Mux's Inputs and Output are Simulated on Model Sim as below.

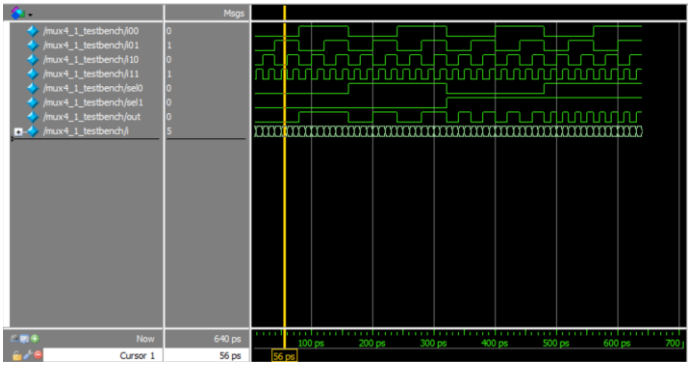


Fig: Mux4_1 Waveform

2.1 Multi-Digit Recognizer

In This Lab, I was assigned to show the last 2 digits of my student ID, which is 41.

The Switch on the DE1_SoC are used to bring the 41. Switch 7 to 4 are used to bring the combination of 4 and Switch 3 to 0 are used to bring the combination of 1. Once we have the switched aligned like this: 0100 0001. The output will turn high. And it only turn high when the switches are aligned like the above, And gate is used to get the desired output.

The waveform of Multi- Digit recognizer are Simulated on Model Sim as below.

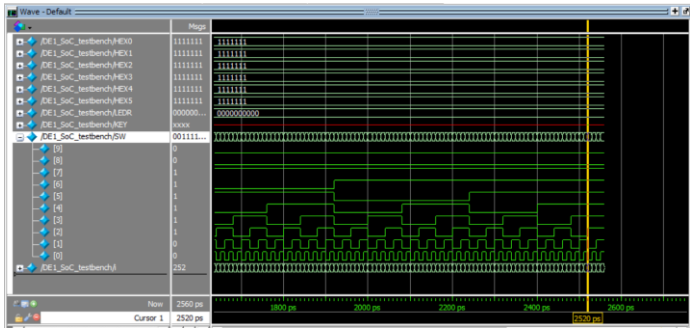


Fig: Multi-Digit Recognizer

The Video of the program on DE1_SoC is separately attached in the folder Lab1- 2.1

2.2 Multi- Level Logic

Here, I was provided with the Six Items with unique UPC codes. The UPC codes assigned to distinguish either the Item is discounted or Expensive. The Table of Items is as below:

Item Name	UPC Code	Discounted?	Expensive?
Shoes	0 0 0	No	Yes
Costume Jewelry	0 0 1	No	No
Christmas Ornament	0 1 1	Yes	No
Business Suit	1 0 0	No	Yes
Winter Coat	1 0 1	Yes	Yes
Socks	1 1 0	Yes	No

Table: Provided UPC code

The waveform of the UPC code after Simulated on Model Sim is below:

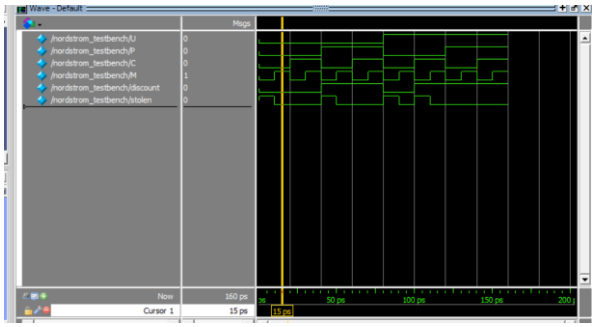
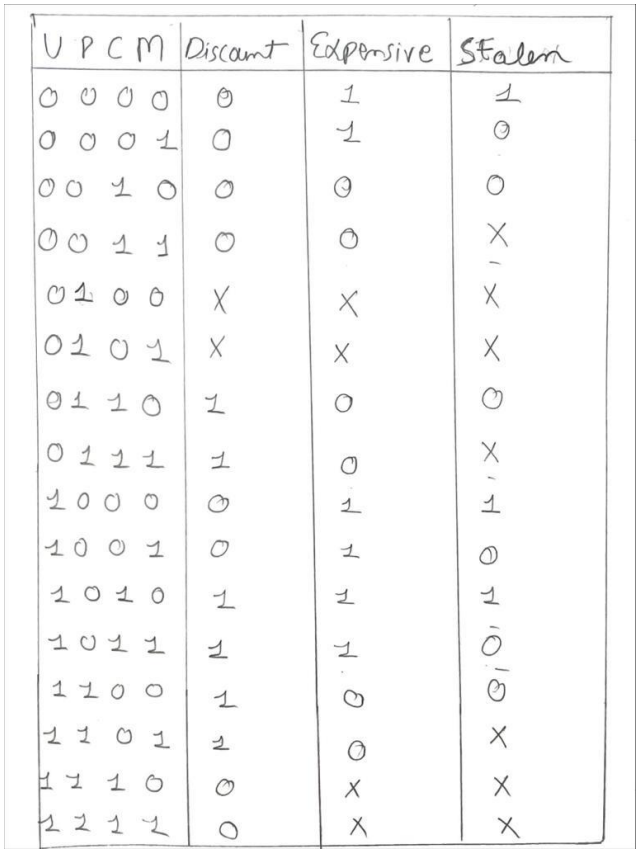


Fig: UPC Wave Form



U	P	C	M	Discount	Expensive	Stolen
0	0	0	0	0	1	1
0	0	0	1	0	1	0
0	0	1	0	0	0	0
0	0	1	1	0	0	X
0	1	0	0	X	X	X
0	1	0	1	X	X	X
0	1	1	0	1	0	0
0	1	1	1	1	0	X
1	0	0	0	0	1	1
1	0	0	1	0	1	0
1	0	1	0	1	1	1
1	0	1	1	1	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	X
1	1	1	0	0	X	X
1	1	1	1	0	X	X

Table: Truth Table of UPC code

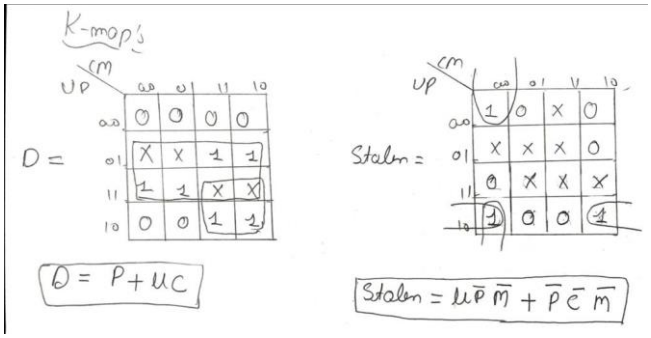


Fig: K-Map of Discount and Stolen

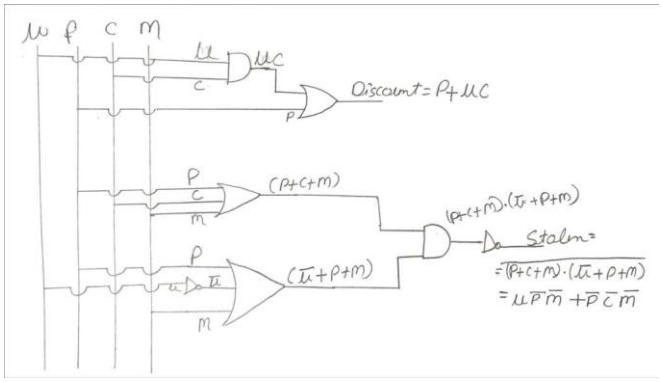


Fig: Circuit Diagram of Discount and Stolen

The Video of the program on DE1_SoC is separately attached in the folder Lab1- 2.2

3.1 High Level Verilog- Seven Segment Display

Here in this project we need to show the number goes from 0 to 9 when we operate switch SW3 to SW0 on HEX0 and again from 0 to 9 when we operate switch from SW7 to SW4 on HEX1.

The waveform of the Seven Segment Display code after Simulated on Model Sim is divided into 3 screenshots. 1st is the overview, 2nd is the Input waves and 3rd is the output below:

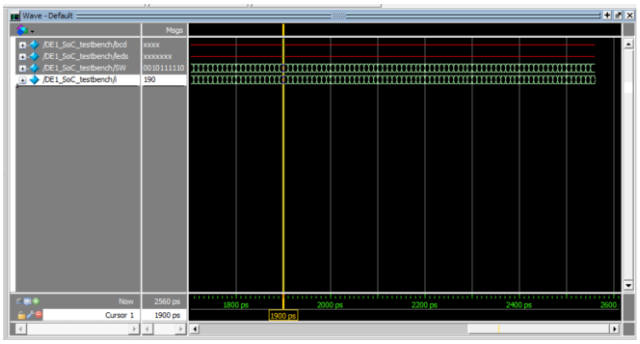


Fig: Seven Segment Display

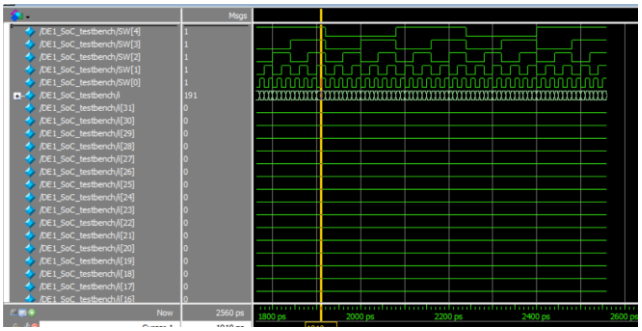


Fig: Input (Switch) Wave form

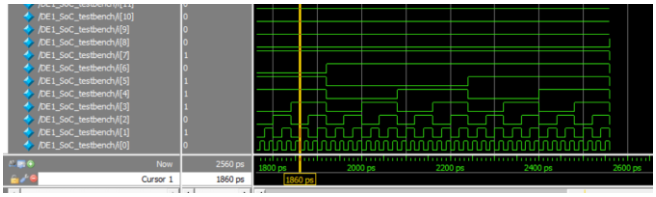


Fig: Output wave form

The Video of the program on DE1_SoC is separately attached in the folder Lab1- 3.1.

3.2 UPC Code to Display on Seven Segment

In this project, we have designed our own UPC item table to display the name on Seven Segment display. It also includes the Discount and Expensive lights. Discount is linked to LEDR0 and Expensive is linked to LEDR1.

The table of the Items is:

U	P	C	Output	Discount	Expensive
0	0	0	Phone	No	Yes
0	0	1	Apple	No	No
0	1	1	Chips	Yes	No
1	0	0	Pencil	No	Yes
1	0	1	COCOA	Yes	Yes
1	1	0	COFFEE	Yes	No

Table: Developed UPC Code table

The waveform of the UPC code after Simulated on Model Sim is below, this is the general waveform. However, in depth waveforms are provided in the media folder of this project.

Fig: UPC waveform

The Video of the program on DE1_SoC is separately attached in the folder Lab1- 3.2.