Gate Oxide Yield Improvement for 0.18µm Power Semiconductor Devices with Deep Trenches

DP: Discrete and Power Devices

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***Abstract*— Two unique gate oxide failure mechanisms are associated with deep trench processes for a 0.18 µm power semiconductor device. One failure mode is a "mini-LOCOS" defect, that is due to inadvertent oxidation of Si in the active area during deep trench oxidation. The other failure mode is due to slip associated with dislocations from the deep trenches. These defects are eliminated by optimizing the SiN oxidation barrier used during deep trench oxidation and by optimizing high temperature anneals to minimize dislocation generation.**

Keywords— Yield, gate oxide, dislocation, power semiconductor, deep trench

I. Introduction

Power semiconductor devices are used in a wide variety of products, including mobile devices and automobiles. A common high voltage device is a Double-diffused Metal-Oxide-Semiconductor (DMOS) transistor) [1,2]. The DMOS device provides low transient losses and is therefore suitable for high-frequency systems (which require high efficiency). A key part of high voltage technology are the deep trenches used for device isolation. The deep trenches allow insulation voltages of over 500V [3-5].

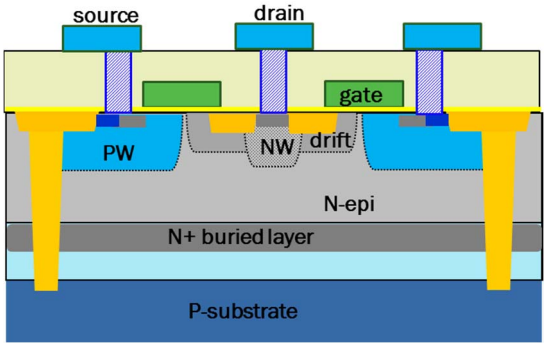

Figure 1: Schematic cross-section of DMOS device. The deep trench surrounds each device providing high voltage isolation. [2].

The deep trenches consist of an oxide liner and a polysilicon fill layer (Fig. 1). The purpose of the polysilicon is to reduce stress associated with the thermal expansion mismatch of Si and SiO_2 [5,6]. Although the polysilicon helps reduce the stress, there is still considerable stress present because the trenches can be on the order of 40 µm deep [3] and the oxide liners can be over 1µm in thickness [4]. The stress from the deep trench during high temperature thermal cycles can cause dislocations and slip, resulting in yield loss (Fig. 1) [4-9].

In this study, we show that there are two unique gate oxide failure mechanisms associated with deep trench processes for a 0.18 µm power semiconductor device. These defects are eliminated by optimizing the SiN oxidation barrier used during deep trench oxidation and by optimizing high temperature anneals to minimize dislocation generation.

II. Experimental

A. Wafer Fabrication

The DMOS devices were fabricated on 200mm Si wafers, using a 0.18 µm CMOS process. Deep trenches are etched in the Si to a depth of ~ 40 µm (Fig. 2a). The trenches are lined with SiO_2, consisting of a thermal oxide and an oxide deposited by chemical vapor deposition (CVD), and filled with polysilicon (Fig. 2b). The excess polysilicon is removed by chemical mechanical polishing (CMP). Next, the wafers go through a series of implants and high temperature anneals, to form wells and high voltage regions (Fig. 2c). The remaining steps consist of standard CMOS processes; gate formation, spacers, source/drain junctions, silicide, and metallization. Note that there are two gate oxide thicknesses, 3.5 nm and 6.2 nm, corresponding to 1.8V and 3.3V CMOS devices.

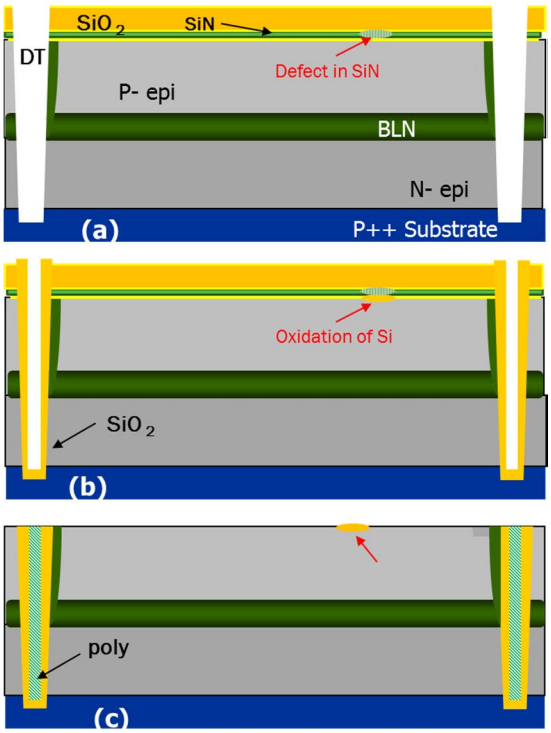

Figure 2. Schematic cross-section of deep trench (DT) formation; (a) deep trench etch, (b) oxidation of deep trench sidewalls, (c) polysilicon fill and CMP. Note that if there is a pinhole in the SiN diffusion barrier, local oxidation of the active area may occur, resulting in a "mini-LOCOS" defect.

B. *Failure Analysis*

Gate oxide yield and reliability were assessed with a ramp breakdown test. The test structures consist of either thin or thick gate oxide devices, surrounded by deep trenches (Fig. 3)

Figure 3. Top-down schematic of deep trench array used for measuring gate oxide yield and reliability. The polysilicon gates consist of either fingers or plates over the active area in each device island, bounded by deep trench

For failure analysis, current-voltage (I-V) curves were measured for virgin devices, ramping the voltage to breakdown. However, the current through the device was limited to minimize electrical damage.

The gate oxide failure location was found using optical beam induced resistance change (OBIRCH) [10]. The failing location was then extracted using a focused ion beam (FIB) cut. Images of the fail were acquired using transmission electron microscopy (TEM).

C. *Stress measurements*

Stress in the silicon from the deep trench was modelled using technology computer aided design (TCAD). The stress is caused by two effects; (1) thermal expansion mismatch of Si and SiO_2 (2) shrinkage of the polysilicon fill due to grain growth during high temperature anneals. The simulation focused on the high temperature anneals after deep trench formation, as these processes will be the most critical for dislocation formation.

The stress in the silicon wafers after device fabrication was measured using X-ray diffraction imaging (XRDI). [11]. XRDI (also known as X-ray topography) is often used for monitoring localized strain and associated defects in Si wafers. XRDI has been used to image slip bands at the edge of wafers caused by high temperature anneals. Recently, XRDI has been used to detect strain in Si associated with deep trenches [9].

III. Results and Discussion

In the initial stage of technology qualification, the gate oxide defect density was unacceptably high (> 2.0 defects/cm^2) for automotive reliability [12], for both thin and thick gate oxides. I-V curves were obtained for virgin devices on wafers with gate oxide fails (Fig. 4). Gate oxide fails (breakdown voltage < 2V) are observed for one or two devices on the failing wafers. The defect density associated with the wafers using deep trench is ~ 2x higher compared to wafers with no deep trench, indicating that that the deep trench process contributes to gate oxide fails

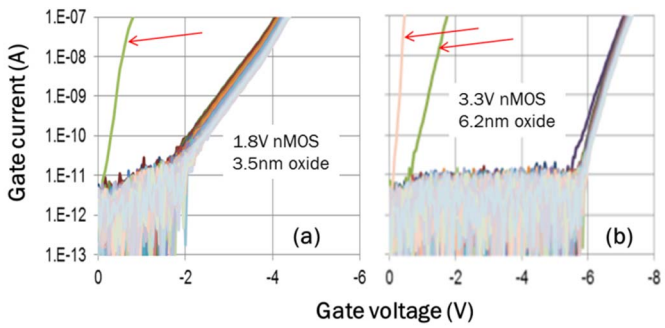

Figure 4. I-V curves for (a) thin gate oxide and (b) thick gate oxide nMOS devices with plate polysilicon gate. 155 devices were tested on each wafer. Red arrows point to IV curves of defective devices (high current at low applied voltage)

A. Thick gate oxide defects; Mini-LOCOS

TEM images of the thick gate oxide defects show a poorly defined thick thermal oxide layer ('mini-LOCOS defect' ~100nm maximum thickness) in the active area (Fig. 5 and 6). In the process flow, only the deep trench thermal oxide is thick enough to cause this type of defect. The active area should be protected by an SiN diffusion barrier during the deep trench thermal oxidation. However, if there are pinholes in the SiN diffusion barrier, then local oxidation of silicon (ie. similar to the LOCOS process) can occur in the vicinity of the pinhole (Fig. 2b).

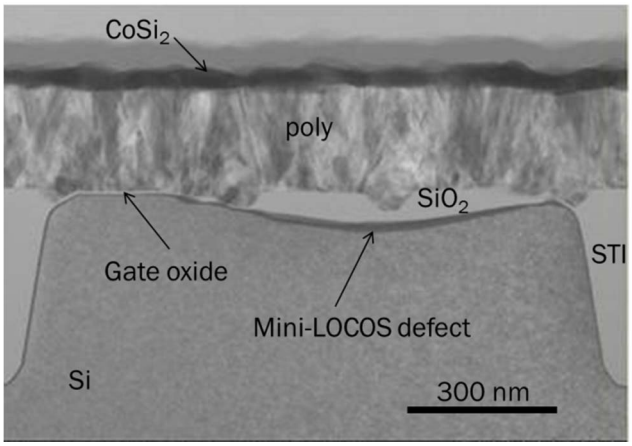

Figure 5. Bright-field TEM cross-section image of mini-LOCOS defect in thick gate oxide region.

At first, it might seem surprising that a defect associated with thick oxidation would cause a gate oxide fail. However, high resolution TEM images (Fig. 6) show that there is thinning of the gate oxide at the perimeter of the defect. Presumably, this thinning is responsible for the gate oxide fails.

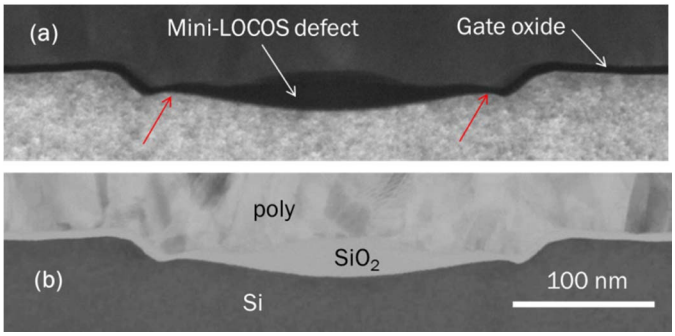

Figure 6. High resolution TEM cross-section images of mini-LOCOS defect in thick gate oxide region. (a) dark field and (b) bright field. Note that there is thinning of the gate oxide at the perimeter of the mini-LOCOS defect.

Wafers were inspected for mini-LOCOS defects after deep trench oxidation. Circular-shaped defects were in fact observed on some wafers (Fig. 7a). TEM images confirm that the defects correspond to local oxidation of Si through pinholes in the SiN diffusion barrier. (Fig. 7b and c). Mini-LOCOS defects were eliminated by optimizing the SiN thickness. The SiN must be sufficiently thick to ensure that there are no pinholes during the deep trench oxidation.

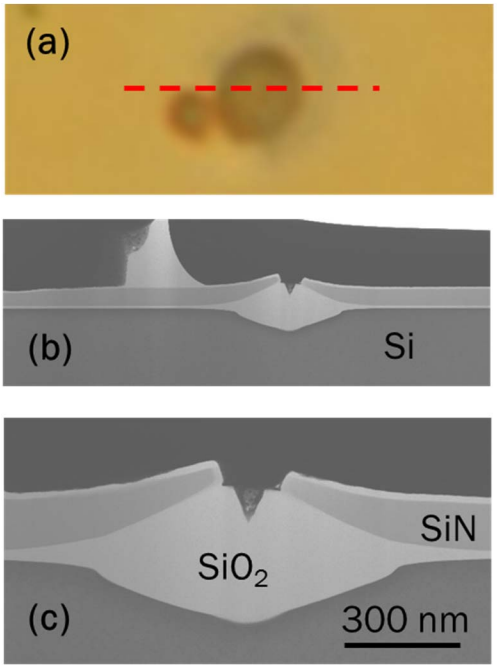

Figure 7. Images of mini-LOCOS defects after deep trench oxidation; (a) top-down optical image showing circular defect; (b) low-magnification and (c) high magnification TEM cross-section images. The Si active area is locally oxidized at a pinhole in the SiN diffusion barrier.

B. Thin gate oxide defects; Dislocations

The Optical Beam Induced Resistance Change (OBIRCH) [10] images of the thin gate oxide defects indicate that there are lines of "hot spots" in the middle of the device region corresponding to gate oxide defects (Fig. 8).

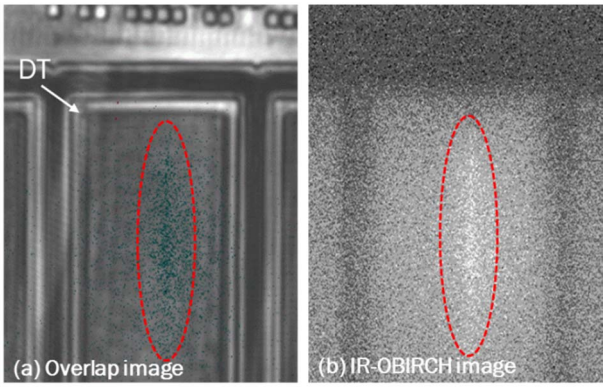

Figure 8. IR-OBIRCH images of thin gate oxide defects in device that is surrounded by deep trench.

Cross-section TEM images show that the gate oxide fails are caused by slip at the surface of the active area (Fig. 9). The origin of the slip is dislocations that originate from the bottom of the deep trench, during high temperature anneals. The dislocations propagate from the bottom of the deep trench to the surface of the active area along the {111} slip plane, when the dislocations reach the surface, slip causes a step in the silicon surface. The step in the Si surface causes localized thinning of the gate oxide, and therefore reduces the breakdown voltage.

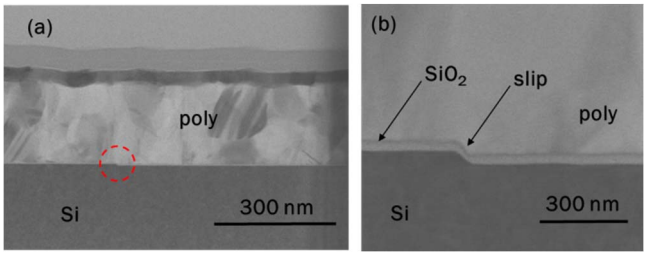

Figure 9. Bright field TEM images of thin gate oxide defects caused by slip at the surface of the active area. (a) shows general view of the polysilicon on gate oxide over silicon. The slip defect is circled in red. (b) is a higher magnification view of the circled are in (a)--note that there is thinning of the gate oxide at the slip surface.

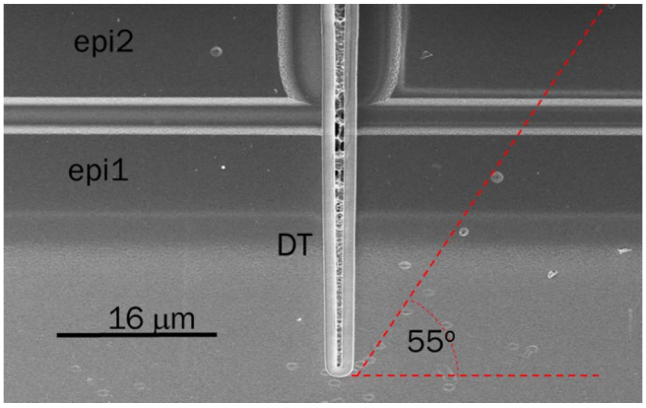

Figure 10. SEM cross-section with defect highlight etch. Dislocations from bottom of deep trench cause slip at surface. The dislocations clustering about the 55 degree line are consistent with propagation of the dislocations along the {111} slip plane.

Dislocations from the deep trench were detected using a defect etch (HF: HNO_3:CH_3COOH:H_2O) (Fig. 10). The bottom tip of the deep trench induces high stress in nearby silicon, causing dislocations to form during thermal processing. Note the dislocations propagate from the bottom of the deep trench to the surface of the active area along the silicon {111} slip plane. The resulting slip at the surface can lead to thinning of the gate oxide and hence low breakdown voltage.

There are a number of ways to minimize stress and dislocations associated with deep trenches. One approach is to optimize high temperature anneals during and after deep trench formation, in terms of ramp rates and temperature uniformity [12]. The stress induced by cross wafer temperature variation, combined thermal expansion mismatch induced stress at high temperature, increases dislocation generation. [14] In fact, it was observed that thin gate oxide fails were associated with a particular rapid thermal anneal (RTA) tool. It was determined that there was a large variation in temperature across the wafer during the ramp up (Fig. 11a), making it more likely for dislocations to form. The thin gate oxide fails were greatly reduced by optimizing the temperature profile in the RTA tool (Fig 11b).

Another approach to minimizing dislocations associated with deep trenches is to optimize the shape, size of, and materials inside the deep trench [4-6]. In particular, the deep trench width is expected to modulate stress. If the trench width is too small, there will be an enhanced stress concentration at the bottom of the trench due to the small radius of curvature of the trench tip. However, if the trench width is tool large, there will be an increasing contribution of stress associated with shrinkage of the polysilicon fill (caused by grain growth) during high temperature anneals.

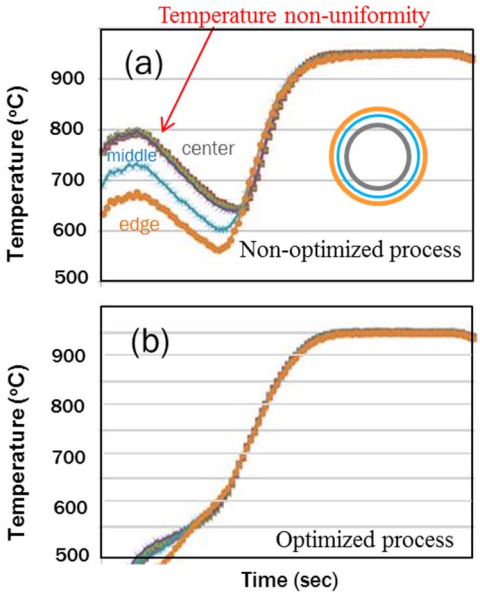

Figure 11. Temperature vs time for RTA tool associated with thin gate oxide fails; (a) Before optimization, there is a non-uniform temperature profile across the wafer during ramp up. (b) After optimization, there is a uniform temperature profile across the wafer.

Simulations of the stress in Si next to deep trenches (Fig. 12) show an increased stress after high temperature anneals as the trench width increases (Fig. 12).

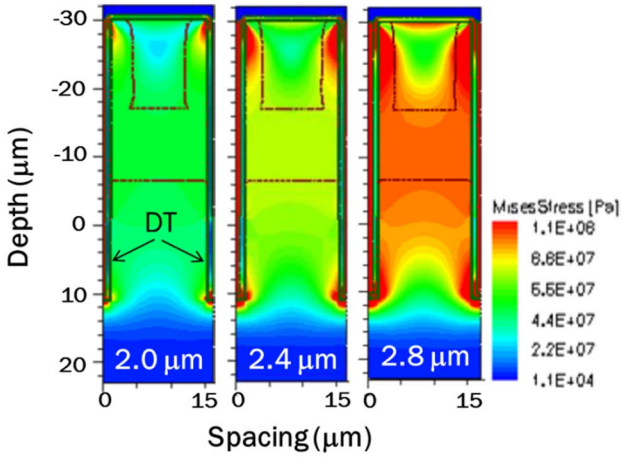

Figure 12. Simulated von Mises stress in Si between two deep trenches. The stress in Si increases as trench width increases from 2.0 µm to 2.8 µm.

Stress in Si measured by XRDI also increases with deep trench width, consistent with the simulations (Fig. 13). The XRDI exhibits dark contrast in regions of the Si that have high stress [9]. It is evident that there is higher stress in the deep trench arrays compared to the regions with no deep trenches. In addition, the contrast is darker, indicating higher stress in the Si, as the width of the trench increases.

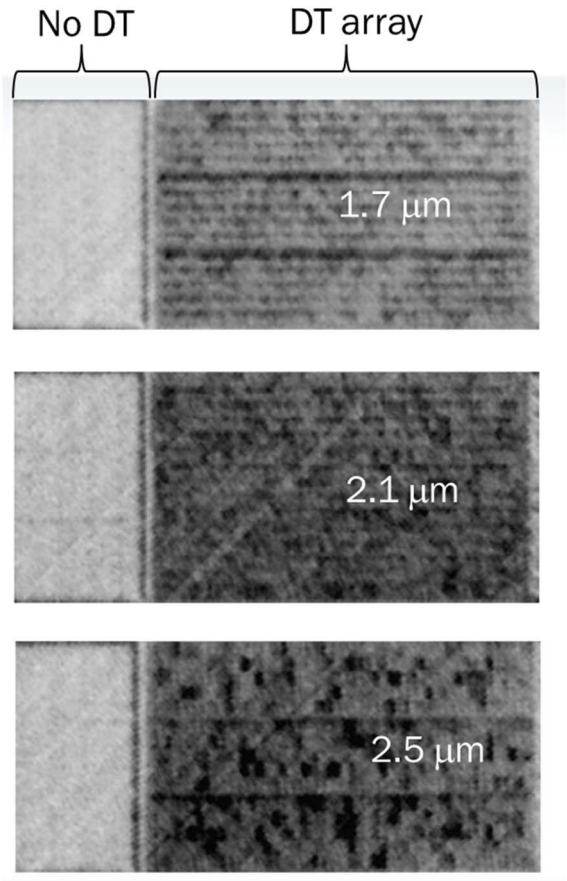

Figure 13. XRD images of deep trench array for DMOS wafers with three different deep trench widths. The contrast is darker as trench width increases, indicating more stress in the Si adjacent to the trench.

The defect density of thin gate oxides is also correlated to the width of the deep trench, with higher defect density as trench width increases (Fig. 14). Hence, trench width must be optimized to minimize dislocation formation.

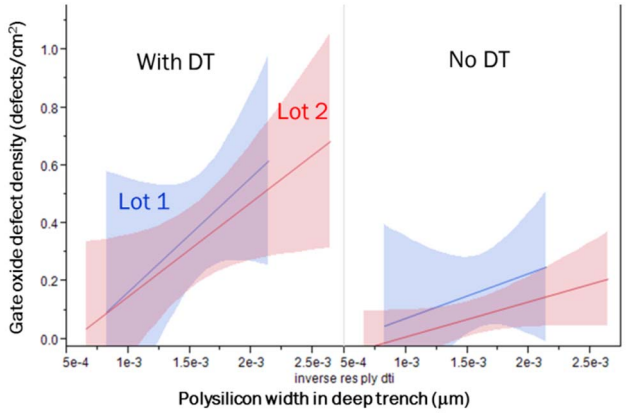

Figure 14. Thin gate oxide defect density vs deep trench width for (a) devices with deep trench and (b) devices with no deep trench. Note that for devices with deep trench isolation, the defect density increases with deep trench width.

IV. Conclusions

Two unique gate oxide failure mechanisms are associated with deep trench processes for a 0.18 µm power semiconductor device. One failure mode is a "mini-LOCOS" defect, that is due to inadvertent oxidation of Si in the active area during deep trench oxidation. The other failure mode is due to slip associated with dislocations from the deep trenches. These defects are eliminated by optimizing the SiN oxidation barrier used during deep trench oxidation and by optimizing high temperature anneals to minimize dislocation generation.

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