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IEEE Guide for Control Architecture for High Power Electronics (1 MW and Greater) Used in Electric Power Transmission and Distribution Systems

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Abstract: Control architecture for high-power electronics from power semiconductor device levels to the power system level is defined and characterized. Coverage includes the application of power electronics in the areas of Power Quality/Custom Power, Flexible AC Transmission Systems (FACTS), High Voltage DC Transmission (HVDC), Distributed Generation, Energy Storage applications, etc. with a power range from hundreds of kW to thousands of MW, but with emphasis on the 1 MW to hundreds of MW.
Keywords: ac-dc converter, control and protection, control architecture, custom power, DVR, FACTS, HVDC, IEEE 1676, MVA, power electronics, Power Electronics Building Block (PEBB), SSTS, STATCOM

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Introduction

This introduction is not part of IEEE Std 1676-2010, IEEE Guide for Control Architecture for High Power Electronics (1 MW and Greater) Used in Electric Power Transmission and Distribution Systems.

A significant degree of common functionality is observed in the control functions of many power electronic systems irrespective of the target application. Using the concept of system levels (or layers), this document defines hierarchical control architecture for these systems. Such definitions enable the use of common designs for multiple applications and the use of commercial electronics and communications modules to increase the cost effectiveness of power electronics applications.

The purpose of this guide is to define hierarchical control architecture, define various parameters/functions that need to be handled within each layer, and those that need to be communicated between the layers and their required speed range. When the control functions of many different power electronic systems are investigated and evaluated, a significant degree of common functionality emerges, irrespective of the target application. Using the concept of system layers, it is possible to define a hierarchical control architecture for high-power electronics-based systems. The intent of this document is to provide a framework and guideline specifically for the control system in order to allow multiple vendors to design and manufacture components, subassemblies, and software that can be used in a large variety of power electronic products or systems. This guideline will also serve as a foundation for interchangeability among different manufacturers at the layer level with defined interfaces.

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Contents

IEEE Guide for Control Architecture for High Power Electronics (1 MW and Greater) Used in Electric Power Transmission and Distribution Systems

1. Overview

In 2003, IEEE Working Group i8 "Power Electronics Building Block Concepts," of Power Electronics Subcommittee, of PES Substations Committee, published a document for a variety of high-power electronics applications in the areas of Power Quality/Custom Power, Flexible AC Transmission Systems (FACTS), High Voltage DC Transmission (HVDC), Distributed Generation, Energy Storage applications, with a power range from hundreds of kW to thousands of MW, but with emphasis on the 1 MW to hundreds of MW. This document, IEEE Product Number 04TP170, "Power Electronics Building Block (PEBB) Concepts," is available from IEEE.

Concurrently, Task Force 1 of the sponsoring Working Group i8, worked on defining control architecture for PEBB-based power electronics, as shown in Figure 1. This Task Force concluded that when the control functions of different power electronic systems are investigated and evaluated, a significant degree of common functionality emerges, irrespective of the target application. Using the concept of system layers, it is possible to define hierarchical control architectures for these systems. Such definitions enable the use of common designs for multiple applications and the use of commercially available electronics and communications modules significantly reducing the cost of power electronics applications. It is important, therefore, that the overall systems control architecture be inherently capable of supporting multiple applications, regardless of their configuration.

The Working Group i8 concluded that this architecture is broadly applicable, whether or not the power electronics is PEBB-based. For consistency, the term PEBB will be used throughout the document. The term PEBB(s) can be substituted, however, by Module(s), Stack(s), Brick(s), Panel(s), etc. It is not the intention of this document to define the contents of a PEBB, Module, Stack, Brick, Panel, etc., nor to define the engineering details of each layer of the architecture, but to define various parameters/functions that need to be handled within each layer and those that need to be communicated between the layers and their required communication speeds.

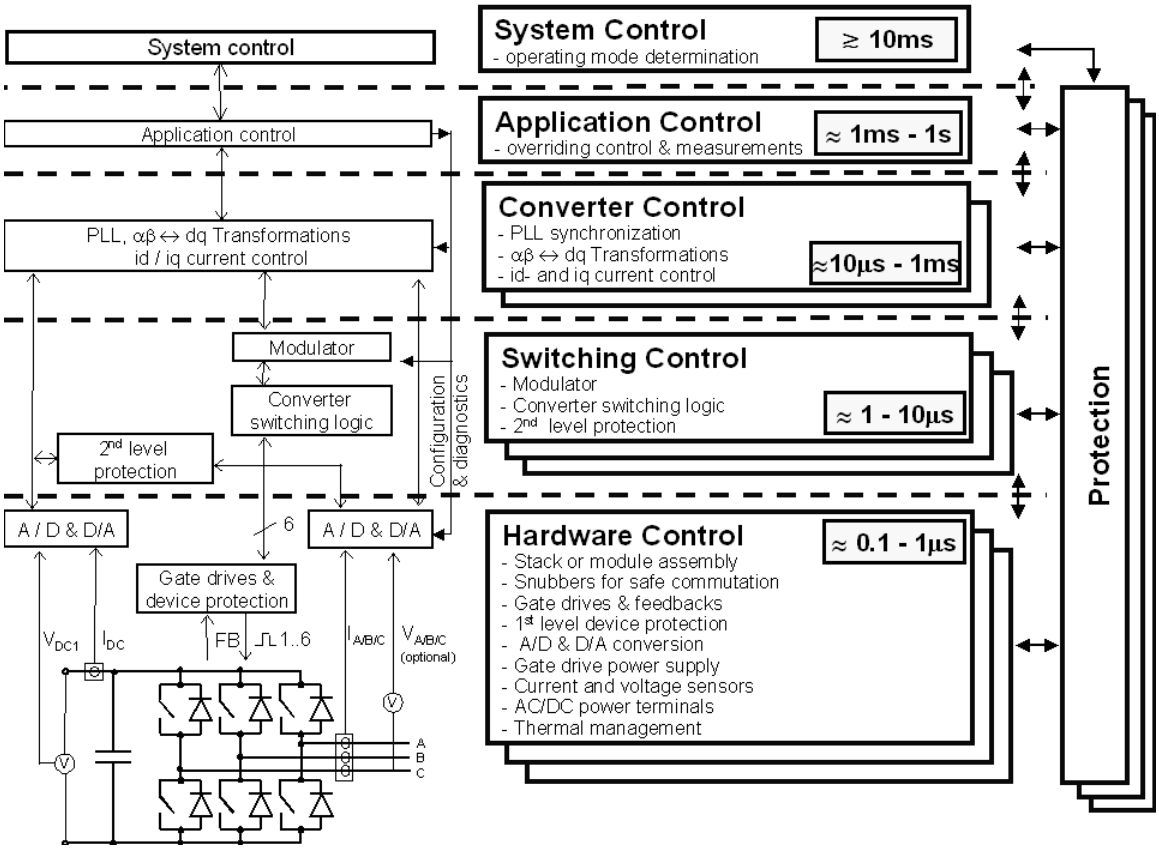


Figure 1—Recommended architecture for power electronics applications

Source: IEEE Product Number 04TP170, "Power Electronics Building Block (PEBB) Concepts."

The move toward modular control architecture is further motivated by the rapid obsolescence of controls relative to other parts of power electronics systems. Consequently, it is imperative that portions or layers of the controls be independently upgradeable to avoid the need to replace the complete power electronics system. A common definition of the control layers, with defined interfaces, enables the ability for a partial upgrade.

These common control layers, as shown in Figure 1, include a system control layer that determines the overall mission of the system, an application control layer responsible for maintaining overall functions of the power electronics, a converter control layer that implements many common functions of converters, a switching control layer that handles the switching logic/sequence, and the hardware control layer that manages everything specific to the power hardware. Each layer has characteristic processing and communication speed requirements, irrespective of the final applications.

The stakeholders of this guide include owners, designers and suppliers of high-power electronics equipment for transmission or distribution systems.

1.1 Scope

The scope of this guide is to define and characterize control architecture for high-power electronics from power semiconductor device levels to the power system level. This guide covers the application of power electronics in the areas of Power Quality/Custom Power, Flexible AC Transmission Systems (FACTS), High Voltage DC Transmission (HVDC), Distributed Generation, Energy Storage applications, etc. with a power range from hundreds of kW to thousands of MW, but with emphasis on the 1 MW to hundreds of MW.

1.2 Purpose

The purpose of this guide is to define hierarchical control architecture, define various parameters/functions that need to be handled within each level, and those that need to be communicated between the levels and their required speed range. When the control functions of many different power electronic systems are investigated and evaluated, a significant degree of common functionality emerges, irrespective of the target application. Using the concept of system levels (or layers), it is possible to define a hierarchical control architecture for high-power electronics-based systems. The intent of this document is to provide a framework and guideline specifically for the control system in order to allow multiple vendors to design and manufacture components, subassemblies, and software, which can be used in a large variety of power electronic products or systems. This guideline will also serve as a foundation for interchangeability among different manufacturers at the layer level with defined interfaces.

1.3 Limitations

This guide is intended specifically for high-power applications with a power range of hundreds of kW to thousands of MW, but with emphasis on the 1 MW to hundreds of MW used in electric power transmission and distribution systems.

1.4 Guide for users

This guide is organized into six clauses and two annexes:

- Clause 1 is an overview of the scope, purpose, and organization of this guide
- Clause 2 lists the indispensible normative references
- Clause 3 provides definitions, abbreviations and acronyms used throughout the text of this guide
- Clause 4 provides the principle of control partitions
- Clause 5 is the recommended architecture and interface design guideline
- Clause 6 is a design example using the guideline
- Annex A provides a case study on interface characterization
- Annex B is a bibliography of related publications

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Product Number 04TP170, "Power Electronics Building Block (PEBB) Concepts," (available from IEEE Customer Service Department, customer-service@ieee.org.)

3. Definitions, acronyms, and abbreviations

3.1 Definitions

For the purposes of this document, the following terms and definitions apply. *The IEEE Standards Dictionary: Glossary of Terms & Definitions* should be consulted for terms not defined in this clause.[1]

***α*:** Signals that may be configuration related and occur at set-up or at infrequent intervals.

application control layer (App): All functions involved in the operation of the power electronic system in order to meet the mission determined by the system control.

NOTE—See 5.1.2.

converter control layer (Cnv): All functions that enable the application control layer to perform its mission by implementing many of the functions common to all converters such as synchronous timing, current and voltage filtering, measurements, and feedback control calculations.

NOTE—See 5.1.3.

hardware control layer (Hwr): All functions that manage everything specific to the power devices; it may consist of multiple modules depending on the power requirements.

NOTE—See 5.1.5.

system control layer (Sys): All functions involved in the determination of the system mission and the duties of the power electronics system.

NOTE—See 5.1.1.

switching control layer (Swt): All functions that enable the power electronics to behave as a switch-mode controlled source and includes modulation control and pulse generation.

NOTE—See 5.1.4.

3.2 Acronyms and abbreviations

App	application control layer
App-Cnv	boundary between the application and converter control layers

[1] *The IEEE Standards Dictionary: Glossary of Terms & Definitions* is available at http://shop.ieee.org/.

BESS	Battery Energy Storage System
C	control commands interface characteristic classification; See A.1
CB	Channel Bandwidth
Cnv	converter control layer
Cnv-Swt	boundary between the converter and switching control layers
DVR	Dynamic Voltage Restorer
FACTS	Flexible AC Transmission Systems
f_{sam}	sampling frequency
f_{sw}	switching frequency
Hwr	hardware control layer
HVDC	High Voltage DC Transmission
IGBT	Insulated-Gate Bipolar Transistor
I	system information
I_{max}	(A) over-current phase; (B) maximum current
I_{ref}	reference current
K_d	ratio of sampling period to transmission time
M	measurement interface characteristic classification
Meas	measurement signals
N	number of signals
nb	number of branches
n_d	number of bits representing the analog signal
nl	number of levels in the converter
n_x	number of bits representing the variable x
P	protection interface characteristic classification; See A.1
PI	Proportional Integral
PEBB	Power Electronics Building Block
PLL	synchronous timing; Phase-Locked Loop
S	settings of the control system interface characteristic classification; See A.1

SSTS	Solid-State Transfer Switch
SVPWM	Space Vector Pulse Width Modulator
Sys	system control layer
Sys-App	boundary between the system and application control layers
Swt	switching control layer
Swt-Hwr	boundary between the switching and hardware control layers
T	start-up and self-check interface characteristic classification; See A.1
UPFC	Unified Power Flow Controller
VAR	Volt Amps Reactive (Reactive Power)
V_{ref}	reference voltage
V_{max}	maximum voltage

4. Principles of control partition

The overall control of a power electronics system is achieved by arranging rudimentary control functions to produce a desired control. Traditional power electronics system designs often combine various parts of control functions together blurring the boundaries of each. The layout of the control structure typically occurs during software development, e.g., assembly code, C-code programming where control modularity is traded for reductions in code size and execution speed. Although a hierarchical partitioning may not yield the most computationally efficient design, partitioning these control functions can increase interconnectivity and reduce reoccurring engineering for follow-on efforts. Moreover, the continuous trend of increasing digital controller performance and memory size along with reduction of cost has now reached a point where the benefits of code optimization rarely outweigh the benefits of modularity.

The concept of control partitioning has been developed and analyzed for generic power electronics applications (see Ericsen et al. [B5]). Utility power system applications with their ratings and complexities can be a promising field for building and developing power electronics systems based on hierarchical modular subsystems.

4.1 Partition criteria and basic architecture

In general, a partition may be based on the following criteria:

- Functional partition, e.g., application control, converter control, switching contol
- Temporal partition, e.g., protection, switching frequency and modulation, time constants, control bandwidth
- Spatial partition, e.g., compartments, drawers, floor
- Technological partition, e.g., digital, analog, miniaturization

All four criteria should be used for partitioning. However, because the technological and spatial criteria are specific to particular implementations, the functional and temporal partitions are considered to be the driving criteria. In the majority of cases, these criteria naturally occur at the same boundaries.

In Celanovic [B1] and Celanovic et al. [B2], a control architecture was proposed for generic power electronics systems. Systems comprised of discrete subsystems and modules, such as PEBB-based systems, simplify the integration of the partitioned architecture concept; however, PEBB-based hardware is not a requirement. The architecture should be independent of the application.

Figure 1 is a typical converter application with a basic partition of the control system. In this case, the power hardware subsystem (stack or module assembly in Figure 1) is composed of a phase leg with the functions of switching and primary device monitoring and protection, as well as the phase current sensing. However, the modularization of a power electronic system does not depend on the power module configuration. In Hanson [B7], a manufacturer presented products based on half-bridge power modules; in Hingorani et al. [B8] another manufacturer used an H-bridge as the basic power module. It is important to note that partitioning hardware modules will not change the basic function of the hardware control layer and will be transparent to higher control layers. Figure 1 also suggests that the partition for a converter system control consists of multiple subsystems arranged in five layers: a system control layer, an application control layer, a converter control layer, a switching control layer, and the hardware control layer. An outline of this discussion is presented in Wang et al. [B24]. In other cases, additional control layers may be necessary, or multiple layers may be combined.

It is recognized that an application may have more than one piece of power electronics hardware, e.g., converter. This may be because one converter is not enough to meet the power requirement or more than one converter is needed to meet power quality, redundancy, etc. The converters may be remote from each other and linked together through transmission or distribution lines. The proposed architecture recommends that each converter have its own independent switch control to serve its hardware control. The proposed architecture further suggests that there may be a common converter control to serve multiple switching controls. Also, one application control may serve more than one converter control. The function of protection is to take the necessary action as fast as required; therefore, the function of protection may go to any of the layers.

The interfaces between control layers are denoted by the hyphenated abbreviations of layer names with the higher layer appearing first as shown in Figure 2. Signals crossing the boundaries are referenced with respect to the originating control layer.

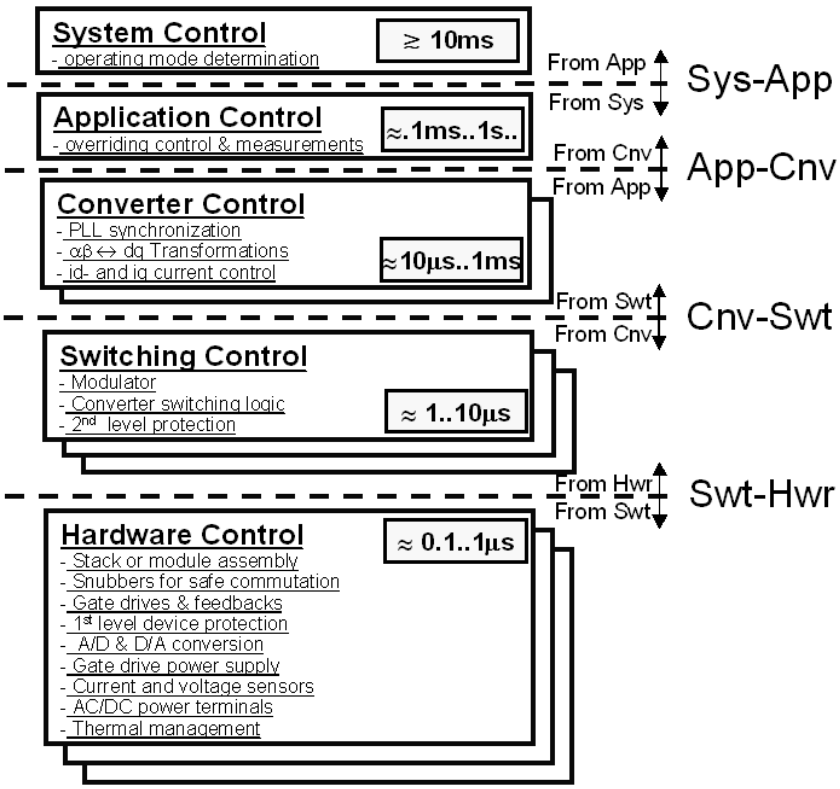


Figure 2—Control layer interfaces and signal direction convention

4.2 Functional Partition

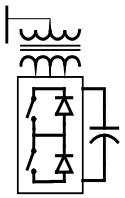
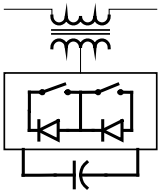
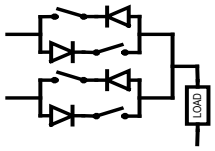
In order to partition a system, it is necessary to determine the control functions of the system. In Annex A, different applications for utility systems are analyzed: a shunt connected compensator represented by a static compensator (STATCOM), a series connected compensator represented by a dynamic voltage restorer (DVR), and a solid-state transfer switch (SSTS). The first two applications are based on voltage source converter topology. The third system corresponds to a symmetrical ac switch best implemented using current source topology.

The functional analysis is divided into the system control layer, application control layer, converter control layer, switching control layer and hardware control layer. The system layer controller, also called external controller, establishes the functions that are the main mission of the power electronics system. These goals determine the function of the application control layer. In order to achieve the goals required by the system and implemented by the application control, some standard control functions should be performed. The converter control layer comprises the control functions necessary to achieve those results. Finally, the desired functions require an operation of the hardware elements. This translation of the control function to the hardware operation is done at the switching control and hardware control layers. Table 1 shows the control function classification for the DVR, STATCOM and SSTS examples.

The functions in the hardware control layer are common to all applications. The only difference appears when one or the other type of stack/module assembly is used and the differentiating characteristic is the reason for using one or the other type of topologies. The switching control layer functions are also common across many of the applications. At that layer, the differentiating factor is the voltage source or current source topology. Above the switching control layer all of the layers have some differences across

applications; however, the differences become more numerous as the layers are traversed upward toward the system control layer.

Table 1—Functional analyses of DVR, STATCOM, and SSTS

System	STATCOM	DVR	SSTS
Simplified one-line diagram			
System control layer	Voltage support and reactive power compensation	Mitigation of the effect of sags by adding a voltage during disturbances	Increase the reliability of the electric supply
Application control layer	1- Reactive power compensation 2- Transient stability enhancement 3- Power oscillation damping 4- VAR reserve control	1- Three-phase voltage regulation 2- Three-phase voltage balance 3- Energy storage administration. 4- By-pass function	1- Disturbance detection 2- Detection of inhibition condition 3- elect the source of energy 4- Open/close mechanical switch
Converter control layer	1- Synchronous timing (PLL) 2- Line current control 3- Include V_{DC} for calculation of duty cycles (in direct control)	1- Synchronous timing (PLL) 2- Output I & V control 3- Management of the energy storage, dc connection (I_{DC} control)	1- Synchronous timing (PLL) 2- Open/close solid state circuit breaker
Switching control layer	1- Duty cycle calculation 2- Switching control (modulation control)		1- Firing pulse computation
Hardware control layer	1- Pulse gating 2- Safe commutation enabling (limiting dv/dt, di/dt, etc) 3- Primary protection of devices 4- Power magnitudes sensing and conditioning		

4.3 Temporal partition

Along with the functional distribution, the temporal distribution is considered to be a driving criterion. In a majority of cases, functional and temporal distributions naturally occur at the same boundaries.

Annex A presents an analysis that illustrates the spatial and temporal partitions have commonality. When a system is partitioned, the partition interface should be designed to meet performance requirements of different layers, including requirements on data volume and transmission rates. The interface should be designed to enable layer modularity such that replacement of any layer should not induce modifications in other layers.

The interface analysis presented here demonstrates that a multi-layer hierarchical control partition is an appropriate architecture that can facilitate construction and analysis of power electronics systems for power system applications.

5. Recommended architecture and interface design guideline

The control layers include a system layer, an application layer, a converter layer, a switching layer, and a hardware layer. These layers, shown in Figure 1, are based on temporal considerations. The communication

speed requirements at the lowest, or hardware, layer are the greatest and decline with each higher control layer. However, in some cases the speed ranges for two adjacent layers may overlap due to synchronization requirements. It is preferred to use communication protocols for which industry standards have already been established.

A basic description and criteria for establishing the contents and boundary of each control layer follows.

5.1 Definition of layers in a hierarchical architecture

In order to determine the locations of the control layer boundaries, it is helpful to categorize power electronic systems. The various types of power electronic systems can be placed into one of three broad categories: shunt connected current controller, series connected voltage controllers, and combinations thereof (see Hingorani et al. [B8]). Simplified control architectures for these basic categories are shown in Figure 3 and Figure 4.

5.1.1 System control layer

All functions involved in the determination of the system mission and the duties of the power electronics system belong to this layer. This layer would also include any human-machine interfaces. The functions contained within the system control layer (Sys) are beyond the scope of this guide and may be found in other standards. From the viewpoint of the system controller, the lower control layers execute all power electronic system functions that are necessary to fulfill the system mission.

5.1.2 Application control layer

The application control layer (App) dictates the operation of the power electronics system in order to meet the mission determined by the system control. From the viewpoint of the application controller, the lower control layers of the power electronics system enable the power electronics system to be viewed as one of the two possible equivalent devices: controlled current source or controlled voltage source. For example, as shown in Figure 3 and Figure 4, the boundary between the application control layer and lower control layers (short dashed line) is determined by those control subsystems that enable the power electronics to behave as a controlled current or voltage source. Here the controlled source is defined as having its terminals at the system side of the coupling impedance of the converter. Therefore, the output signal for the application control layer at the interface with the converter control layer should contain either current or voltage reference signals.

5.1.3 Converter control layer

The primary characteristic of the converter control layer (Cnv) is the feedback control system, as shown in Figure 3 and Figure 4, while the other components support the input and output requirements of the feedback control system. The converter control layer implements many of the functions common to all converters such as synchronous timing (e.g., PLL), current and voltage measurement filtering, and feedback control calculations. The PLL is shown separately since, in general, it may be used by the application control layer, the converter control layer, and the switching control layer. In this case, the temporal distribution is the deciding factor placing it within the converter control layer.

5.1.4 Switching control layer

The switching control layer (Swt) and all lower layers enable the power electronics to behave as a switch-mode controlled source and include modulation control and pulse generation. These functions are common and independent of the final application. Here the switch-mode controlled source is defined as having its terminals directly at the power terminals of the PEBB hardware.

5.1.5 Hardware control layer

The hardware control layer (Hwr) manages everything specific to the power devices, and it may consist of multiple modules depending on the power requirements. Gating, galvanic isolation, safe commutation, limits of di/dt, dv/dt, and first level protections, etc., are functions of this layer and are common for virtually any application.

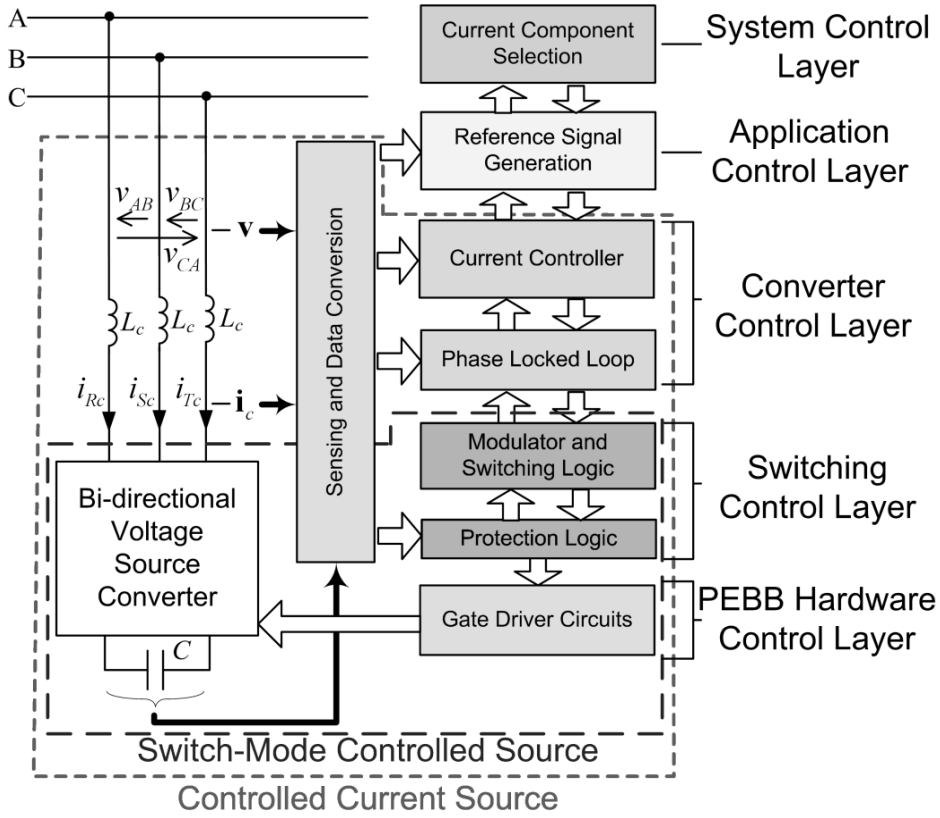


Figure 3— Functional diagram of a shunt connected current controller

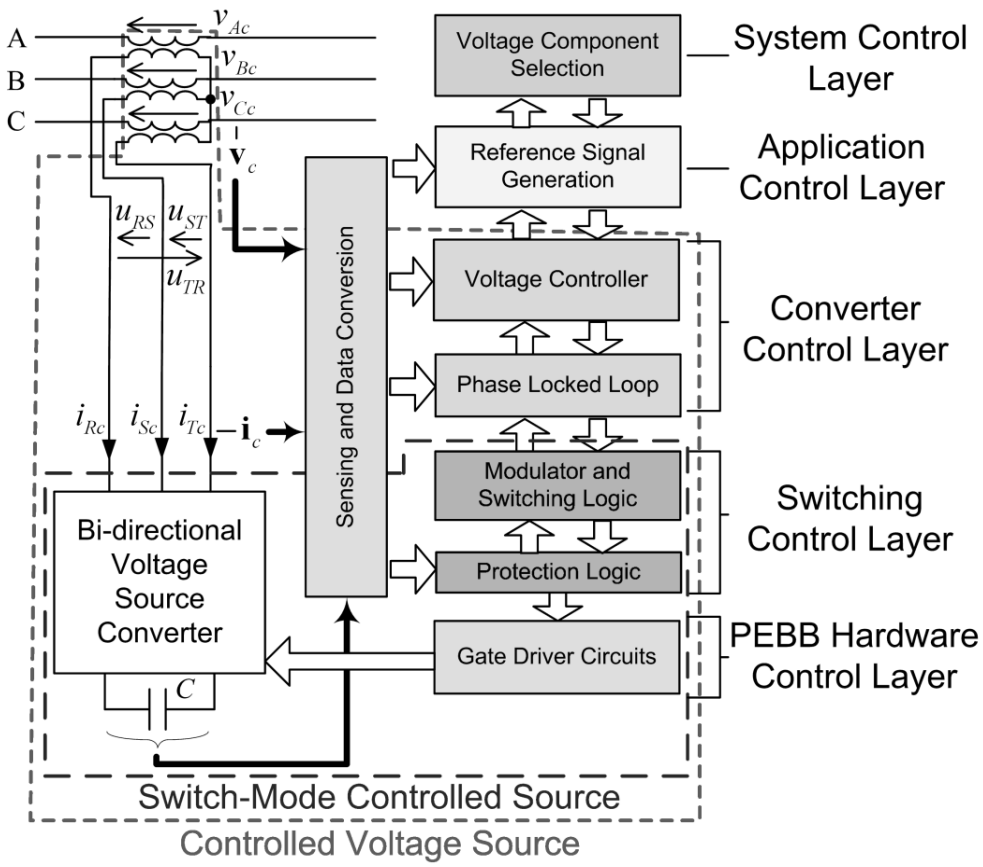


Figure 4— Functional diagram of a series connected voltage controller

5.2 Interface guidelines for the layered architecture

The interface requirements between layers are summarized in this clause. Signal directions are defined at each layer interface with respect to their layer of origin, i.e., originating from the layer above or below the interface. The standard recognizes the necessity of categorizing and characterizing interface signals and recognizes that there are many approaches to accomplishing this such as primary, auxiliary, measurement, functional, fast-speed, slow-speed, priority, etc. Thus, signals are divided into three broad categories that will accommodate the majority of more detailed characterizations. These are: Control and Protection Signals (simply referred to here as Control Signals), State Signals, and Measurement Signals (Meas). Control Signals refer to the signals associated with the main control or protection tasks of a particular control layer. State Signals refer to those signals that either set or report the state of a control layer subsystem or of the converter system as a whole. Measurement Signals are any signals that were generated by an analog to digital conversion process. Once in digital form, Measurement Signals remain as Measurement Signals if no operations other than scaling are performed. If a Measurement Signal enters a control subsystem and an operation more complex than scaling is performed, then the resulting signal is considered to be a Control Signal.

Some information may be traversing the interfaces of the hierarchy and not generated or used by the adjacent layers; in these cases the signal is designated as a pass-through signal. Provisions should be made for a pass-through signal if the control structure is to remain strictly hierarchical.

All measurements are passed up from the hardware layer where the A/D converters are located. Measurement signals are always from the layer below an interface and passed into a layer above an interface.

Provisions may be needed to incorporate diagnostic and prognostic signal monitoring and acquisition of real-time contextual information as required by the approach selected to meet the diagnostic and prognostic requirements for any specific application. Both the real-time contextual and monitoring signal, e.g., temperature and vibration, and the information flow between layers should be in accordance with the diagnostic and prognostic requirements of the application. The software for translating raw data to information should be applied to signals at the appropriate layer required to meet the diagnostic and prognostic requirements for the application.

Table 2 provides representative examples of the required signals passing into or out of each control layer and Table 3 through Table 6 list required signals for each interface. Each interface signal specified in Table 3 through Table 6 is derived from Table 2. For each signal in the Signals Generated Within the Layer column, the number of occurrences of the signal in the Signals Utilized from an External Layer column and position relative to the layer generated determine the number of interfaces to which the signal belongs.

Table 2—Examples of control layer signals[a]

Control Layer	Signal type	Signals generated within the layer	Signals utilized from an external layer
System	**State**	1. Converter mode selection data 2. Application layer controller parameter setting data 3. Converter layer controller parameter setting data 4. Modulator parameter setting data (Ex: *fsw*, dead-time)	1. Converter operating mode data 2. Converter system ready status 3. Application layer controller parameter provisioning data 4. Converter layer controller parameter provisioning data 5. Modulator parameter provisioning data
	Meas.		1. System line currents
Application	**Control**	Voltage or current reference signals	1. Synchronization signal (Ex: phase-locked-loop)
	State	1. Converter system ready status 2. State-commands for circuit configuration devices (such as contactors) 3. State-commands for auxiliary equipment 4. Converter operating mode data 5. Application layer controller parameter provisioning data	1. Converter mode selection data 2. Status of circuit configuration devices 3. Status of auxiliary equipment 4. Application layer controller parameter setting data 5. PEBB overcurrent/overvoltage 6. Status of gate drivers
	Meas.		1. Voltages at point of converter connection 2. System line currents 3. dc bus voltage or current

[a]If a signal is generated in a layer, the same signal will be found in at least one layer of the utilized column.

Table 2—Examples of control layer signals[a] (Continued)

Control Layer	Signal type	Signals generated within the layer	Signals utilized from an external layer
Converter	**Control**	1. Modulator duty cycle command vector. 2. Synchronization signal (Ex: phase-locked-loop)	1. Voltage or current reference signals
	State	1. Converter layer controller parameter provisioning data	1. Converter layer controller parameter setting data 2. Modulator status (Ex: normal, saturated)
	Meas.		1. Voltages at point of converter connection 2. Currents in each phase leg
Switching	**Control**	1. Gate control signals –1 per semiconductor switch	1. Modulator duty cycle command vector. 2. Synchronization signal (Ex: phase-locked-loop) 3. PEBB overcurrent/overvoltage 4. Device protection – 1 per semiconductor switch
	State	1. Modulator parameter provisioning data 2. Modulator status (Ex: normal, saturated)	1. Modulator parameter setting data (Ex: *fsw*, dead-time)
	Meas.		1. dc bus voltage or current

[a]If a signal is generated in a layer, the same signal will be found in at least one layer of the utilized column.

5.2.1 System layer to application layer interface description

An example list of the typical signals at the system layer–application layer (Sys-App) interface is summarized in Table 3 below.

Table 3—Examples of signals at system–application interface (Sys-App)

System layer - application layer interface signals	Type	Generating layer	Utilizing layers
Converter mode selection data	State	System	Application
Converter operating mode data	State	Application	System
Converter system ready status	State	Application	System
Application layer controller parameter setting data	State	System	Application
Application layer controller parameter provisioning data	State	Application	System
Converter layer controller parameter setting data	State	System	Converter
Converter layer controller parameter provisioning data	State	Converter	System

5.2.2 Application layer to converter layer interface description

An example list of the typical signals for the application control layer–converter control layer (App-Cnv) interface is summarized in Table 4 below.

Table 4—Examples of signals at application–converter interface (App-Cnv)

Application layer- converter layer interface signals	Type	Generating layer	Utilizing layers
Voltage or current reference signals	Control	Application	Converter
Synchronization signal from a phase-locked-loop	Control	Converter	Switching, application
State commands for circuit configuration devices	State	Application	Hardware
Status of circuit configuration devices	State	Hardware	Application
State commands for auxiliary equipment	State	Application	Hardware
Status of auxiliary equipment	State	Hardware	Application
State of gate drivers	State	Hardware	Application
Converter layer controller parameter setting data	State	System	Converter
Converter layer controller parameter provisioning data	State	Converter	System
Voltages at point of converter connection	Meas	Hardware	Converter, application
System line currents	Meas	Hardware	Application
dc bus voltage or current	Meas	Hardware	Switching, application

5.2.3 Converter layer to switching layer interface description

An example list of the typical signals for the converter control layer – switching control layer (Cnv-Swt) interface is summarized in Table 5.

Table 5—Examples of signals at converter–switching interface (Cnv-Swt)

Converter layer- switching layer interface signals	Type	Generating layer	Utilizing layers
Modulator duty cycle command vector	Control	Converter	Switching
Synchronization signal from a phase-locked-loop	Control	Converter	Switching, application
State commands for circuit configuration devices	State	Application	Hardware
Status of circuit configuration devices (pass-through)	State	Hardware	Application
State commands for auxiliary equipment (pass-through)	State	Application	Hardware
Status of auxiliary equipment (pass-through)	State	Hardware	Application
State of gate drivers (pass-through)	State	Hardware	Application
Modulator parameter setting data	State	System	Switching
Modulator parameter provisioning data	State	System	Switching
Modulator status data	State	Switching	Converter
Voltages at point of converter connection	Meas	Hardware	Converter, application
Currents in each phase leg	Meas	Hardware	Converter
System line currents (pass-through)	Meas	Hardware	Application
dc bus voltage or current	Meas	Hardware	Switching, application

5.2.4 Switching layer to hardware layer interface description

A minimum list of the typical signals for the switching control layer–hardware control layer (Swt-Hwr) interface is summarized in Table 6 below.

Table 6—Examples of signals at switching–hardware interface (Swt-Hwr)

Switching layer- hardware layer interface signals	Type	Generating layer	Utilizing layers
Gate control signals	Control	Switching	Hardware
Device protection PEBB overcurrent/overvoltage	Control	Hardware	Switching, application
State commands for circuit configuration devices (such as contactors)	State	Application	Hardware
State commands for auxiliary equipment such a heat sink fans	State	Application	Hardware
Status of circuit configuration devices	State	Hardware	Application
Status of auxiliary equipment	State	Hardware	Application
Status of gate drivers	State	Hardware	Application
Voltages at point of converter connection	Meas	Hardware	Converter, application
Currents in each phase leg	Meas	Hardware	Converter
System line currents	Meas	Hardware	Application
dc bus voltage or current	Meas	Hardware	Switching, application

6. Design example using the guideline

An example design is presented that follows the recommended architecture and interface guidelines provided in Clause 5. A voltage source converter connected in the shunt configuration is selected as the design example due to the large number of applications to which that configuration can be applied. The application is a STATCOM/active filter combination.

6.1 System requirements

The active compensator application described here is a typical active power filter application. The term active compensator is used because the power electronic system should be able to selectively inject compensating currents. Each current component, reactive, unbalanced and distorted, should be individually scalable. Thus, the percentage of each measured quantity to be compensated for is determined by the system control according to the mission of the system.

Operating modes such as off, standby and online should be controllable by the system control layer. Also, the control parameters for the dc and current control loops should be adjustable from the system control layer. Finally, error and fault conditions as well as all control parameter values should be reported to the system control.

6.2 Control System Architecture

This implementation meets the power electronics system requirements described in Ginn et al. [B6], and the simplified functional diagram is shown in Table 5. Each block of the functional diagram is examined according to the criteria set forth in 5.1 in order to determine to which layer control subsystems belong. Then, the interface requirements for the layers are determined based on the traversing signals.

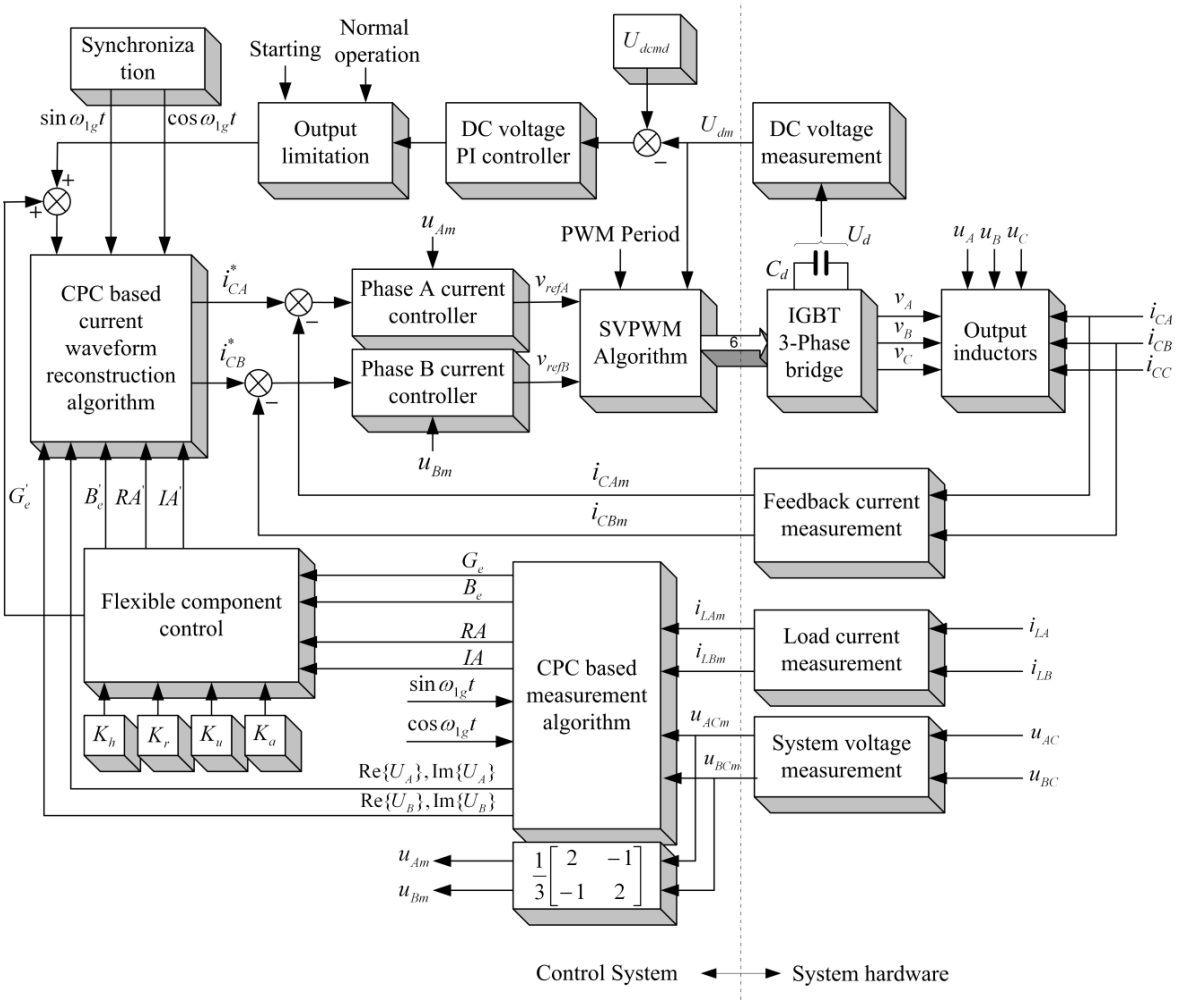


Figure 5—System functional diagram for the example application

6.3 Partitioning and interface requirements

The division shown in Figure 5 between system hardware and the control system corresponds to the partition between the hardware and switching layers in Figure 1. The outputs of the "CPC based current waveform reconstruction algorithm" block are the current reference signals. The subsystems that accept those references enable the power electronics system to function as a controlled source. Thus, that is the boundary between the application layer and the converter control layer. The space vector pulse width modulator (SVPWM) algorithm block belongs to the switching control layer and the inputs into it mark the boundary between the converter control and switching control layers. Figure 6 presents the partitioned system in greater detail in the format of Figure 1. The system shown in Figure 6 is based on the prototype implementation described in Ginn et al. [B6]. However, the developed prototype was for a 100 kW power level in a 480 volt system. Higher voltage and higher power systems may differ in their placement of A/D converters as compared to similar lower voltage, lower power systems. Therefore, in this example the A/D converters are placed in the hardware control layer in accordance with this guide, while for the system in Ginn et al. [B6] they are placed in the switching control layer.

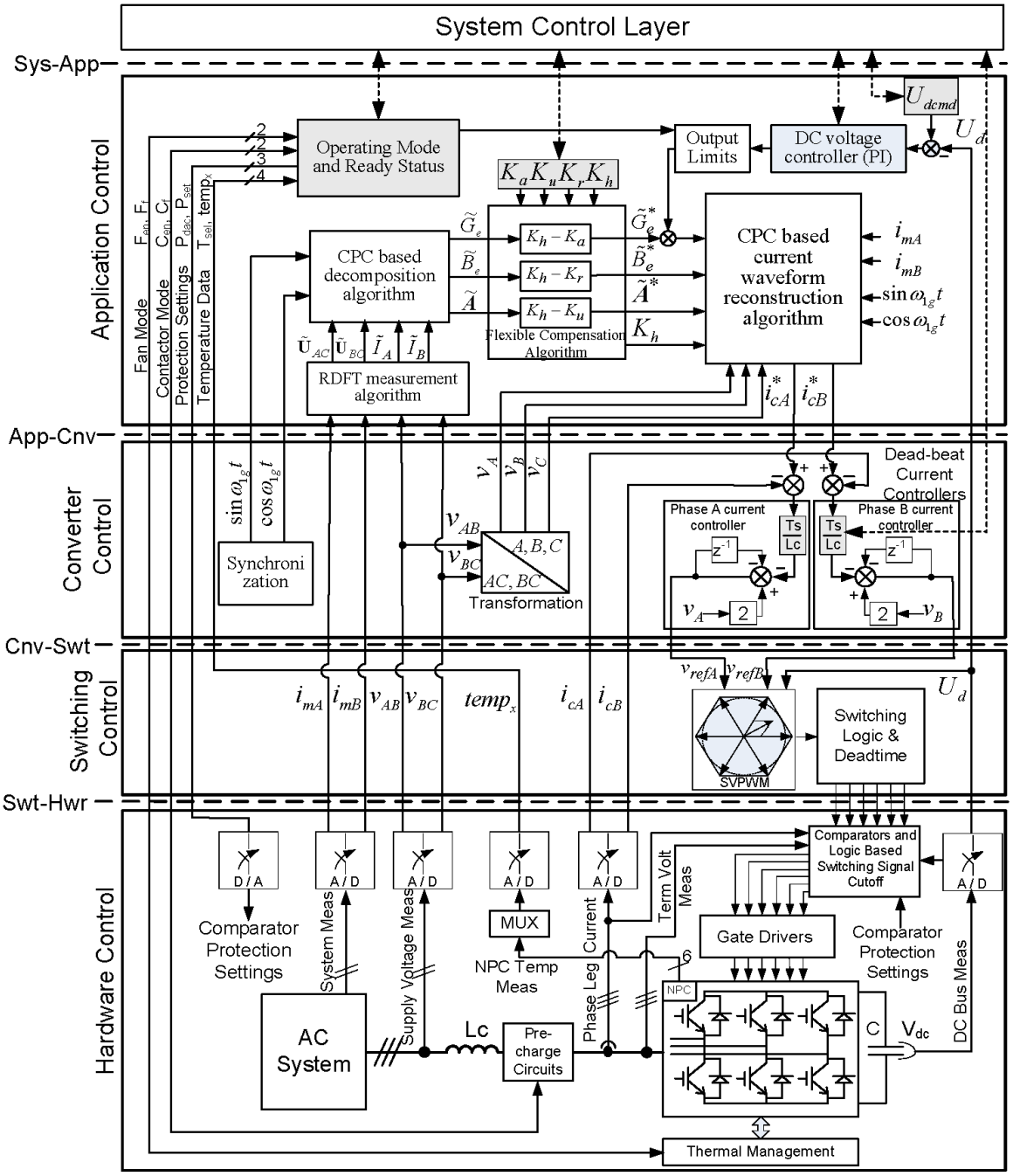


Figure 6—Partitioned system functional diagram for the example application

Table 7—Signals at switching to hardware layer interface (Swt-Hwr)

Signal type	Signal name	Interface signal description	Generating module (layer)	Utilizing module (layer)	Bit resolu-tion	Sampling or update rate
Meas	i_{CA}	Phase A feedback current	A/D converter (Hwr)	Current cont (Cnv)	12-bit	12 kHz
	i_{CB}	Phase B feedback current	A/D converter (Hwr)	Current cont (Cnv)	12-bit	12 kHz
	i_{mA}	Phase A line measured current	A/D converter (Hwr)	RDFT alg (App)	12-bit	12 kHz
	i_{mB}	Phase B line measured current	A/D converter (Hwr)	RDFT alg (App)	12-bit	12 kHz
	v_{AC}	ac voltage, phase A to C	A/D converter (Hwr)	Voltage trans (Cnv)	12-bit	12 kHz
	v_{BC}	ac voltage, phase B to C	A/D converter (Hwr)	Voltage trans (Cnv)	12-bit	12 kHz
	U_d	dc bus voltage	A/D converter (Hwr)	SVPWM (Swt) dc voltage cont (App)	12-bit	12 kHz
	C_f	Precharge feedback	Auxiliary contact (Hwr)	A/D conv (Swt)	1-bit	12 kHz
	F_f	Fan feedback	Fan tach signal (Hwr)	Operating mode and ready status (App)	12-bit	12 kHz
	$temp_x$	Temp channel	IGBT module NPC (Hwr)	A/D conv (Swt) operating mode and ready status (App)	12-bit	12 kHz
Control	PWMA [1-6]	Driving signal for six switches	Switching logic & deadtime (Swt)	Comparators and logic based switching signal cutoff (Hwr)	1 bit per signal	125MHz
	E_{res}	Error reset	Operating mode and ready status (App)	Out comparators and logic based switching signal cutoff (Hwr)	1-bit	α
State	F_{en}	Fan enable, active low	Operating mode and ready status (App)	Thermal management (Hwr)	1-bit	α
	C_{en}	Precharge, active high	Operating mode and ready status (App)	Precharge circuits (Hwr)	1-bit	α
	P_{dac}	Protection function setting selection	Operating mode and ready status (App)	Comparator D/A for protection settings (Hwr)	2-bit	α
	P_{set}	Serial data for DAC	Operating mode and ready status (App)	Comparator D/A for protection settings (Hwr)	16-bit	1.25MHz
	T_{sel}	Channel selection bits for temperature measurement	Operating mode and ready status (App)	Temp meas MUX (Hwr)	3-bit	α

NOTE—α denotes signals that may be configuration related and occur at set-up or at infrequent intervals. The sampling rate at which these signals occur is dependent upon how fast the application needs to self-configure.

Table 8—Signals at converter to switching layer interface (Cnv-Swt)

Signal type	Signal name	Interface signal description	Generating module (layer)	Utilizing module (layer)	Bit resolu-tion	Sampling or update rate
Meas	i_{CA}	Phase A feedback current	A/D converter (Hwr)	Current cont (Cnv)	12-bit	12 kHz
	i_{CB}	Phase B feedback current	A/D converter (Hwr)	Current cont (Cnv)	12-bit	12 kHz
	i_{mA}	Phase A line measured current	A/D converter (Hwr)	RDFT alg (App)	12-bit	12 kHz
	i_{mB}	Phase B line measured current	A/D converter (Hwr)	RDFT alg (App)	12-bit	12 kHz
	v_{AC}	ac voltage, phase A to C	A/D converter (Hwr)	Voltage trans (Cnv)	12-bit	12 kHz
	v_{BC}	ac voltage, phase B to C	A/D converter (Hwr)	Voltage trans (Cnv)	12-bit	12 kHz
	U_d	dc bus voltage	A/D converter (Hwr)	SVPWM (Swt) dc voltage cont (App)	12-bit	12 kHz
	C_f	Precharge feedback	Auxiliary contact (Hwr)	A/D conv (Swt)	1-bit	12 kHz
	F_f	Fan feedback	Fan tach signal (Hwr)	Operating mode and ready status (App)	12-bit	12 kHz
	$temp_x$	Temp channel	IGBT module NPC (Hwr)	A/D conv (Swt) operating mode and ready status (App)	12-bit	12 kHz
Control	vrefA	Modulator voltage reference	Current controller A (Cnv)	SVPWM (Swt)	32-bit	12 kHz
	vrefB	Modulator voltage reference	Current controller B (Cnv)	SVPWM (Swt)	32-bit	12 kHz
	E_{res}	Error reset (under user control)	Operating mode and ready status (App)	Out comparators and logic based switching signal cutoff (Hwr)	1-bit	α
State	F_{en}	Fan enable, active low	Operating mode and ready status (App)	Thermal management (Hwr)	1-bit	α
	C_{en}	Precharge, active high	Operating mode and ready status (App)	Precharge circuits (Hwr)	1-bit	α
	P_{dac}	Protection function setting selection (under user control)	Operating mode and ready status (App)	Comparator D/A for protection settings (Hwr)	2-bit	α
	P_{set}	Serial data for DAC	Operating mode and ready status (App)	Comparator D/A for protection settings (Hwr)	16-bit	1.25MHz
	T_{sel}	Channel selection bits for temperature measurement	Operating mode and ready status (App)	Temp meas MUX (Hwr)	3-bit	α

NOTE—α denotes signals that may be configuration related and occur at set-up or at infrequent intervals. The sampling rate at which these signals occur is dependent upon how fast the application needs to self-configure.

Table 9—Signals at application to converter layer interface (App-Cnv)

Signal type	Signal name	Interface signal description	Generating module (layer)	Utilizing module (layer)	Bit resolu-tion	Sampling or update rate
Meas	i_{mA}	Phase A line measured current	A/D converter (Hwr)	RDFT alg (App)	12-bit	12 kHz
	i_{mB}	Phase B line measured current	A/D converter (Hwr)	RDFT alg (App)	12-bit	12 kHz
	v_{AC}	ac voltage, phase A to C	A/D converter (Hwr)	Voltage trans (Cnv)	12-bit	12 kHz
	v_{BC}	ac voltage, phase B to C	A/D converter (Hwr)	Voltage trans (Cnv)	12-bit	12 kHz
	U_d	dc bus voltage	A/D converter (Hwr)	SVPWM (Swt) dc voltage contoller (App)	12-bit	12 kHz
	C_f	Precharge feedback	Auxiliary contact (Hwr)	A/D conv (Swt)	1-bit	12 kHz
	F_f	Fan feedback	Fan tach signal (Hwr)	Operating mode and ready status (App)	12-bit	12 kHz
	$temp_x$	Temp channel	IGBT module NPC (Hwr)	A/D conv (Swt) operating mode and ready status (App)	12-bit	12 kHz
Control	i^*_{cA}	Current reference	Waveform reconstruction algorithm (App)	Current controller A (Cnv)	32-bit	12 kHz
	i^*_{cB}	Current reference	Waveform reconstruction algorithm (App)	Current controller B (Cnv)	32-bit	12 kHz
	$S\omega_{1g}$	Synchronization signal	Synchronization (Cnv)	CPC decomposition algorithm (App) current reconstruction alg (App)	32-bit	12 kHz
	$C\omega_{1g}$	Synchronization signal	Synchronization (Cnv)	CPC decomposition algorithm (App) current reconstruction alg (App)	32-bit	12 kHz
	v_A	Transformed voltage signal	Transformation (Cnv)	Current reconstruction alg (App)	32-bit	12 kHz
	v_B	Transformed voltage signal	Transformation (Cnv)	Current reconstruction alg (App)	32-bit	12 kHz
	v_C	Transformed voltage signal	Transformation (Cnv)	Current reconstruction alg (App)	32-bit	12 kHz
	E_{res}	Error reset (under user control)	Operating mode and ready status (App)	Out comparators and logic based switching signal cutoff (Hwr)	1-bit	α
State	F_{en}	Fan enable, active low	Operating mode and ready status (App)	Thermal management (Hwr)	1-bit	α
	C_{en}	Precharge, active high	Operating mode and ready status (App)	Precharge circuits (Hwr)	1-bit	α
	P_{dac}	Protection function setting selection	Operating mode and ready status (App)	Comparator D/A protection settings (Hwr)	2-bit	α
	P_{set}	Serial data for DAC	Operating mode and ready status (App)	Comparator D/A for protection settings (Hwr)	16-bit	1.25 MHz
	T_{sel}	Channel selection for temperature measurement	Operating mode and ready status (App)	Temp meas MUX (Hwr)	3-bit	α

Signal type	Signal name	Interface signal description	Generating module (layer)	Utilizing module (layer)	Bit resolu-tion	Sampling or update rate
State	SIK	Set current controller gain Ts/Lc	System (Sys)	Dead-beat current controllers (Cnv)	16-bit	N/A
	RIK	Report current controller gain Ts/Lc	Dead-beat current controllers (Cnv)	System (Sys)	16-bit	N/A

NOTE 1—α denotes signals that may be configuration related and occur at set-up or at infrequent intervals. The sampling rate at which these signals occur is dependent upon how fast the application needs to self-configure.

NOTE 2—Rate not applicable (N/A). The data is intermittent system dependent data.

Table 10—Signals at system to application layer interface (Sys-App)

Signal type	Signal name	Interface signal description	Generating module (layer)	Utilizing module (layer)	Bit resolu-tion	Sampling or update rate
State	MStat	Operating mode and status	Operating mode and ready status (App)	System (Sys)	16-bit	N/A
	Mset	Operating mode set	System (Sys)	Operating mode and ready status (App)	16-bit	N/A
	SK_h	Set harmonic current gain	System (Sys)	Flexible compensation algorithm (App)	16-bit	N/A
	SK_r	Set reactive current gain			16-bit	N/A
	SK_u	Set unbalanced current gain			16-bit	N/A
	SK_a	Set active current gain			16-bit	N/A
	RK_h	Report harmonic current gain	Flexible compensation algorithm (App)	System (Sys)	16-bit	N/A
	RK_r	Report reactive current gain			16-bit	N/A
	RK_u	Report unbalanced current gain			16-bit	N/A
	RK_a	Report active current gain			16-bit	N/A
	SIK	Set current controller gain Ts/Lc	System (Sys)	Dead-beat current controllers (Cnv)	16-bit	N/A
	RIK	Report current controller gain Ts/Lc	Dead-beat current controllers (Cnv)	System (Sys)	16-bit	N/A
	SVK_p	Set K_p of voltage controller	System (Sys)	dc voltage controller (App)	16-bit	N/A
	SVK_i	Set K_i of voltage controller			16-bit	N/A
	SVK_d	Set K_d of voltage controller			16-bit	N/A
	RVK_p	Report K_p of voltage controller	dc voltage controller (App)	System (Sys)	16-bit	N/A
	RVK_i	Report K_i of voltage controller			16-bit	N/A
	RVK_d	Report K_d of voltage controller			16-bit	N/A
	SUdcmd	Set dc bus voltage setpoint	System (Sys)	dc setpoint (App)	16-bit	N/A
	RUdcmd	Report dc bus voltage setpoint	dc setpoint (App)	System (Sys)	16-bit	N/A

NOTE—Rate not applicable (N/A). The data is dependent data.

6.4 Implementation summary

6.4.1 System layer

The system control layer sets operating modes, receives status information, and sends control loop settings and set-points in the application and converter control layers. The system control layer communicates with lower layers through fiber optic Ethernet using the standard transmission control protocol/internet protocol (TCP/IP) for transportation of the data. Riding on the TCP/IP is the Application Protocol Data Unit

(APDU) utilizing the IEC60870 standard protocol. The communication between the system control layer and lower layers is asynchronous in that it depends on both network traffic and frequency of requests from the system control layer.

6.4.2 Application layer

The application control layer consists of several subsystems. These include the Operating Mode and Ready Status module, several modules that together comprise a reference signal generator, and a dc control loop to regulate the dc bus of the converter system. The reference signal generator blocks operate at the same sampling frequency as the converter control layer, which is 12 kHz. It accepts measurements and synchronization signals from lower layers and provides a current reference. The dc voltage controller is a simple PI feedback controller operating at a sampling rate of 1.2 kHz.

The system states provided below are managed by the application control layer "Operating Mode and Ready Status" module shown in Figure 6. State change requests shown in Table 7 are made from the system control layer, and the current state is reported to the system control layer.

System states definitions:

1) System pre-charge state:
   - Precharge contactor is opened
   - All insulated-gate bipolar transistor (IGBT) signals are turned off
   - System has no errors
2) dc voltage rising state:
   - Precharge contactor is closed
   - dc voltage control loop is in operation with active reference current limitation
   - System has no errors
3) Normal operation state:
   - Precharge contactor is closed
   - dc voltage control loop and current control loop are in operation based on system working mode
   - Fan is turned on
   - System has no errors
4) Error state:
   - All IGBT signals are turned off
   - Precharge contactor is opened
   - Fan is turned off

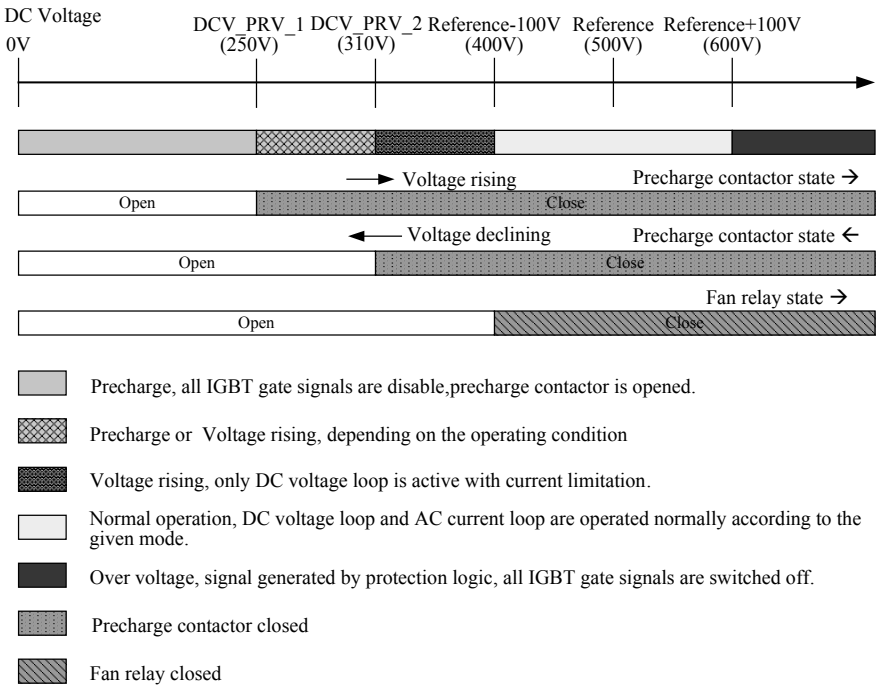


Figure 7—System state diagram

6.4.3 Converter control layer

The converter control layer consists of a synchronization module, voltage transformation module, and feedback control loops to regulate converter current such that it tracks the current references generated in the application control layer.

6.4.4 Switching control layer

The switching control layer consists of a SVPWM and switching logic and deadtime generator. The switching logic and deadtime generator is clocked at a rate of 125 MHz. The swiching logic clock provides a resolution of 8 ns or 5208 steps per half-period of the symmetrical aligned SVPWM with a switching frequency of 12 kHz.

6.4.5 Hardware control layer

The hardware control layer is a mixed analog and digital system. It contains both analog circuits such as the gate drivers, protection comparators, current and voltage sensors, etc., as well as digital circuits such as low level protection logic and the A/D converters. Only the digital subsystems of the hardware control layer are important with regard to the Swt-Hwr interface requirements.

The A/D converters have a 12-bit resolution and are sampled at a rate of 12 kHz. The data is transmitted as a 12-bit fixed-point number to upper control layers. However, at each receiving layer the data is converted into a 32-bit fixed-point number for use by other control subsystems.

The comparator logic for low level protection is clocked at a rate of 16 MHz in order to act on a protection signal as quickly as possible. This provides a 16.5 ns maximum time between detection of a fault and the blocking of all gate drive signals. However, it only receives inputs from the switching control layer. Therefore, the rate needed at the interface is determined by the switching logic and deadtime module in the switching control layer.

Annex A

(informative)

Interface Characterization

This Annex shows application examples that although not in accordance with the proposed architecture, are exercises for analyzing and quantifying the interface requirements including their frequency bandwidth. This analysis illustrates that the spatial and temporal partitions have commonality across various applications that, thereby, leads to the proposed architecture.

A.1 Interface characteristics classifications

When a system is partitioned, the partition interface should be designed to meet the performance requirements of different layers. In addition to the compatibility requirements, it is important to characterize the requirements on data volume and transmission rate. The interface study is carried out to define layer interfaces that facilitate the interconnection and integration of the complete control system.

For the purpose of partitioning, interface signals are classified in the following examples as:

a) Control and protection:
   1) Control commands (C): e.g., reference voltage (V_{ref}), reference current (I_{ref})
   2) Protection commands (P): variables generating protection actions, e.g., phase over-current
b) Measurements (M): e.g., voltage, current, temperature
c) State:
   1) Settings of the control system (S): e.g., maximum current (I_{max}), maximum voltage (V_{max})
   2) Start-up and self-check (T): e.g., gate driver ready
   3) System information (I): e.g., performance, system health, electronic prognostics

In principle, the format of the signals can be either analog or digital. Nevertheless, because a digital controller is assumed, the signals handled by the controller are digital. For the measurement signals, an A/D converter is directly coupled at the output of the measurement transducer converting the signals into digital type.

A.2 Interface requirements case study

There is a wide variety of power electronics applications in utilities, for example: DVR, STATCOM, SSTS, battery energy storage system (BESS), unified power flow controller (UPFC), static VAR compensator (SVC), and similar applications called by different names. The examples provide the data capacity and data resolution requirements without specifying the medium of transporting the data between the layers. In general, there are multiple communication protocols that could meet the data communication requirements.

A.2.1 Dynamic voltage restorer

There are some interface requirements that are independent of the control algorithm. For example, the required speed in the response of the DVR determines the minimum requirements for the bandwidth of the

voltage controller loop. However, some characteristics, like the number of signals to be handled, depend on the control algorithm selected for the application.

The analysis is based on the system configuration shown in Figure A.1. The four indicated interfaces are analyzed below. The details of the signals handled at each interface, denoted by the dotted lines, are shown in Table A.1. For the calculation of the capacity requirements, the following considerations are necessary:

The channel bandwidth (CB) requirement for the digital type signal is:

$$CB = N K_d f_{sam} n_x \tag{1}$$

where

N is the number of signals

K_d is the ratio of sampling period to transmission time,

f_{sam} is the sampling frequency

n_x is the number of bits representing the variable x

The bandwidth (BW) requirement for an analog type signal is:

$$BW = N \frac{f_{sw} 2^{n_d}}{\pi} \tag{2}$$

where

N is the number of signals

f_{sw} is the switching frequency

n_d is the number of bits representing the analog signal

Analog signals that are not directly related to the switching frequency may permit a lower bandwidth; in the quantification presented below, these signals are called analog b type.

Bandwidth, or channel bandwidth, is a measure of available or consumed data communication resources of a transmission channel, in bits/s or kbits/s or Mbit/s. Channel capacity is the maximum number of bits or other information elements (measured in bits) that can be handled in a particular channel per unit time. The bandwidth or the channel bandwidth must be equal to or less than the channel capacity.

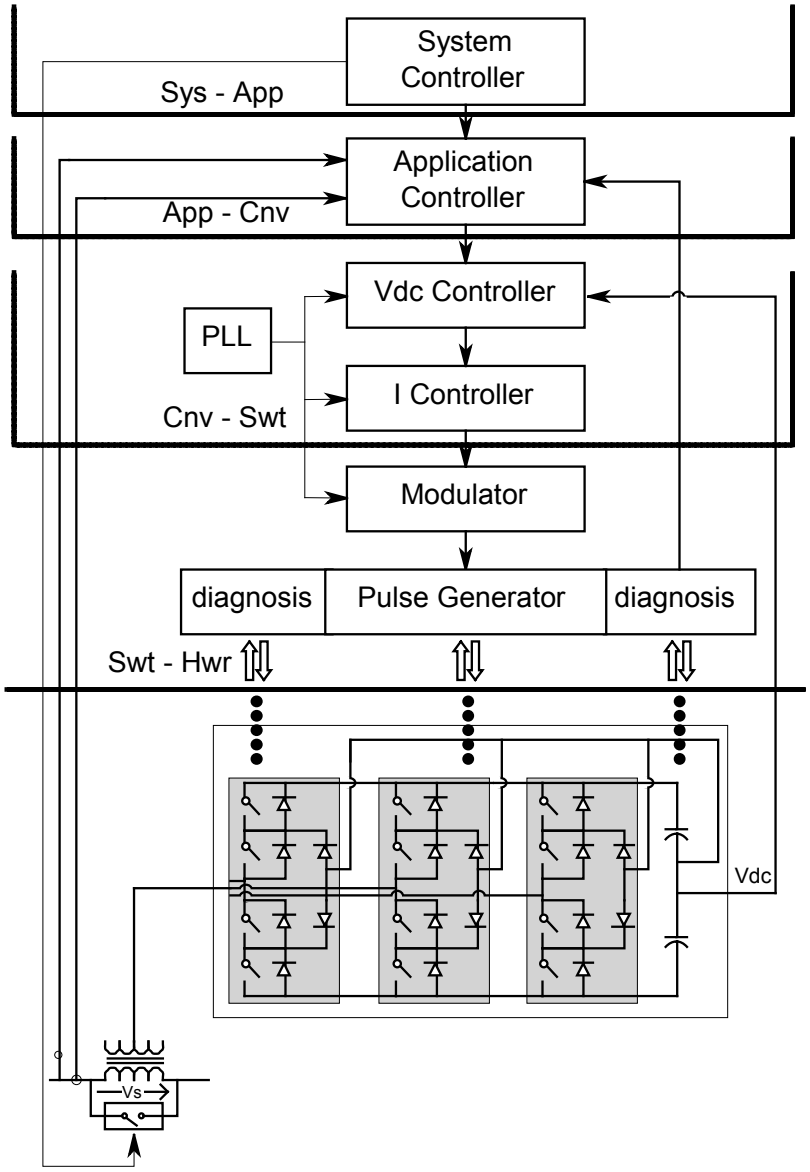


Figure A.1—DVR control system and interfaces

NOTE—The conversion between analog and digital may be located in the hardware or the switching control layer.

The numbers shown in Table A.1 were calculated considering values of f_{sw} = 2 kHz, K_d = 2, and the other parameters indicated in the table, with *nl* referring to the number of levels in the converter (two in this case). The sum of the values estimated for the interface Sys-App, App-Cnv, Cnv-Swt, and Swt-Hwr capacities are: 1.23 Mbit/sec, 9.34 Mbit/sec, 10.18 Mbit/sec, and 39.30 Mbit/sec, respectively. A large amount of the capacity requirement in the Swt-Hwr interface corresponds to the analog signals, which are confined inside the hardware control layer, while the digital representation of those measurements crosses the interface.

In general, the characteristics of a particular application determine the minimum requirements for the parameters of the signal handling. Thus, adopting a higher speed requirement enables many more applications to use the same interfaces. A 40 kHz sampling frequency produces a precision of less than one degree in a 50/60 Hz phase-locked loop (PLL), which should be appropriate. Bit resolution for measurements and other internal control variables were adopted according to standard values and are shown in Table A.1.

An interface analysis based on a modular partition of a power electronic system has already been described for a general case in Celanovic [B1]. This clause analyzes the case of a DVR system applying some concepts of that previous work.

Table A.1—Interface characteristics for the DVR system

Layer interface	Signal origin	Class[a]	Description	Name	# of signals (N)	Resolution (bits) (n_x)	Sampling freq (kHz) (f_{sqm})	Channel capacity[d] (Mbit/sec)
Sys-App	Sys	C	To Hwr layer: DVR bypass/discon.	Bypass discon.	1 1	Analog b[b] Analog b		0.055 0.055
		T	Operation mode	mode	1	14	40	1.12
Sys-App	App	C	Control/com. ready	P_{c2}	1	1	2	0.004
		S	External fault (bypass)	I_s bypass	3			
App-Cnv	App	C	Operation reference signals	V_{sdref}, V_{sqref}	2	14	40	2.24
App-Cnv	Cnv	M	ac measurements from Hwr layer	V_{ls}, I_s	2 x 3	14	40	6.72
		P	Overcurrent phase	$I_s$max, Imax	2 x 3	Analog b		0.33
		T	Ready signals from Swt layer, Cont/com. ready	I_{sr},V_{lsr} P_{c1}	2 x 3 3 x nb	1 1	2 2	0.024 0.024
Cnv-Swt	Cnv	C	3-ph duty cycles PLL angle signals	$D_{d,q}$ sinθ , cosθ	2 2	14 14	40 40	2.24 2.24
		P	PWM signal stop	PWM_{stop}	1	1	40	0.08
Cnv-Swt	Swt	M	ac meas. from Hwr layer	I, V_{dc}	3 + 2	14	40	5.60
		T	Ready signals from Hwr layer	I_r, V_{dcr}	3 + 2	1	2	0.02
		S	I loop limit, V loop limit	$I_d$max, $I_q$max, V_{sd}max, V_{sq}max,	2 2			
Swt-Hwr	Swt	C	Firing pulses (1 signal per switch)	$S_{1\text{-}6}$	6 x (nl-1) x nb	Analog		13.30
		C	From system controller: DVR bypass/discon.	Bypass discon.	1 1	Analog b Analog b		0.055 0.055
Swt-Hwr	Hwr	M	Module measurements: 3-phase I 3-phase converter V and I, V dc side	I V_s, V_{ls}, V_{dc}	3 2 x 3 = 6 1 x 2 = 2	14 14 14	40 40 40	3.36 6.72 2.24
		P	Device protection (1 signal/device)	Short	6 x nb x (nl-1)	Analog		13.30
		P	Overcurrent PEBB overvoltage dc side	No V_{dc}max	2	Analog b		0.11
		T	Gate drivers ready, sensors ready, control/com. ready	S_c I_r, I_{sr}, V_{lsr}, V_{dcr}, P_{c1}	6 x nb x (nl-1) 3 x 3 + 2 3 x nb	1 1 1	2 2 2	0.096 0.044 0.024
		S	V connection matrix	V(3x3)	9 x (nl-1)			

[a]Signal class: C- control, S- settings, P- protection, T- start-up and self-test, M - measurements, I - system information.

[b]Analog signals that are not directly related to the switching frequency may permit a lower bandwidth; in the quantification presented, these signals are called analog b type.

[c] nl = number of levels in the converter; nb = number of branches.

[d]Channel capacity is the maximum number of bits or other information elements (measured in bits) that can be handled in a particular channel per unit of time.

A.2.2 STATCOM

The STATCOM control diagram is shown in Figure A.2. In this example, a PEBB is based on an H-bridge. The controller configuration corresponds to a general-purpose regulator with the specific control actions defined at the system controller layer. Those specific characteristics also will define the required measurements that need to be processed at the system controller. The load controller working principle is based on the general guidelines presented in Daeler et al. [B4], and the H-bridge configuration for a STATCOM was described in Liang et al. [B19].

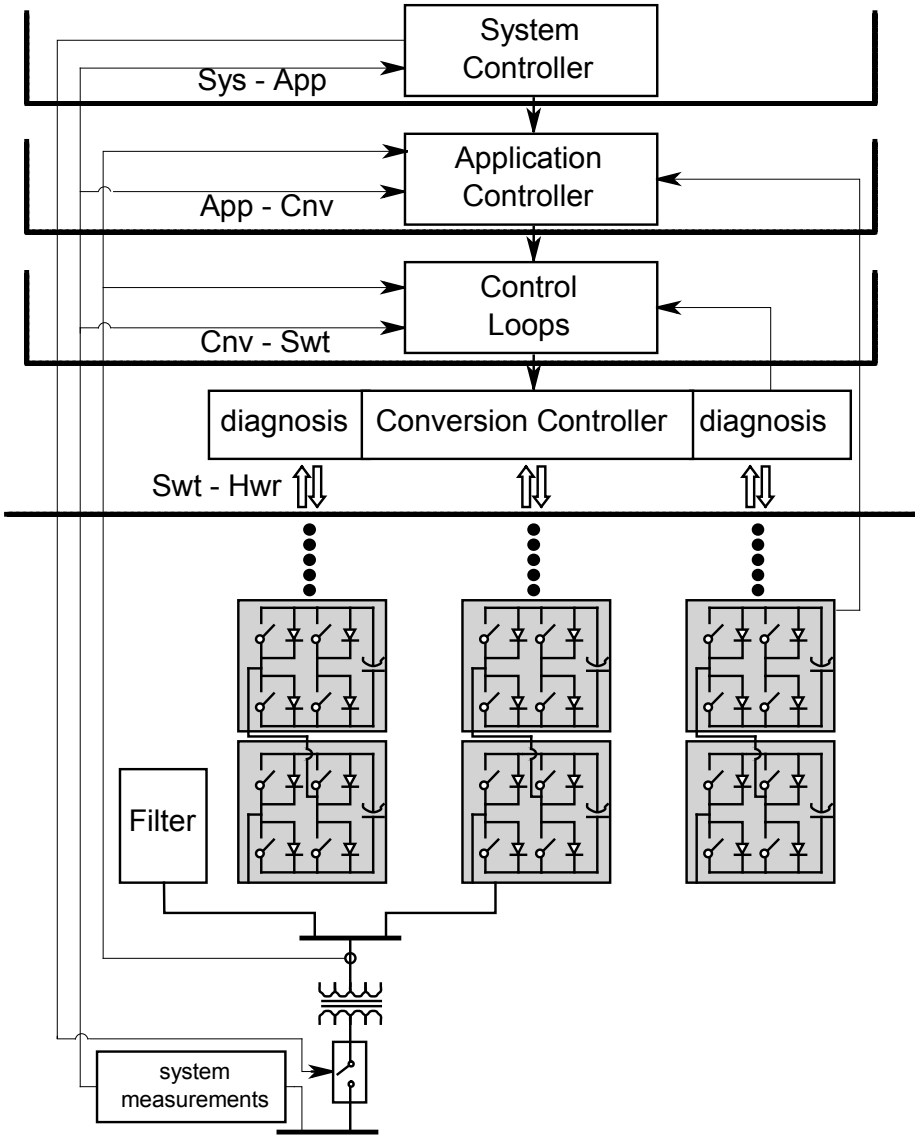
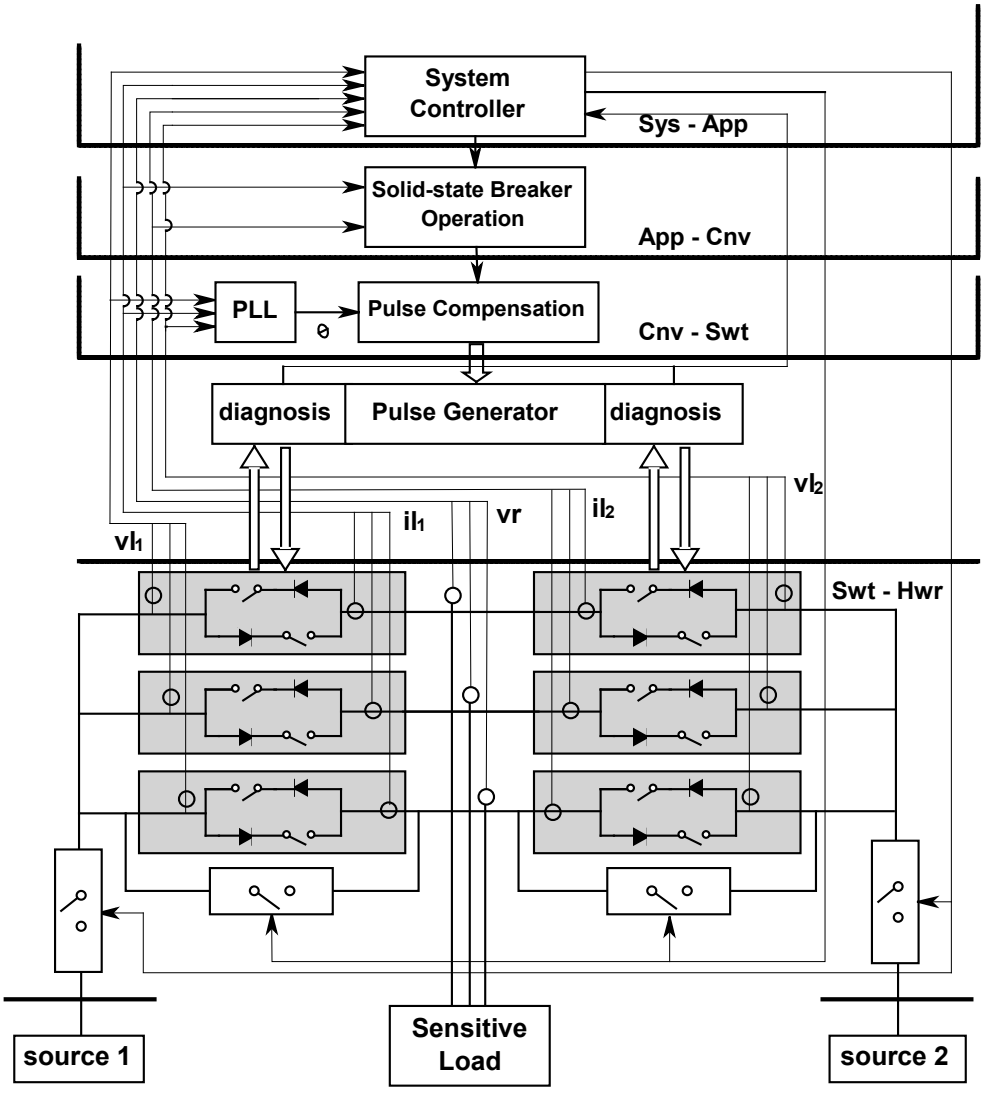


Figure A.2—STATCOM control system and interfaces

The number of H-bridge blocks connected in series to achieve the desired final voltage of the STATCOM varies according to the voltage at the connection point. In the case under analysis, sixteen H-bridges are connected in series in each of the three phases. The calculation of the different interface capacities was done using the same parameters as in A.2.1.

A.2.3 Solid State Transfer Switch (SSTS)

Figure A.3 shows the simplified block diagram of an SSTS configuration (see Scwartzenberg et al. [B22]). In this case, the power cell subsystem should be able to isolate the voltage source from the load. Therefore, the basic switch-cell is different from the previously analyzed voltage source-based configurations. The switch operation also is different since the duty cycle has only two possible values: zero and one. In this way no pulse width modulator (PWM) signal is required. The number of branches, usually two, depends on how many sources the system relies on for improving the availability. The required local control functions are relatively simple once the system controller has made the decision for line connection/disconnection and is reflected in a reduced set of functions at lower control layers. Although the sampling frequency requirements are not high, 40 kHz was used as in the other examples above.



a)

Figure A.3—Transfer switch control system and interfaces

A.3 Analysis of results

The calculation for the three given examples was done in the same way as shown in Table A.1. Because the H-bridge-based STATCOM uses a large number of H-bridges per phase, first the calculation was done considering only one H-bridge in each phase. These results for the total interface capacity requirements are

summarized in Figure A.4. In this figure, it is possible to observe the same pattern in the capacity requirements for the three different applications if only the one H-bridge per phase STATCOM is considered. There is a difference for the STATCOM with multiple H-bridges per phase.

Before calculating the total capacity for the STATCOM case, it is better to discuss the partition and the location of the interfaces of the control system in the previously mentioned hierarchy. Figure A.5 shows the detailed block diagram of the STATCOM control system.

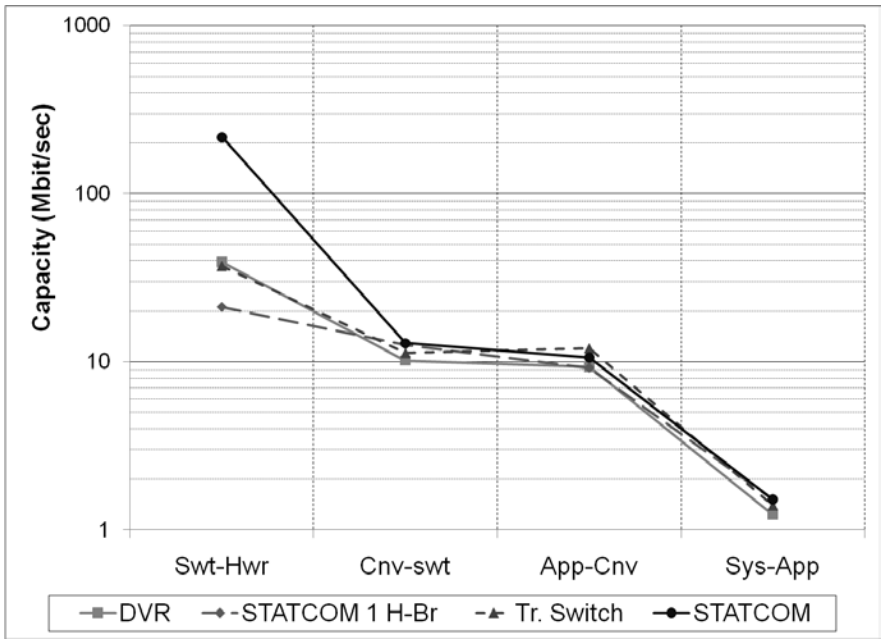


Figure A.4—Total capacity requirements at the four layer interfaces

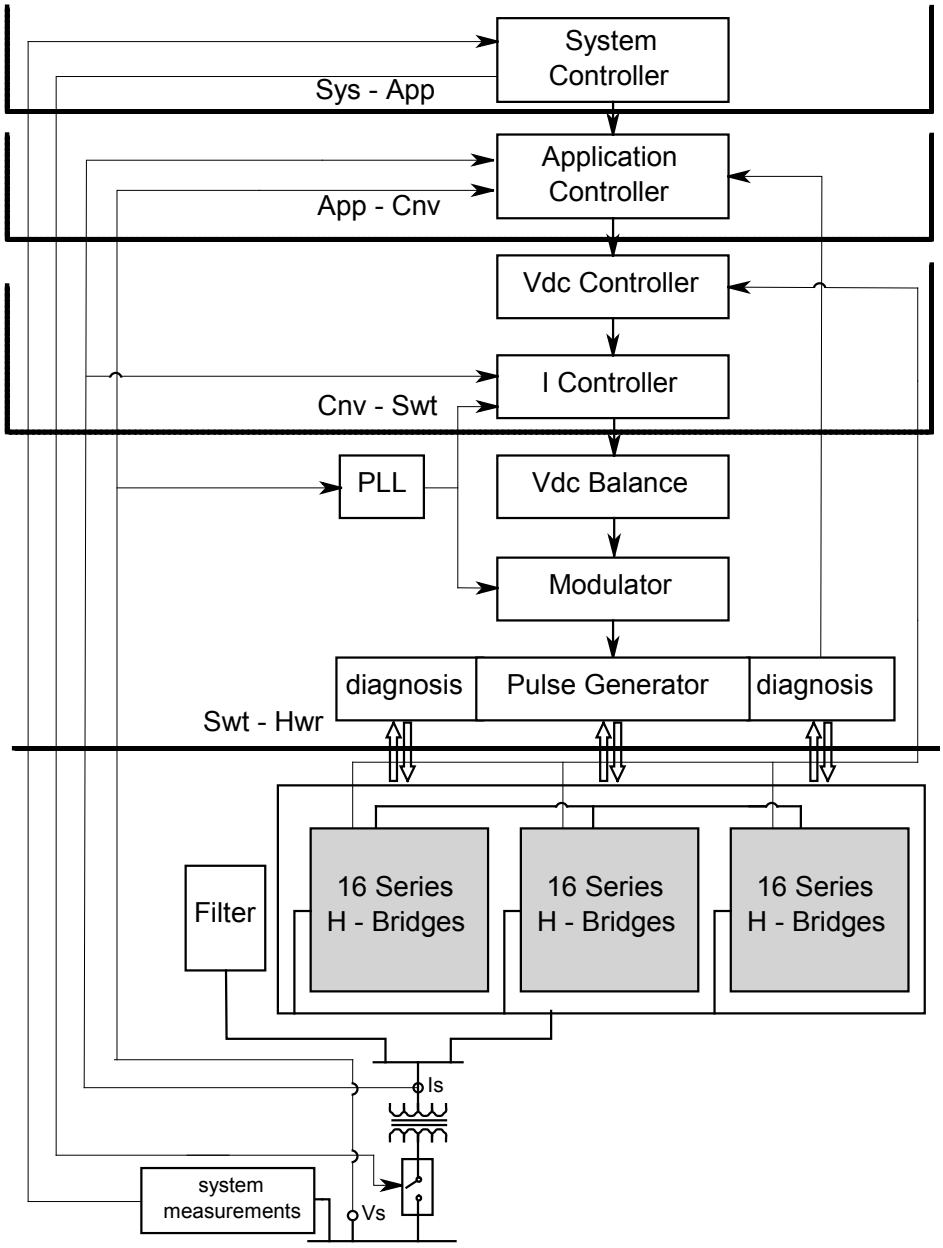


Figure A.5—STATCOM control system and interfaces

The Cnv-Swt interface could be placed just between the Modulator and the Pulse generator. However, the series connection of the H-bridges requires a voltage balancing function. Otherwise, the voltage will become unevenly divided among all the connected H-bridges. This control function works by adjusting the firing angle of each of the devices in the H-bridges at each phase. Therefore, it is more reasonable to place the Cnv-Swt interface as shown in Figure A.5 instead of between the Modulator and the Pulse generator. With this consideration Figure A.4 shows the results for all the analyzed systems.

The interface quantification showed that the larger capacities are required by the analog communications, which are usually close to the power hardware subsystem and can be integrated within the hardware control layer. In that sense, the layered architecture concept simplifies the communication and data transmission inside the power electronics system by reducing the interface requirements between different control layers. Fundamentally, this occurs because the A/D converters are located in the hardware control layer and the high bandwidth analog signals no longer cross the any interface (see Figure 6).

The requirements for digital communication are shown in Figure A.6. From the analysis, it is possible to observe that the major capacity requirements are required at the Swt-Hwr interface, both for analog and digital communication types. Figure A.4 and Figure A.6 show rather high capacity requirements at the Swt-Hwr interface for the STATCOM in relation to the other cases because the STATCOM is a high-voltage, high-power version with many H-bridges in series. Nevertheless, if the repetitiveness given in the STATCOM case is not considered, the digital capacity requirements remain almost constant for the interfaces.

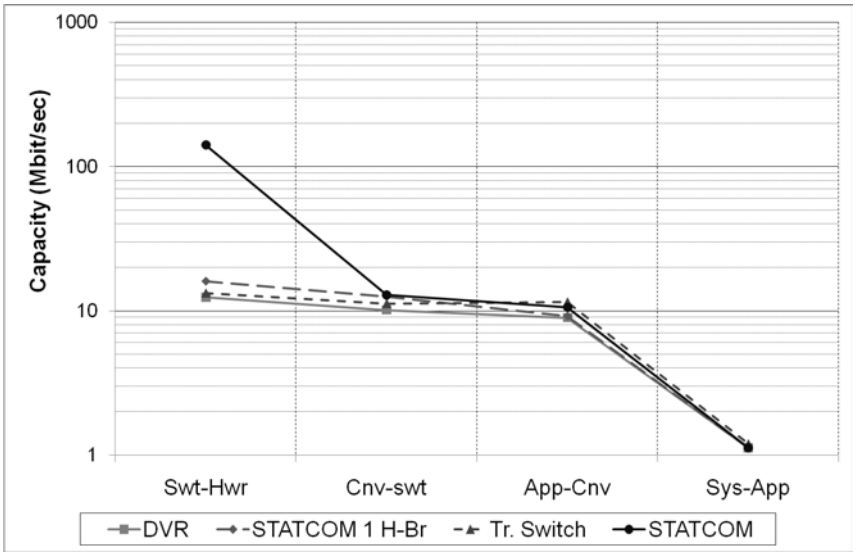


Figure A.6—Digital capacity requirements at the four layer interfaces

Annex B

(informative)

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