Carrier Lifetime Control in Power Semiconductor Devices

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Abstract— This paper surveys the present technology of carrier lifetime control in power semiconductor devices by controlling recombination centre types and concentration. The correlation of lifetime with device properties such as on-state voltage drop, off-state leakage current and switching times of bipolar devices has been elucidated. Various techniques for preserving or reducing lifetime during semiconductor device fabrication are presented. Advantages, problems and some limits of individual techniques are discussed.

***Index Terms*—Charge carrier lifetime, power semiconductor devices, semiconductor device fabrication**

I. Introduction

All important characteristics of bipolar devices, i.e. diodes, transistors, thyristors, IGBTs and also integrated structures depend on the excess carrier lifetime. Bipolar devices of the same geometry but with different excess carrier lifetime have different on-state and dynamic characteristics. For high voltage devices, such as diodes, thyristors and IGBTs, a long carrier lifetime is desirable, in order to keep on-state losses acceptably low. On the other hand, devices required to operate at high frequencies need the carrier lifetime to be short, in order to obtain fast turn-off and to minimise the reverse recovery charge. In the case of silicon devices, excess carrier lifetime is mainly controlled by local recombination centres creating deep energy levels in the gap [1] until the current density reaches a level of the order of 10^3 A/cm^2, when Auger recombination becomes significant [2]. In the ranges of current density normally experienced, carrier lifetime is inversely proportional to the concentration of the recombination centres: $\tau \sim N_t^{-1}$.

II. Recombination Via Local Centres

The theory of carrier generation and recombination via local centres is usually referred as the Shockley-Read-Hall theory [3], [4] ,[5]. During the recombination process, electron hole pairs recombine through deep level impurities, characterised by the impurity concentration N_t, energy level $-W_t$ in the bandgap and capture cross-sections σ_n and σ_p for electrons and holes, respectively. For a single deep donor level, recombination rates are given by

$$R_{\mathrm{n}} = -\frac{\mathrm{d}\Delta n}{\mathrm{d}t} = v_{\mathrm{th,n}}\sigma_{\mathrm{n}}\left(nN_{\mathrm{t}}^{+} - n_1 N_{\mathrm{t}}^{*}\right), \qquad (1)$$

$$R_{\mathrm{p}} = -\frac{\mathrm{d}\Delta p}{\mathrm{d}t} = v_{\mathrm{th,p}}\sigma_{\mathrm{p}}\left(pN_{\mathrm{t}}^{*} - p_1 N_{\mathrm{t}}^{+}\right), \qquad (2)$$

where v_{thp} and v_{thn} are thermal velocity of holes and electrons, N_t^+ is ionised centre concentration, N_t^* is neutral centre concentration, n_1 and p_1 are concentrations of electrons and holes if the Fermi level is identical with the centre energy level, i.e. $p_1 = N_v \exp[-(W_g - W_t)/kT]$, and $n_1 = N_c \exp(-W_t/kT)$. Similar relations could also be derived for a case of a single acceptor level.

In order to maintain the dynamic equilibrium, electroneutrality conditions must be kept. Assuming that the concentration of the centres is much lower than equilibrium majority carrier concentration ($N_t << n_0+p_0$), $R_n = R_p$ and the carrier lifetime is given by

$$\tau = \tau_{p0}\frac{n_0 + n_1 + \Delta n}{n_0 + p_0 + \Delta n} + \tau_{n0}\frac{p_0 + p_1 + \Delta n}{n_0 + p_0 + \Delta n}, \qquad (3)$$

where n_0 and p_0 are concentration of electrons and holes in thermodynamic equilibrium, Δn ($\Delta n = \Delta p$) is excess carrier concentration, $\tau_{p0} = (v_{thp}\sigma_p N_t)^{-1}$ and $\tau_{n0} = (v_{thn}\sigma_n N_t)^{-1}$.

Bipolar power semiconductor devices usually operate in a switching mode. When turned on, the internal layers are flooded with excess carriers under high injection conditions. Low injection conditions can be connected with very low current densities only. When turned off, a thick depleted layer develops at the blocking PN junction.

Under high injection conditions ($\Delta n >> n_0 + p_0$ and $\Delta n >> N_t$) the high injection carrier lifetime τ_H is given by

$$\tau_{\mathrm{H}} = \tau_{\mathrm{n0}} + \tau_{\mathrm{p0}} = \frac{1}{N_t}\left(\frac{1}{v_{thn}\sigma_n} + \frac{1}{v_{thp}\sigma_p}\right) \qquad (4)$$

It is now independent of the energy level of the centre, and depends only on centre concentration N_t and the capture cross-sections..

In depleted layers, deep level centres cause carrier generation. the generation rate, G, is given by

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$$G = \frac{n_i^2}{\left(n_1 \tau_{p0} + p_1 \tau_{n0}\right)} = \frac{n_i}{\tau_{sc}}, \qquad (5)$$

where the carrier lifetime in the space charge region

$$\tau_{sc} = \tau_{p0} \exp\left(\frac{-\left(W_i + W_t\right)}{kT}\right) + \tau_{n0} \exp\left(\frac{\left(W_i + W_t\right)}{kT}\right) \qquad (6)$$

depends on the position of the trapping energy level W_t with respect to the position of the Fermi level in undoped semiconductor W_i and, it is shortest when W_t and W_i coincide.

Recombination centres in silicon are created by both heavy metal impurities and point defects, and each type of centre has its own characteristic energy level and carrier capture cross section. The resulting carrier lifetime is determined by the total set of recombination centres present.

III. Influence of Carrier Lifetime on Device Characteristics

Recombination centres influence all device characteristics, both off-state blocking characteristics and on-state characteristics and transient characteristics during turn-on and turn-off processes.

Off-state characteristics of all type of devices (including MOSFETs) are characteristics of a reverse biased PN junction. Therefore, the characteristics are influenced by the thermal generation of electron-hole pairs in the space charge layer [6]. The additional current density that flows through the junction as a result of this process is known as the *generation-recombination* current. It depends on the magnitude of the reverse bias voltage through the width of the depletion layer, d, and may be expressed as

$$J_{gr} = e\int_0^d G\,\mathrm{d}x = \frac{e n_i d}{\tau_{sc}} \qquad (7)$$

The total current density, J_R, flowing across a reverse-biased junction is given by the sum of J_0 and J_{gr}:

$$J_R = n_i^2 e\left(\frac{D_n}{L_n}\frac{1}{p_{p0}} + \frac{D_p}{L_p}\frac{1}{n_{n0}}\right) + \frac{e n_i d}{\tau_{sc}} \qquad (8)$$

To keep the reverse current low enough, it is necessary keep a high generation carrier lifetime τ_{sc}. As follows from analysing (6), the energy levels should differ considerably from the position of the Fermi level in intrinsic material W_i, preferably out of the central part of the band-gap, as indicated in Fig.1.

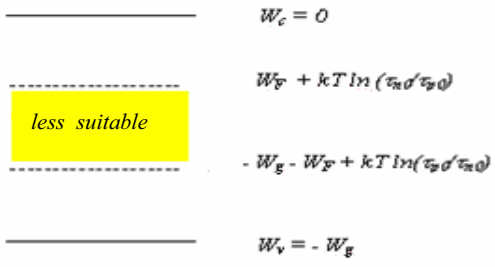

Fig. 1. Energy level scheme with indication of position deep levels less suitable for carrier lifetime control from the viewpoint of influencing reverse characteristics

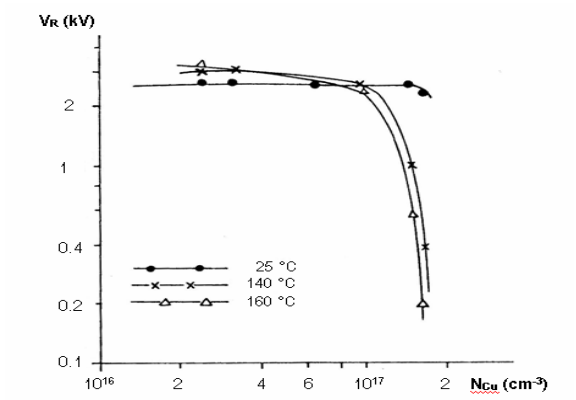

Fig.2. The influence of Cu concentration on reverse characteristics of power diodes

Some impurities may (at higher concentrations) create clusters of intermetallic compounds with silicon that may cause deterioration of reverse characteristics, as demonstrated in Fig.2 by the influence of Cu concentration on the reverse voltage of silicon power diodes [7]. Similar behaviour can also be found in the case of silver, palladium, if the concentration exceeds a critical level. More details about impurities in silicon can be found in [8], [9], some remarks on problems of recombination centres in high voltage devices can be found in [10].

On-state characteristics of bipolar devices depend strongly on carrier lifetime (high injection carrier lifetime (4), because high injection conditions are connected with the device on-state). With decreasing carrier lifetime the excess carrier concentration decreases and consequently, the on-state voltage drop increases [2],[11]. An example of the relations between forward voltage drop and carrier lifetime for power diodes is shown in Fig.3. Therefore, long carrier lifetime is desirable from this viewpoint. A maximum "acceptable" voltage drop is marked with a dashed line. From this it the minimum carrier lifetime for particular device thickness can be found.

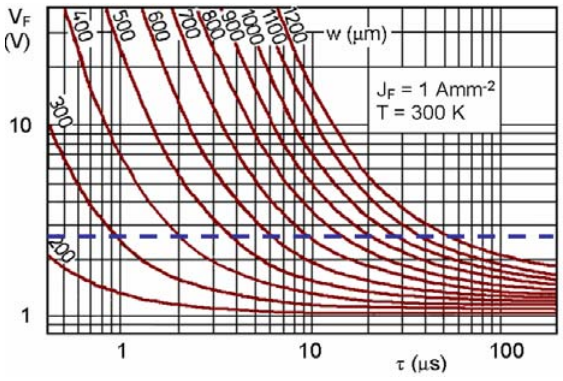

Fig.3, Theoretical dependences of the forward voltage drop across a p^+in^+ power diode on carrier lifetime, with the thickness of the i-region as a parameter [11].

Transient characteristics. For switching devices, short turn-on and turn-off times are desirable. Especially, turn-off time strongly depends on carrier lifetime, because the space charge region at the PN junction can build up after decreasing carrier concentration to the thermodynamic equilibrium value [2], [11], [15]. As shown in [10], during transient processes in power semiconductor devices high injection lifetime (4) should be considered. From this point of view, a very short carrier lifetime is desirable for fast switching devices. On the other hand, reducing the carrier lifetime can result in a deterioration of the on-state current-voltage characteristic. Therefore, a good trade-off of all the construction and technology should be made.

From this we can derive some demands on recombination centres suitable for carrier lifetime control:

- it should not create a deep energy level close to the middle of the bandgap
- it should not create intermetallic compounds with silicon
- the centre concentration should be easily controlled
- it should have a capture crosssection that is large and independent from temperature.

Recombination centres should be homogeneously distributed over the large-area power devices in order to avoid local overloading under static or dynamic conditions [12].

Some recombination centres used for carrier lifetime control are shown diagrammatically in Fig. 4.

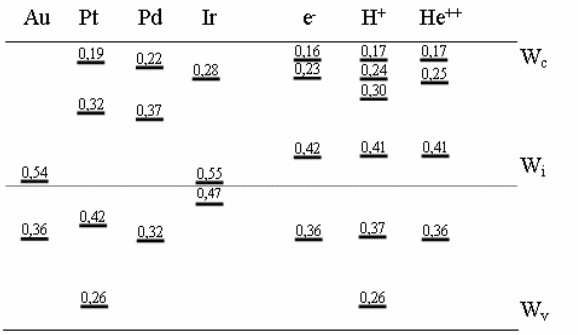

Fig. 4. Localised energy levels, within the silicon bandgap suitable for carrier lifetime control

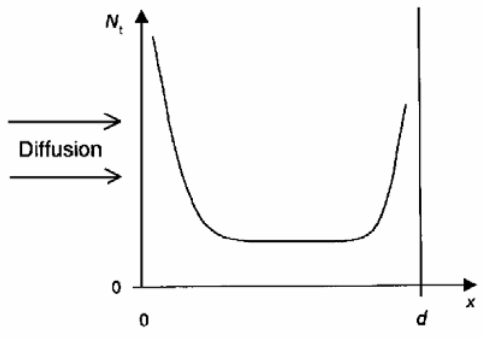

Fig.5. U-shaped diffusion profile of deep impurities used for lifetime reduction

IV. Techniques for Obtaining Long Carrier Lifetimes

In the as-grown single crystal silicon, the carrier lifetime can be as long as 1 ms. However, during high temperature processing, lattice defects are generated in the volume of the silicon wafers. Point defects creating recombination centres can originate locally in areas with higher internal stress or dislocation density even if the diffusion processes are carefully controlled. In addition, due to chemical activity of the silicon surface, some heavy metals like Fe, Cu, Au, etc., can be adsorbed (e.g. during wet chemical processes) and can diffuse in the silicon wafer during any subsequent high-temperature process

[8],[13],[14]. In such cases, recombination centres are created and the carrier lifetime is shortened. Possible sources of unwanted contamination include:

- residual surface impurities from the lapping and polishing operations,
- contamination adsorbed from chemicals used in the etching and cleaning processes,
- impurities from quartz tubes and boats.

In order to prevent this contamination, very pure (electronic grade) chemicals are used for cleaning the silicon, the diffusion sources, gases, diffusion tubes and boats used are all of the highest purity, and good environmental control is maintained. The concentration of lattice defects can be minimised by cooling the wafers slowly (at a rate not exceeding about 1°C/minute) after the final high-temperature process. This is particularly effective after phosphorous diffusion, when the surface is covered with a layer of phosphosilicate glass (PSG).

The types of metallic impurity that create deep trapping levels normally diffuse rapidly in silicon by the interstitial-substitution mechanism. That is, they migrate through interstitial positions and become substitution either by filling a lattice vacancy or by replacing a silicon atom (the “kick-off” mechanism). They diffuse to the surface covered with the PSG layer where they form compounds either with the glass or in the n^+-layer under the glass. A similar effect occurs after boron diffusion when the p^+-surfaces are covered with borosilicate glass.

This is known as *gettering*, which is a powerful technique for reducing the concentration of defects and impurities in critical regions [14]. Another method of gettering is to create mechanically damage (for example, by grinding) on the silicon surface on one side of the wafer. The trapping impurities quickly diffuse to occupy the vacancies created underneath the damaged layer. Using these techniques individually, or in combination, it is possible to fabricate devices with carrier lifetimes exceeding one hundred microseconds, even after high-temperature processing operations. This is especially important in the fabrication of high voltage thyristors and diodes.

Unfortunately, dislocations and impurity sources are not distributed homogeneously on a wafer area. Consequently, a non-uniform distribution of carrier lifetime in large-area wafers can originate in this way [13] ($\tau_{0max} > \tau_0 > \tau_{0min}$). For homogenisation, it is necessary to minimise the concentration of randomly created centres to a level $N_t(x;y) < N_{tM} \sim 1/\tau_0$ (clean processes, gettering, etc.) and then to introduce homogeneously recombination centres of higher concentration related to carrier lifetime τ_{in} . The resulting carrier lifetime will be in the interval

$$\frac{\tau_{in}}{1+\tau_{in}/\tau_{0\max}} \geq \tau \geq \frac{\tau_{in}}{1+\tau_{in}/\tau_{0\min}} \qquad (8)$$

From that follows, that for homogenisation a high ratio τ_{0min}/τ_{in} is desirable.

V. Techniques for Reducing Carrier Lifetimes

In many other circumstances, especially for devices operating at higher frequencies, it is important to reduce the carrier lifetime in a controlled and predetermined manner and so to control critical parameters such as the recovered charge and the turn-off time. In devices, where soft reverse recovery is desirable, a suitable axial carrier lifetime gradient can improve the voltage waveforms during the turn-off process [16] (axial carrier lifetime control [17]).

In power device fabrication technology, the carrier lifetime is reduced by introducing efficient recombination centres either by the diffusion of metallic impurities such as gold [18] and platinum [19], or by high energy irradiation. In either case, this is usually one of the last steps in the processing sequence.

A. Diffusion techniques,

Carrier lifetime reduction by gold diffusion has been used for more than 40 years. Gold diffusion [18] is generally performed between 800 and 1000 °C by coating the wafers with a thin evaporated or sputtered Au film or with an $AuCl_3$ solution. Gold diffuses rapidly in silicon by the interstitial-substitution mechanism and gives rise to concentration profiles very different from erfc or Gaussian profiles impurities like B, P, Al, As or Ga. The resultant doping profiles are U-shaped, as shown in Fig.5 with a high impurity concentration at both surfaces of the wafer and a flat plateau in the middle.

A disadvantage of gold as a recombination centre is that the dominated deep energy level is very close to the middle of the band-gap., as shown in Fig.4. Therefore, the leakage current is very high in gold-doped devices. Platinum is an alternative [19]. Because the platinum energy levels lie further from the middle of the band-gap, as shown in Fig. 4, the leakage current is reduced. For platinum coating, the wafers are coated with spin-on paints.

Some further alternatives that can be used for carrier lifetime reduction by diffusion technology are Pd and Ir. Palladium has a very high diffusion coefficient even at temperatures over 600°C and a considerable carrier lifetime reduction may be realized by Pd diffusion at 700°C [20]. Energy levels created by Pd diffusion [21] are also shown in Fig. 4. Iridium has a much lower diffusion coefficient than Au or Pt and is also an impurity that generates recombination centres [22]. It may, therefore, be suitable for setting up a concentration gradient of trapping levels suitable for fabricating soft reverse recovery diodes and thyristors [22] [23]. Nevertheless, application of the Ir diffusion for high voltage devices is limited by the thermo-donor origin.

Although the diffusion of lifetime reducing impurities is straightforward and does not require precise control, it may occur preferentially in regions of higher defect density and this may result both in non-uniform carrier lifetime distribution and hot spot formation. An example of inhomogeneous gold distribution after gold diffusion is shown in Fig.6.

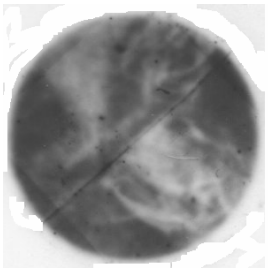

Fig.6. An example of inhomogeneous distribution of gold in silicon wafer after diffusion

Therefore, for precise carrier lifetime control in voltage controlled devices ion implantation and subsequent diffusion of Pt or Au can be used [24].

As the diffusion of lifetime reducing impurities has to be performed before metallisation, the device characteristics cannot be checked before and after doping.

B. Irradiation techniques

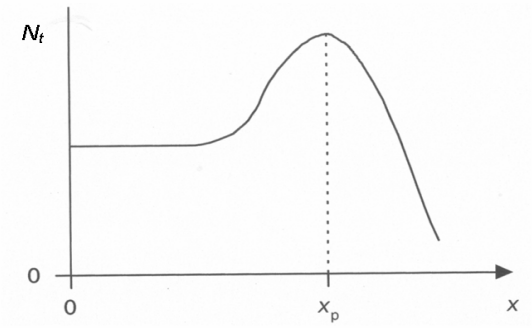

Fig.7. A schematic illustration of crystal lattice damage with depth following high particke irradiation

High-energy particles penetrate the crystal lattice, losing their energy in interactions with the lattice atoms which become displaced from their normal position and create defects [25]. These include vacancies, di-vacancies, impurity-vacancy pairs, interstitials and impurity-vacancy-interstitial complexes, all of which introduce recombination centres into the silicon. Electron, proton, alpha and gamma radiation can be used in this way to influence the carrier lifetime[26]. Deep levels created by irradiation are shown in Fig.4. A schematic illustration of the distribution of crystal lattice damage with depth following high energy particle irradiation is shown in Fig.7. The figure shows a typical variation of defects with depth below the surface of the defect concentration. The depth x_p of the peak value (the penetration depth) is a function of the particle mass and energy. For a given energy, the penetration depth is approximately in inverse proportion to the particle mass. There is most radiation damage at the end of the particle range, as illustrated in Fig.7. Some of the defects created by irradiation are unstable and can be annealed out at temperatures close to the working temperatures of the devices. As this can lead to undesirable changes in parameters, devices are

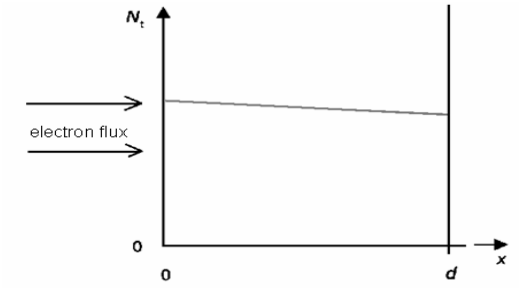

Fig.8. Distribution of recombination centres created by high energy electron irradiation

annealed at 250ºC to 300ºC for up to several hours after irradiation, to ensure long term operational stability.

Gamma radiation is able to penetrate very deeply, allowing the carrier lifetime in metallised and encapsulated devices to be modified. However, this can damage the p-n junction surface termination and degrade its reverse blocking characteristics.

Electron irradiation is commonly used. After metallisation but before encapsulation, devices are bombarded with electrons of several MeV energy. These penetrate the silicon to a depth of several mm (e.g. >6 mm for 3 MeV electrons) and create defects quite homogeneously through the device structure, as indicated in Fig.8. The concentration of deep levels is proportional to the radiation dose Φ applied, so the carrier lifetime [26] depends on the radiation dose as

$$\tau = \frac{\tau_0}{1 + \tau_0 K \Phi}, \qquad (9)$$

where τ_0 is carrier lifetime before irradiation and K is assumed to be a damage factor. The reproducibility of the process is excellent because the dosage can be monitored accurately.

Electron irradiation is often used for homogenisation of carrier lifetime distribution in large-area devices. Fig.9. shows an example of the change in carrier lifetime distribution with the electron irradiation measured on structures of reverse blocking GTO (the static method [27] was used). With the irradiation dose applied, the carrier lifetime decreases according to (8) and the carrier lifetime dispersion becomes lower. On the other hand, homogeneous distribution of carrier lifetime in the device volume may be not optimal for a trade-off of dynamic and static parameters. High radiation doses deteriorate the parameters of voltage controlled devices (power MOSFETs and IGBTs) [28].

Proton and alpha irradiation. Protons [29] have a much shorter penetration depth than electrons. This varies, as a function of the particle energy, from a few to several hundred microns. Irradiation with alpha particles [30], ions of He^{++}, causes similar effects to proton bombardment. Because their mass is greater, higher particle energies (typically ~10 MeV) are needed to give the same penetration depth. Proton and He^{++} penetration depth in silicon as a function of energy are shown in Fig.10. An increase in radiation damage at the end of the range allows a well-defined thin layer of reduced lifetime to be created at a depth below the surface that is controlled by the bombardment energy [31]. In this way, the trade-off between the static and dynamic parameters of bipolar power devices can be optimised. The trapping levels that mainly arise from vacancy complexes but also from implanted hydrogen are shown in Fig.4.

.Both proton and alpha irradiation have to be performed under vacuum with the result that equipment costs are high. However, these techniques can shorten the carrier lifetime in a well determined part of the device structure and they are used as a very powerful tool for device parameter trade-off. The use of this technique for high voltage devices is limited by the shallow doping [32] introduced by both hydrogen and helium, which can have

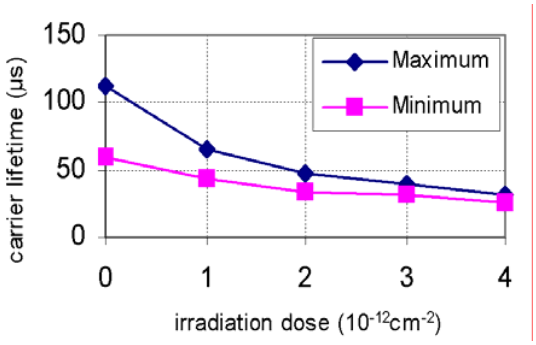

Fig.9. An example of the change of carrier lifetime dispersion in dependence on electron irradiation dose

a detrimental influence on the blocking voltage of power devices if high irradiation fluencies or wrong annealing conditions are chosen.

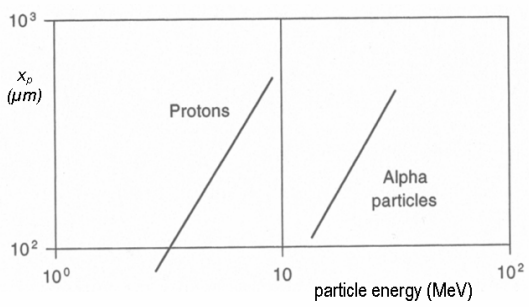

Fig.10. Penetration depth of H^+ and He^{++} ions in crystaline Si as a function of energy

C. Combination of techniques

To obtain special profiles of recombination centres, the techniques discussed above can be combined. It is possible to combine light ion (H^+ or He^{++}) irradiation with electron irradiation to suppress the dynamic avalanche during fast reverse recovery of power diodes. A change in profiles of fast diffusing metal impurities by high energy particles irradiation preceding the diffusion was suggested in [33]. Local lifetime control using platinum diffusion after light ion irradiation was studied in [34], and local lifetime control using palladium diffusion enhanced by radiation defects was used in [35]. These methods bring new tools for improving recombination centre profile and consequently, device parameters and reliability.

VI. Conclusion

Carrier lifetime tailoring is very important for obtaining an optimum combination both static and dynamic parameters. This paper reviewed some of classical and advanced methods of carrier lifetime control that can be used for both prolongation and shortening carrier lifetime. Possibilities of reaching homogeneous or construction specific carrier lifetime distribution in the device structures have been discussed.

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