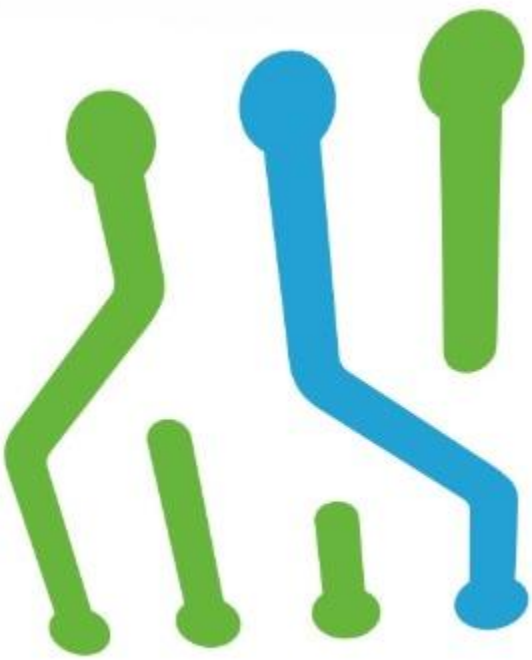


ICpedia Internship

Internship Final Project

Islam Nasser

EXCUSE

I sincerely apologize for the delay in delivering the project. Unforeseen technical issues beyond my control caused the delay. I understand the importance of timeliness and I'm committed to ensuring this doesn't happen again in the future. Thank you for your understanding.

Introduction

We have the "wbqspiflash" design, and we want to perform RTL2GDSII flow (logic synthesis and proceed through physical synthesis steps).

Target: We want to have a minimum area with maximum performance also we want to sell the chip, so we don't trap with high frequency and the chip don't operate.

SYNTHESIS MODIFICATIONS:

1- Input and output delay: I made it 0.55 from clock cycle to the neighboring block (0.05 from clock to routing between ports and 0.5 to the adjacent block)

Note → (the IP will put in chip and should take in consideration the timing with adjacent blocks)

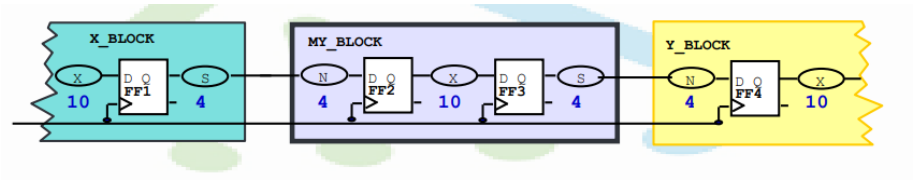


Figure 1:Time budgeting

Note → I left 0.05 to routing and the adjacent block will be left the same to have 0.1 from clock to routing and that enough as it is old technology (routing delay is small and not dominant)

The parameter control input and output delay is IO_PCT you can find in configurations/synthesis.tcl.

```
27 set ::env(SYNTH_ADDER_TYPE) "YOSYS"
28 set ::env(CLOCK_BUFFER_FANOUT) 16
29 set ::env(SYNTH_READ_BLACKBOX_LIB) 0
30 set ::env(SYNTH_TOP_LEVEL) 0
31 set ::env(SYNTH_FLAT_TOP) 0
32 set ::env(IO_PCT) 0.55
33 set ::env(SYNTH_EXTRA_MAPPING_FILE) ""
34
```

Figure 2: configurations/synthesis.tcl

```
 9
10 set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
11 set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
12 puts "\[INFO\]: Setting output delay to: $output_delay_value"
13 puts "\[INFO\]: Setting input delay to: $input_delay_value"
14
```

Figure 3: scripts/basc.sdc

To ensure the outside world constrains parameters is settled correctly you can find in scripts/base.tcl:

- **Driving cell → sky130_fd_sc_hd__inv_2 (we use cell with low driving strength to not be more optimistic)**
- **Load cap → 33.44 ff (also moderate out load cap to simulate the real case)**

Project iterations

BEFORE STARTING: I had big problem with STA after synthesis it run in the typical corner only not all corners and that make me relaxed with timing in all phases and shocked me in signoff.

Solution:

- **Start from flow.tcl (search for run_synthesis proc) I didn't find it.**
- **Grep it the found it in scripts/tcl_commands/synthesis.tcl**
- **With some tracing run_sta proc founded and has a switch of (-pre_sta)**
- **Grep for run_sta to find in scripts/tcl_commands/sta.tcl and has two flage (-pre_sta , -multi_corner)**
- **I back to run_sta proc and change the switch to -multi_corner and it works Alhamdulillah.**

sta.tcl - /home/opentools/OpenLane/scripts/tcl_commands/

File Edit Search Preferences Shell Macro Windows

```
11 # WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or
12 # See the License for the specific language governing permissions
13 # limitations under the License.
14
15 proc run_sta {args} {
16     set options {
17         {-log required}
18         {-lef optional}
19         {-process_corner optional}
20     }
21     set flags {
22         -multi_corner
23         -pre_cts
24     }
25     parse_key_args "run_sta" args arg_values $options flags_map $1
26     set multi_corner [info exists flags_map(-multi_corner)]
27     set pre_cts [info exists flags_map(-pre_cts)]
28
```

Figure 4: Here we know there is two switches to proc run_sta.

synthesis.tcl - /home/opentools/OpenLane/scripts/tcl_commands/

File Edit Search Preferences Shell Macro Windows

```
112 proc run_synthesis {args} {
113     increment_index
114     TIMER::timer_start
115     puts_info "Running Synthesis..."
116     set ::env(CURRENT_SDC) $::env(BASE_SDC_FILE)
117     # in-place insertion
118     if { [file exists $::env(synthesis_results)/$::env(DESIGN_NAME).v] } {
119         puts_warn "A netlist at $::env(synthesis_results)/$::env(DESIGN_NAME
120         set_netlist $::env(synthesis_results)/$::env(DESIGN_NAME).v
121     } else {
122         run_yosys
123     }
124     TIMER::timer_stop
125     exec echo "[TIMER::get_runtime]" | python3 $::env(SCRIPTS_DIR)/write_ru
126
127     run_sta -multi_corner -log $::env(synthesis_logs)/sta.log
128     set ::env(LAST_TIMING_REPORT_TAG) [index_file $::env(synthesis_reports)
129
130     if { $::env(RUN_SIMPLE_CTS) && $::env(CLOCK_TREE_SYNTH) } {
131         if { ! [info exists ::env(CLOCK_NET)] } {
132             set ::env(CLOCK_NET) $::env(CLOCK_PORT)
133         }
```

Figure 5:Here we find the proc run_sta and edit the switch of -multi_corner

```
[INFO]: Preparing LEF files for the nom corner...
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[STEP 1]
[INFO]: Running Synthesis...
[STEP 2]
[INFO]: Running Multi-Corner Static Timing Analysis...
[INFO]: Saving current set of views in 'designs/wbqspiflash/runs/iter1_5ns/resul
ts/final'...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
```

Figure 6: Now we can run multi corner analysis.

Conclusion → We can run multi corner static timing analysis after synthesis.

Iteration 1

Starting from:

- **Clock period = 5ns**
- **Clock transition = 0.1ns**
- **Max fanout = 4 cells**

and run synthesis.

- We reached to -5.08 slack and transition violation because the big fanout in the clock net in addition to the cap violation.

- Area → 24064 um2

```
Startpoint: _5114_ (rising edge-triggered flip-flop clocked by i_clk)
Endpoint: o_qspi_sck (output port clocked by i_clk)
Path Group: i_clk
Path Type: max
Corner: ss

Fanout     Cap     Slew   Delay    Time   Description
---------------------------------------------------------------------------
                           0.00    0.00   clock i_clk (rise edge)
                           0.00    0.00   clock source latency
                    3.63   2.69    2.69 ^ i_clk (in)
   280    0.51                           i_clk (net)
                    3.63   0.00    2.69 ^ _5114_/CLK (sky130_fd_sc_hd__dfxtp_2)
                    0.06   1.64    4.33 ^ _5114_/Q (sky130_fd_sc_hd__dfxtp_2)
     2    0.00                           lldriver.o_sck (net)
                    0.06   0.00    4.33 ^ _2457_/A (sky130_fd_sc_hd__buf_1)
                    0.23   0.27    4.60 ^ _2457_/X (sky130_fd_sc_hd__buf_1)
     4    0.01                           _2096_ (net)
                    0.23   0.00    4.61 ^ _2458_/A (sky130_fd_sc_hd__buf_1)
                    0.16   0.29    4.90 ^ _2458_/X (sky130_fd_sc_hd__buf_1)
     4    0.01                           _2097_ (net)
                    0.16   0.00    4.90 ^ _2459_/A (sky130_fd_sc_hd__buf_1)
                    0.23   0.31    5.21 ^ _2459_/X (sky130_fd_sc_hd__buf_1)
     4    0.01                           _2098_ (net)
                    0.23   0.00    5.22 ^ _2460_/A (sky130_fd_sc_hd__buf_1)
                    0.25   0.36    5.57 ^ _2460_/X (sky130_fd_sc_hd__buf_1)
     4    0.01                           _2099_ (net)
                    0.25   0.00    5.58 ^ _2461_/A (sky130_fd_sc_hd__buf_1)
                    0.21   0.34    5.91 ^ _2461_/X (sky130_fd_sc_hd__buf_1)
     4    0.01                           _2100_ (net)
                    0.21   0.00    5.92 ^ _2462_/A (sky130_fd_sc_hd__buf_1)
                    0.19   0.31    6.22 ^ _2462_/X (sky130_fd_sc_hd__buf_1)
     4    0.01                           _2101_ (net)
                    0.19   0.00    6.23 ^ _2491_/A0 (sky130_fd_sc_hd__mux2_2)
                    0.07   0.33    6.55 ^ _2491_/X (sky130_fd_sc_hd__mux2_2)
     1    0.00                           _2129_ (net)
                    0.07   0.00    6.56 ^ _2492_/A (sky130_fd_sc_hd__buf_1)
                    0.67   0.57    7.13 ^ _2492_/X (sky130_fd_sc_hd__buf_1)
     1    0.03                           o_qspi_sck (net)
                    0.67   0.00    7.13 ^ o_qspi_sck (out)
                           7.13    7.13   data arrival time

                           5.00    5.00   clock i_clk (rise edge)
                           0.00    5.00   clock network delay (propagated)
                          -0.20    4.80   clock uncertainty
                           0.00    4.80   clock reconvergence pessimism
                          -2.75    2.05   output external delay
                                   2.05   data required time
---------------------------------------------------------------------------
                                   2.05   data required time
                                  -7.13   data arrival time
---------------------------------------------------------------------------
                                  -5.08   slack (VIOLATED)
```

Figure 7: negative slack 5.08ns

```
594
595 max fanout
596
597 Pin                                  Limit Fanout  Slack
598 ------------------------------------------------------
599 i_clk                                    4    280   -276 (VIOLATED)
600
601 max capacitance
602
```

Figure 8: we have max fanout make big transition and big delay.

The solution is to use set_dont_touch command to ignore i_clk net but the version of tool we use isn't updated enough the new versions accept this command.

```
[STEP 2]
[INFO]: Running Multi-Corner Static Timing Analysis...
[ERROR]: during executing openroad script /home/opentools/OpenLane/scripts/o
pad/sta_multi_corner.tcl
[ERROR]: Exit code: 1
[ERROR]: full log: designs/wbqspiflash/runs/iter1_5ns_try/logs/synthes
og
[ERROR]: Last 10 lines:
[INFO ODB-0226] Finished LEF file:  /home/opentools/OpenLane/designs/w
/runs/iter1_5ns_try/tmp/merged.nom.lef
lf {[info exists ::env(CLOCK_PORT)] && $::env(CLOCK_PORT) != ""} {
    create_clock [get_ports $::env(CLOCK_PORT)]  -name $::env(CLOCK_PO
od $::env(CLOCK_PERIOD)
} else {
    create_clock -name __VIRTUAL_CLK__ -period $::env(CLOCK_PERIOD)
    set ::env(CLOCK_PORT) __VIRTUAL_CLK__
}
set_dont_touch i_clk
Error: base.sdc, 7 invalid command name "set_dont_touch"
child process exited abnormally
```

```
4     create_clock -name __VIRTUAL_CLK__ -period $::env
5     set ::env(CLOCK_PORT) __VIRTUAL_CLK__
6 }
7 set_dont_touch i_clk
8
9 #DONT_BUFFER_PORTS ::env(CLOCK_PORT)
0
1 set input_delay_value [expr $::env(CLOCK_PERIOD) * $
2 set output_delay_value [expr $::env(CLOCK_PERIOD) *
3 puts "\[INFO\]: Setting output delay to: $output dela
```

Figure 9: Tool don't accept this command.

In my opinion to proceed to CTS where well-structured clock network will be used, and this transition will disappear.

Iteration 2

We run to CTS this time with the same constrains:

- **Clock period = 5ns**
- **Clock transition = 0.1ns**
- **Max fanout = 4 cells**

- The clock tree has been structured and we get -0.99 slack instead of -5.08 and less fanout violations.

- Area → 27820 um2

13-cts_rsz_sta.slew.rpt - /home/opentools/OpenLane/designs/wbqspiflash/runs/iter2_5ns/rep...

File Edit Search Preferences Shell Macro Windows

```
1
2 ========================================================================
3  report_check_types -max_slew -max_cap -max_fanout -violators
4 ========================================================================
5 max fanout
6
7 Pin                                   Limit Fanout  Slack
8 ------------------------------------------------------------
9 clkbuf_5_10_0_i_clk/X                     4     17    -13 (VIOLATED)
10 clkbuf_0_i_clk/X                         4     16    -12 (VIOLATED)
11 clkbuf_5_11_0_i_clk/X                    4     13     -9 (VIOLATED)
12 clkbuf_5_6_0_i_clk/X                     4     13     -9 (VIOLATED)
13 clkbuf_5_15_0_i_clk/X                    4     12     -8 (VIOLATED)
14 clkbuf_5_31_0_i_clk/X                    4     12     -8 (VIOLATED)
15 clkbuf_5_8_0_i_clk/X                     4     12     -8 (VIOLATED)
16 clkbuf_5_9_0_i_clk/X                     4     12     -8 (VIOLATED)
17 clkbuf_5_16_0_i_clk/X                    4     10     -6 (VIOLATED)
18 clkbuf_5_28_0_i_clk/X                    4     10     -6 (VIOLATED)
19 clkbuf_5_29_0_i_clk/X                    4     10     -6 (VIOLATED)
```

Figure 10: CTN was structured and we ger less violations.

But this slack is misleading as CTS run in TT corner only, I try to make it as synthesis, but it doesn't work.

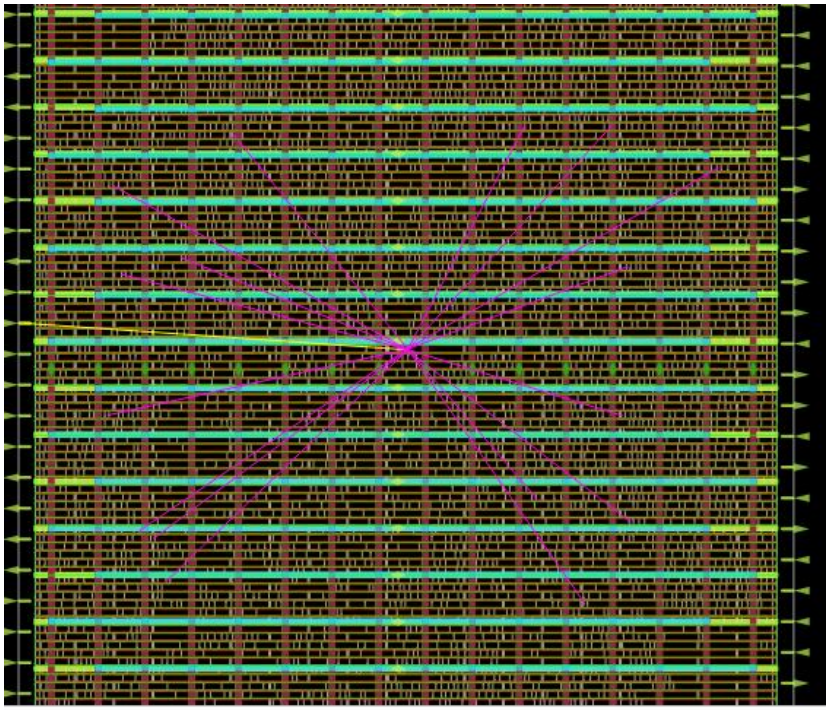


Figure 11: Screenshot from GUI to ensure CTS performed.

The solution is to run the flow to signoff and make analysis in its STA engine with multi corners and then can judge in timing correctly.

Iteration3

We run to signoff this time with the same constrains:

- **Clock period = 5ns**
- **Clock transition = 0.1ns**
- **Max fanout = 4 cells**

- We have slack of -4.12ns in SS corner also logical DRC violations (transition, capacitance and fanout).

- Area → 58220 um2

- DRCs → zero

29-rcx_mca_sta.slew.rpt - /home/opentools/OpenLane/designs/wbqspiflash/runs/iter3_5ns/re...

File Edit Search Preferences Shell Macro Windows

```
  6 ======================= Slowest Corner ================================
  7
  8 max slew
  9
 10 Pin                                        Limit    Slew   Slack
 11 ------------------------------------------------------------------
 12 clkbuf_4_8_0_i_clk/A                        1.50    1.63   -0.13 (VIOLATED)
 13 clkbuf_4_9_0_i_clk/A                        1.50    1.63   -0.13 (VIOLATED)
 14 clkbuf_4_10_0_i_clk/A                       1.50    1.63   -0.13 (VIOLATED)
 15 clkbuf_4_0_0_i_clk/A                        1.50    1.63   -0.13 (VIOLATED)
 16 clkbuf_4_1_0_i_clk/A                        1.50    1.63   -0.13 (VIOLATED)
 17 clkbuf_4_2_0_i_clk/A                        1.50    1.63   -0.13 (VIOLATED)
 18 clkbuf_4_11_0_i_clk/A                       1.50    1.63   -0.13 (VIOLATED)
 19 clkbuf_4_12_0_i_clk/A                       1.50    1.63   -0.13 (VIOLATED)
 20 clkbuf_4_13_0_i_clk/A                       1.50    1.63   -0.13 (VIOLATED)
 21 clkbuf_4_7_0_i_clk/A                        1.50    1.63   -0.13 (VIOLATED)
 22 clkbuf_4_15_0_i_clk/A                       1.50    1.63   -0.13 (VIOLATED)
 23 clkbuf_4_3_0_i_clk/A                        1.50    1.63   -0.13 (VIOLATED)
 24 clkbuf_4_5_0_i_clk/A                        1.50    1.63   -0.13 (VIOLATED)
 25 clkbuf_4_4_0_i_clk/A                        1.50    1.63   -0.13 (VIOLATED)
 26 clkbuf_4_14_0_i_clk/A                       1.50    1.63   -0.13 (VIOLATED)
 27 clkbuf_4_6_0_i_clk/A                        1.50    1.63   -0.13 (VIOLATED)
 28 clkbuf_0_i_clk/X                            1.51    1.63   -0.12 (VIOLATED)
 29
```

Figure 12: DRC violations

So, in this iteration we discover that we have problem with setup violation and that may fix by increase the period, second problem with the logical DRCs (transition, fanout, cap)

- To solve logical DRCs problem in my opinion to give it more slack in timing to insert more buffers and make more branches of fanouts to decrease the capacitance on the drivers and enhance the output transition of them, so I will increase clock period to 20ns and see what happen.

Iteration 4

We run to signoff with this constrains:

- **Clock period = 20ns**
- **Clock transition = 0.1ns**
- **Max fanout = 4 cells**

- Positive slack 1.96ns

- Area 57998 um2

The logical DRCs remain the same and increased and this is unexpected I expect with more positive slack will fix logical DRCs.

29-rcx_mca_sta.slew.rpt - /home/opentools/OpenLane/designs/wbqspiflash/runs/itertry_5ns/r...

File Edit Search Preferences Shell Macro Windows

29-rcx_mca_sta.slew.rpt | 29-rcx_mca_sta.worst_sl | 29-rcx_mca_sta.rpt

```
  6 ========================= Slowest Corner ===================================
  7
  8 max slew
  9
 10 Pin                                              Limit     Slew    Slack
 11 ------------------------------------------------------------------------
 12 clkbuf_4_14_0_i_clk/A                             1.50     1.72    -0.22  (VIOLATED)
 13 clkbuf_4_11_0_i_clk/A                             1.50     1.72    -0.22  (VIOLATED)
 14 clkbuf_4_10_0_i_clk/A                             1.50     1.72    -0.22  (VIOLATED)
 15 clkbuf_4_15_0_i_clk/A                             1.50     1.72    -0.22  (VIOLATED)
 16 clkbuf_4_8_0_i_clk/A                              1.50     1.72    -0.22  (VIOLATED)
 17 clkbuf_4_0_0_i_clk/A                              1.50     1.72    -0.22  (VIOLATED)
 18 clkbuf_4_1_0_i_clk/A                              1.50     1.72    -0.22  (VIOLATED)
 19 clkbuf_4_13_0_i_clk/A                             1.50     1.72    -0.22  (VIOLATED)
 20 clkbuf_4_2_0_i_clk/A                              1.50     1.72    -0.22  (VIOLATED)
 21 clkbuf_4_3_0_i_clk/A                              1.50     1.72    -0.22  (VIOLATED)
 22 clkbuf_4_4_0_i_clk/A                              1.50     1.72    -0.22  (VIOLATED)
 23 clkbuf_4_12_0_i_clk/A                             1.50     1.72    -0.22  (VIOLATED)
 24 clkbuf_4_9_0_i_clk/A                              1.50     1.72    -0.22  (VIOLATED)
 25 clkbuf_4_5_0_i_clk/A                              1.50     1.72    -0.22  (VIOLATED)
 26 clkbuf_4_6_0_i_clk/A                              1.50     1.72    -0.22  (VIOLATED)
 27 clkbuf_4_7_0_i_clk/A                              1.50     1.72    -0.22  (VIOLATED)
 28 clkbuf_0_i_clk/X                                  1.51     1.72    -0.20  (VIOLATED)
 29
 30 max fanout
 31
 32 Pin                                            Limit  Fanout   Slack
 33 ------------------------------------------------------------------------
 34 input28/X                                         4      26     -22  (VIOLATED)
 35 input33/X                                         4      25     -21  (VIOLATED)
 36 input56/X                                         4      25     -21  (VIOLATED)
 37 clkbuf_5_0_0_i_clk/X                              4      21     -17  (VIOLATED)
 38 clkbuf_0_i_clk/X                                  4      16     -12  (VIOLATED)
 39 clkbuf_5_1_0_i_clk/X                              4      15     -11  (VIOLATED)
 40 clkbuf_5_21_0_i_clk/X                             4      13      -9  (VIOLATED)
 41 clkbuf_5_3_0_i_clk/X                              4      13      -9  (VIOLATED)
```

Figure 13: Logical DRCs still exist.

To ensure I investigated the max slew net and the max fanout net.

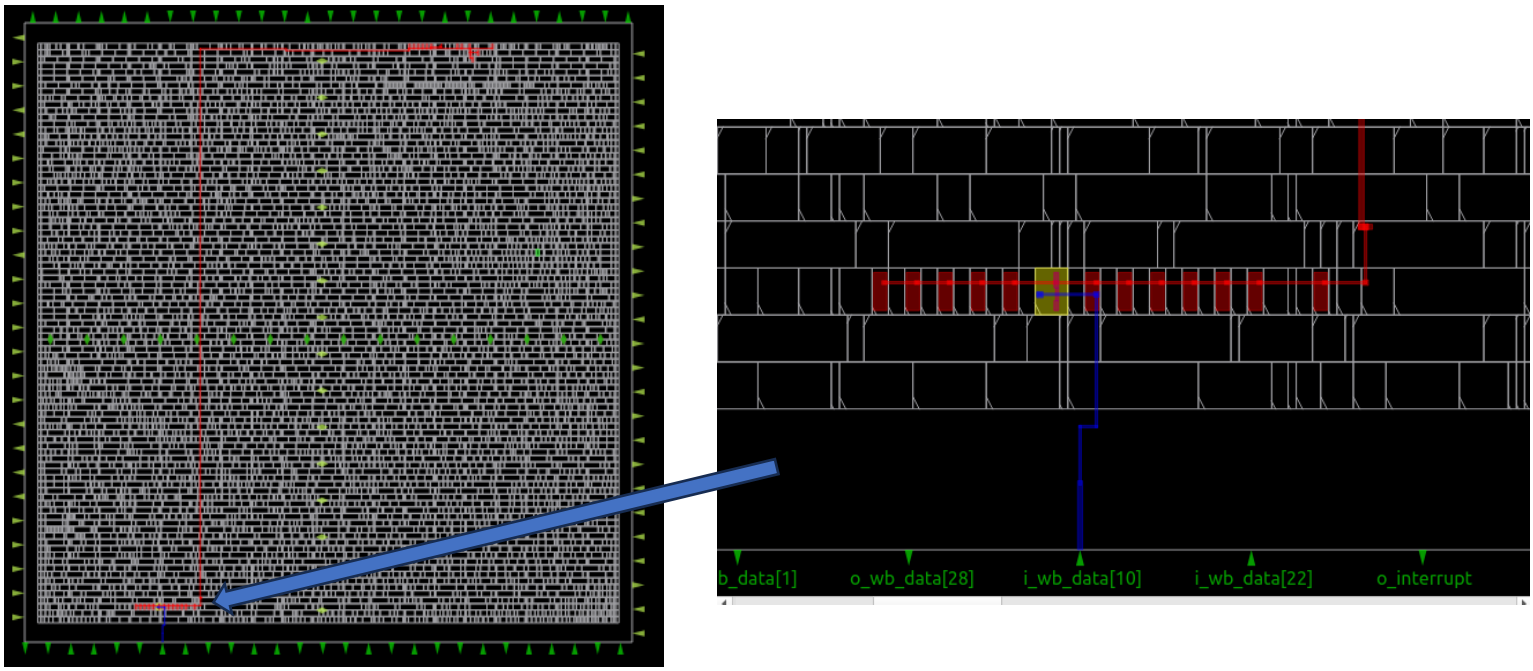


Figure 14 : The max fanout net derived by x2 buffer.

The max fanout net: drive 26 cell and derived by x2 buffer.

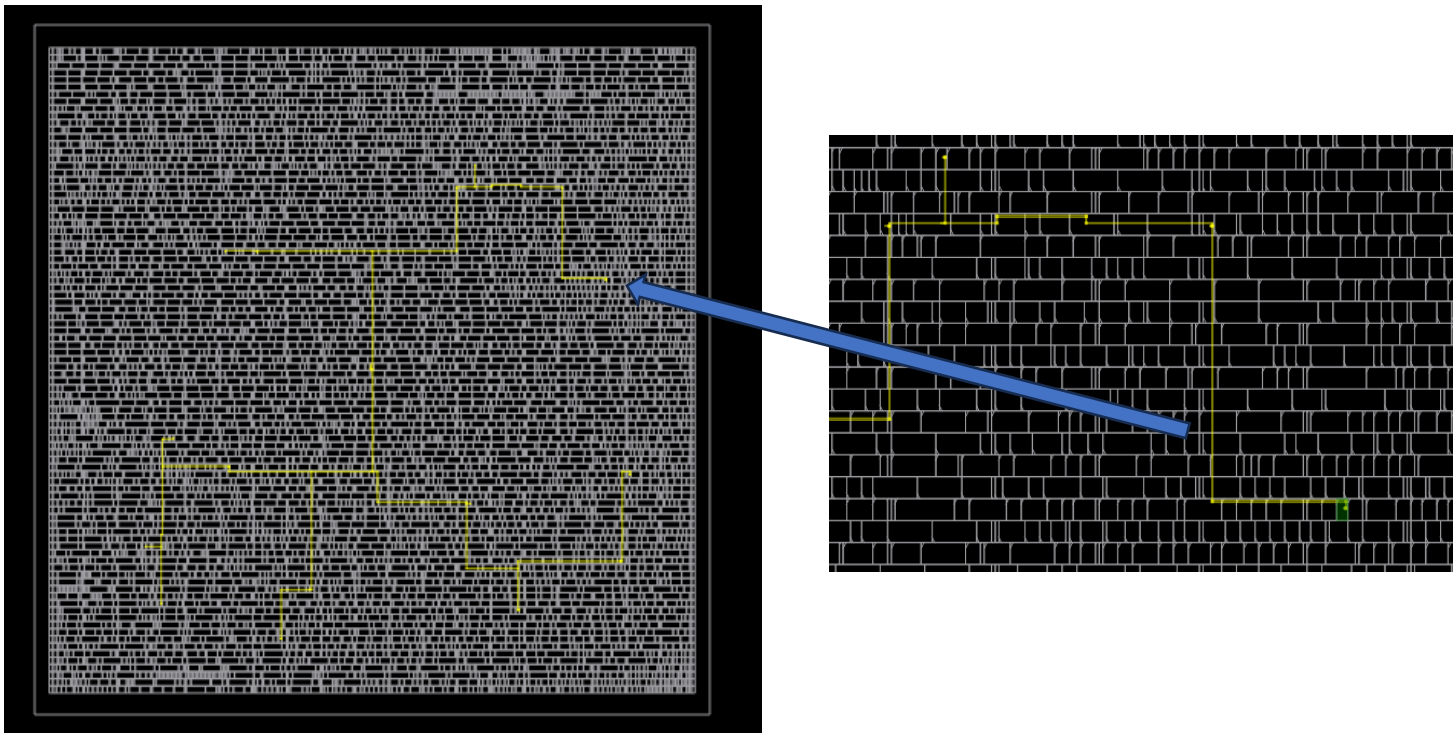


Figure 15: The big net is derived by x1 buffer.

The biggest transition net is divided by x1 buffer.

Now I am confused between I haven't good understand about fixing the violation or the tool engines are weak and didn't respond.

As I know in tool should do High fanout synthesis in placement stage and add buffers to decrease the fanout then the capacitance decreases then the transition decrease also place cells with same timing path near to each other, but let's proceed and know how we will fix the violations.

Iteration5

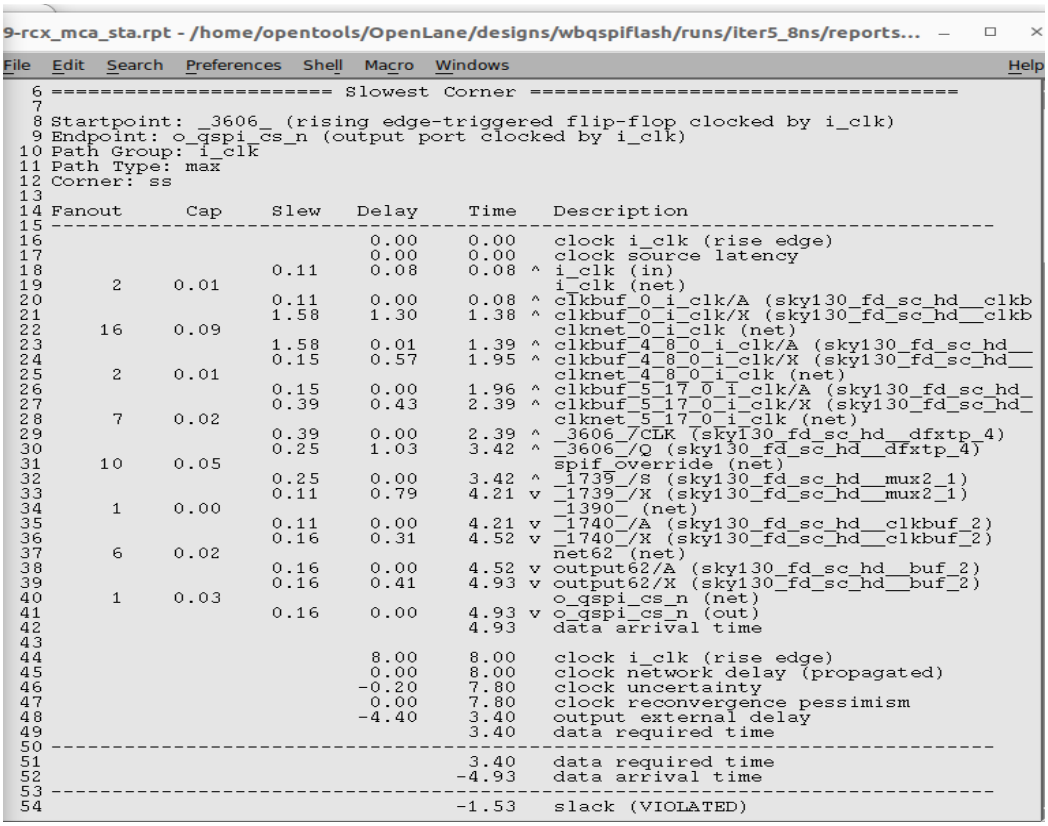
We run to signoff with these modifications:

- **Clock period = 8ns**
- **Clock transition = 0.1ns**
- **Max fanout = 16 cells**

- Negative slack -1.53ns

- Area 51866 um2 (the synthesis cell area is smaller as with high fanout the tool doesn't use more buffers it doesn't optimize the HFN)

Logical DRCs almost disappear I don't want to say fixed.



```
9-rcx_mca_sta.rpt - /home/opentools/OpenLane/designs/wbqspiflash/runs/iter5_8ns/reports...
File  Edit  Search  Preferences  Shell  Macro  Windows  Help
  6 ======================== Slowest Corner ===================================
  7
  8 Startpoint: _3606_ (rising edge-triggered flip-flop clocked by i_clk)
  9 Endpoint: o_qspi_cs_n (output port clocked by i_clk)
 10 Path Group: i_clk
 11 Path Type: max
 12 Corner: ss
 13
 14 Fanout      Cap     Slew    Delay    Time    Description
 15 ---------------------------------------------------------------------------
 16                             0.00    0.00    clock i_clk (rise edge)
 17                             0.00    0.00    clock source latency
 18                      0.11   0.08    0.08 ^ i_clk (in)
 19       2     0.01                           i_clk (net)
 20                      0.11   0.00    0.08 ^ clkbuf_0_i_clk/A (sky130_fd_sc_hd__clkb
 21                      1.58   1.30    1.38 ^ clkbuf_0_i_clk/X (sky130_fd_sc_hd__clkb
 22      16     0.09                           clknet_0_i_clk (net)
 23                      1.58   0.01    1.39 ^ clkbuf_4_8_0_i_clk/A (sky130_fd_sc_hd__
 24                      0.15   0.57    1.95 ^ clkbuf_4_8_0_i_clk/X (sky130_fd_sc_hd__
 25       2     0.01                           clknet_4_8_0_i_clk (net)
 26                      0.15   0.00    1.96 ^ clkbuf_5_17_0_i_clk/A (sky130_fd_sc_hd_
 27                      0.39   0.43    2.39 ^ clkbuf_5_17_0_i_clk/X (sky130_fd_sc_hd_
 28       7     0.02                           clknet_5_17_0_i_clk (net)
 29                      0.39   0.00    2.39 ^ _3606_/CLK (sky130_fd_sc_hd__dfxtp_4)
 30                      0.25   1.03    3.42 ^ _3606_/Q (sky130_fd_sc_hd__dfxtp_4)
 31      10     0.05                           spif_override (net)
 32                      0.25   0.00    3.42 ^ _1739_/S (sky130_fd_sc_hd__mux2_1)
 33                      0.11   0.79    4.21 v _1739_/X (sky130_fd_sc_hd__mux2_1)
 34       1     0.00                           _1390_ (net)
 35                      0.11   0.00    4.21 v _1740_/A (sky130_fd_sc_hd__clkbuf_2)
 36                      0.16   0.31    4.52 v _1740_/X (sky130_fd_sc_hd__clkbuf_2)
 37       6     0.02                           net62 (net)
 38                      0.16   0.00    4.52 v output62/A (sky130_fd_sc_hd__buf_2)
 39                      0.16   0.41    4.93 v output62/X (sky130_fd_sc_hd__buf_2)
 40       1     0.03                           o_qspi_cs_n (net)
 41                      0.16   0.00    4.93 v o_qspi_cs_n (out)
 42                             4.93    data arrival time
 43
 44                             8.00    8.00    clock i_clk (rise edge)
 45                             0.00    8.00    clock network delay (propagated)
 46                            -0.20    7.80    clock uncertainty
 47                             0.00    7.80    clock reconvergence pessimism
 48                            -4.40    3.40    output external delay
 49                             3.40    data required time
 50 ---------------------------------------------------------------------------
 51                             3.40    data required time
 52                            -4.93    data arrival time
 53 ---------------------------------------------------------------------------
 54                            -1.53    slack (VIOLATED)
```

Figure 16:Critical path in iteration 5 with -1.53 slack

Iteration6

We run to signoff with some modifications:

- **Clock period = 8ns**
- **Clock transition = 0.1ns**
- **Max fanout = 16 cells**
- **Change in PDN VPITCH & HPITCH to 100**

- Negative slack -1.64ns

- Area 51683 um2 (less routing in PDN)

It is obvious that the design doesn't have bottleneck in the routing resources as the slack don't improve but we can benefit from such iteration coming in the area.

x_mca_sta.rpt - /home/opentools/OpenLane/designs/wbqspiflash/runs/iter5_8ns_PDN/re...

Edit Search Preferences Shell Macro Windows Help

```
========================== Slowest Corner ===================================

Startpoint: _3606_ (rising edge-triggered flip-flop clocked by i_clk)
Endpoint: o_qspi_cs_n (output port clocked by i_clk)
Path Group: i_clk
Path Type: max
Corner: ss

Fanout      Cap     Slew    Delay     Time    Description
-----------------------------------------------------------------------------
                            0.00     0.00    clock i_clk (rise edge)
                            0.00     0.00    clock source latency
                    0.11    0.08     0.08 ^  i_clk (in)
      2     0.01                             i_clk (net)
                    0.11    0.00     0.08 ^  clkbuf_0_i_clk/A (sky130_fd_sc_hd__clkb
                    1.64    1.35     1.43 ^  clkbuf_0_i_clk/X (sky130_fd_sc_hd__clkb
     16     0.09                             clknet_0_i_clk (net)
                    1.64    0.00     1.43 ^  clkbuf_4_9_0_i_clk/A (sky130_fd_sc_hd__
                    0.15    0.58     2.01 ^  clkbuf_4_9_0_i_clk/X (sky130_fd_sc_hd__
      2     0.01                             clknet_4_9_0_i_clk (net)
                    0.15    0.00     2.01 ^  clkbuf_5_18_0_i_clk/A (sky130_fd_sc_hd_
                    0.38    0.43     2.43 ^  clkbuf_5_18_0_i_clk/X (sky130_fd_sc_hd_
      8     0.02                             clknet_5_18_0_i_clk (net)
                    0.38    0.00     2.44 ^  _3606_/CLK (sky130_fd_sc_hd__dfxtp_4)
                    0.30    1.06     3.50 ^  _3606_/Q (sky130_fd_sc_hd__dfxtp_4)
     17     0.06                             spif_override (net)
                    0.30    0.00     3.50 ^  _1739_/S (sky130_fd_sc_hd__mux2_1)
                    0.11    0.82     4.32 v  _1739_/X (sky130_fd_sc_hd__mux2_1)
      1     0.00                             _1390_ (net)
                    0.11    0.00     4.32 v  _1740_/A (sky130_fd_sc_hd__clkbuf_2)
                    0.16    0.32     4.64 v  _1740_/X (sky130_fd_sc_hd__clkbuf_2)
      6     0.02                             net62 (net)
                    0.16    0.00     4.64 v  output62/A (sky130_fd_sc_hd__buf_2)
                    0.16    0.41     5.05 v  output62/X (sky130_fd_sc_hd__buf_2)
      1     0.03                             o_qspi_cs_n (net)
                    0.16    0.00     5.05 v  o_qspi_cs_n (out)
                            5.05     5.05    data arrival time

                            8.00     8.00    clock i_clk (rise edge)
                            0.00     8.00    clock network delay (propagated)
                           -0.20     7.80    clock uncertainty
                            0.00     7.80    clock reconvergence pessimism
                           -4.40     3.40    output external delay
                            3.40     3.40    data required time
-----------------------------------------------------------------------------
                            3.40     3.40    data required time
                                    -5.05    data arrival time
-----------------------------------------------------------------------------
                                    -1.65    slack (VIOLATED)
```

Figure 19: Critical path in iteration7 -1.64 slack

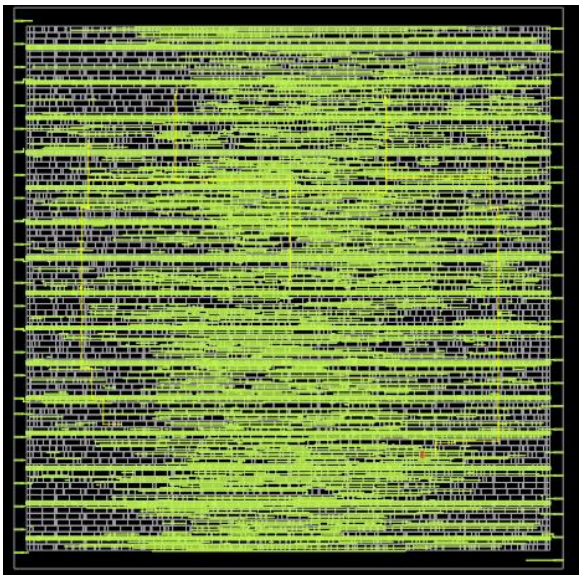


Figure 17:Before edit in PDN I thought there's need for mode routing resources.

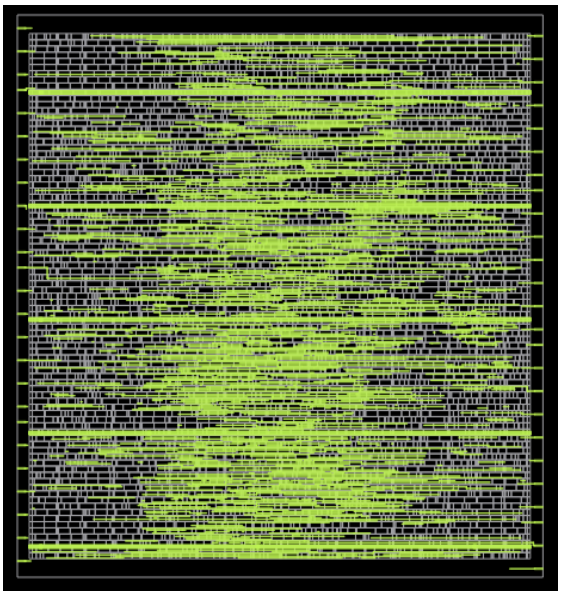


Figure 18:After edit in PDN there's more routing resources but the delay doesn't enhance.

Iteration7

We run to signoff with some modifications:

- **Clock period = 10ns**
- **Clock transition = 0.1ns**
- **Max fanout = 16 cells**
- **Change in PDN VPITCH & HPITCH to 100**

- Negative slack -0.76ns

- Area 51753 um2 (less routing in PDN)

- **We need to more increase in clock period.**

Iteration 8

We run to signoff with some modifications:

- **Clock period = 12ns (will have 0.9 to slack and 1.1 to output delay I think this will work)**
- **Clock transition = 0.1ns**
- **Max fanout = 16 cells (still found slight -ve slack in transition and cap)**
- **Change in PDN VOFFSET& HOFFSET to 100**

- Positive slack 0.16 ns

- Area 51683 um2 (less routing in PDN)

- **Now we meet timing alhamdulillah I want to change in FP_CORE_UTIL and reach the optimum in it to increase the slack as cells will be closer and if happen detouring, I have more routing resources from remover strips.**

Iteration 9

We run to signoff with some modifications:

- **Clock period = 12ns (will have 0.9 to slack and 1.1 to output delay I think this will work)**
- **Clock transition = 0.1ns**
- **Max fanout = 14 cells (still found slight -ve slack in transition and cap)**
- **Change in PDN VOFFSET& HOFFSET to 1000**
- **FP_CORE_UTIL = 45 (higher 5%)**

- Positive slack 0.26 ns (cells close to each others and we consume less delay in routing)

- Area 45892 um2 (less routing in PDN and less core area)

- **We enhance in delay and area which a good step.**

Iteration 10

We run to signoff with some modifications:

- **Clock period = 12ns (will have 0.9 to slack and 1.1 to output delay I think this will work)**
- **Clock transition = 0.1ns**
- **Max fanout = 14 cells (still found slight -ve slack in transition and cap)**
- **Change in PDN VOFFSET& HOFFSET to 1000**
- **FP_CORE_UTIL = 50 (higher 5%)**

- positive slack 0.11 ns

- Area 41367 um2 (less routing in PDN and less core area)

- **We enhance in area which a good step, we lose some slack, but we still meet timing.**

Iteration 11

- **The same configurations of iteration10 but FP_CORE_UTIL = 55 (higher 5%)**

- routing congestion is too high

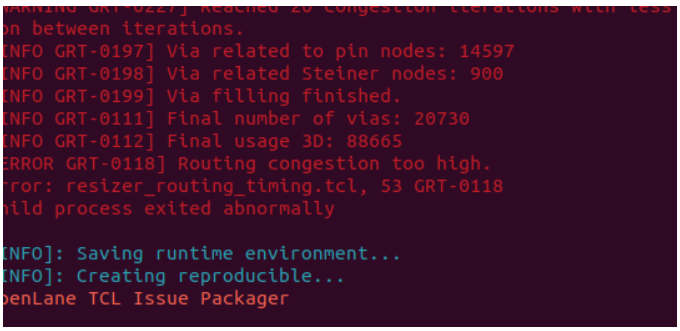


Figure 20: High congestion

Table of iterations

Iteration	Changed parameters	Period (ns)	Area (um2)	DRCs	Objective
1	-to synthesis	5	24064	0	Synthesis
2	-to CTS	5	27820	0	To rebuild the CTN which wrongly structured in synthesis and current tool version don't support set_don't_touch command
3	-to signoff	5	58220	0	To use multi corner STA which not found in CTS
4	CLOCK_PERIOD	20	57998	0	Fix logical DRCs (specially the transition)
5	SYNTH_MAX_FANOUT	8	51866	0	Fix logical DCs

6	VPITCH & HPITCH	8	51683	0	Provide more routing resources to enhance timing
7	CLOCK_PERIOD	10	51753	0	Meet setup
8	CLOCK_PERIOD	12 {0.16}	51683	0	Meet setup (MET)
9	FP_CORE_UTIL 45%	12(0.27)	45892	0	Enhance the delay
10	FP_CORE_UTIL 50 %	12(0.11)	41367	0	Enhance the delay
11	FP_CORE_UTIL 55%	-	congestion	0	Enhance the delay

Problems

when I put max fanout to 16 I have max fanout violation -1 then I increase the fanout in constrains to get transition violation and I can't break this loop

```
1
2 ===========================================================================
3  report_check_types -max_slew -max_cap -max_fanout -violators
4 ===========================================================================
5
6 ======================= Slowest Corner ====================================
7
8 max fanout
9
10 Pin                                  Limit Fanout  Slack
11 ---------------------------------------------------------
12 clkbuf_0_i_clk/X                       16     17       (VIOLATED)
13
14
15 ======================= Typical Corner ====================================
16
17 max fanout
18
19 Pin                                  Limit Fanout  Slack
20 ---------------------------------------------------------
21 clkbuf_0_i_clk/X                       16     17       (VIOLATED)
22
23
24 ======================= Fastest Corner ====================================
25
26 max fanout
27
28 Pin                                  Limit Fanout  Slack
29 ---------------------------------------------------------
30 clkbuf_0_i_clk/X                       16     17       (VIOLATED)
31
32
33 ===========================================================================
34 max slew violation count 0
35 max fanout violation count 1
36 max cap violation count 0
37 ===========================================================================
38
```

Figure 22: Max fanout violation

```
1
2 ===========================================================================
3  report_check_types -max_slew -max_cap -max_fanout -violators
4 ===========================================================================
5
6 ======================= Slowest Corner ====================================
7
8 max slew
9
10 Pin                                   Limit    Slew   Slack
11 ------------------------------------------------------------
12 clkbuf_4_0_0_i_clk/A                   1.50    1.54   -0.04 (VIOLATED)
13 clkbuf_4_2_0_i_clk/A                   1.50    1.54   -0.04 (VIOLATED)
14 clkbuf_4_1_0_i_clk/A                   1.50    1.54   -0.04 (VIOLATED)
15 clkbuf_4_3_0_i_clk/A                   1.50    1.54   -0.04 (VIOLATED)
16 clkbuf_4_4_0_i_clk/A                   1.50    1.54   -0.04 (VIOLATED)
17 clkbuf_4_5_0_i_clk/A                   1.50    1.54   -0.04 (VIOLATED)
18 clkbuf_4_7_0_i_clk/A                   1.50    1.54   -0.04 (VIOLATED)
19 clkbuf_4_6_0_i_clk/A                   1.50    1.54   -0.04 (VIOLATED)
20 clkbuf_4_13_0_i_clk/A                  1.50    1.54   -0.04 (VIOLATED)
21 clkbuf_4_15_0_i_clk/A                  1.50    1.54   -0.04 (VIOLATED)
22 clkbuf_4_14_0_i_clk/A                  1.50    1.54   -0.04 (VIOLATED)
23 clkbuf_4_12_0_i_clk/A                  1.50    1.54   -0.04 (VIOLATED)
24 clkbuf_4_10_0_i_clk/A                  1.50    1.54   -0.04 (VIOLATED)
25 clkbuf_4_8_0_i_clk/A                   1.50    1.54   -0.04 (VIOLATED)
26 clkbuf_4_9_0_i_clk/A                   1.50    1.54   -0.04 (VIOLATED)
27 clkbuf_4_11_0_i_clk/A                  1.50    1.54   -0.04 (VIOLATED)
28 clkbuf_0_i_clk/X                       1.51    1.54   -0.02 (VIOLATED)
29
```

Figure 22: Max transition violation

Conclusion

Finally, we run all PnR phases in the spiflash design and reached to 12 ns period which equal operating frequency 80 MHZ the critical path from DFF "_3606_" to the outport "o_qspi_cs_n" the design will give more operating frequency with more powerful optimization engines and more knowledgeable engineer than me.

the end of iteration

Question1

Part1: Arrange the pins.

- **I added the parameter FP_PIN_ORDER_CFG**
- **Pass the file name to it.**
- **Then put the file in the same directory with the arrangement of pins.**

Open

pin_order.cfg
/home/opentools/OpenLane/designs/wbqspiflash

```
1 #N
2 o_wb_ack
3 o_wb_stall
4 o_qspi_sck
5 o_qspi_cs_n
6 o_qspi_mod.*
7 o_qspi_dat.*
8
9 #S
10 o_wb_data.*
11 o_interrupt
12
13 #E
14 i_clk
15 i_wb_cyc
16 i_wb_data_stb
17 i_wb_ctrl_stb
18 i_wb_we
19 i_qspi_dat.*
20 i_wb_addr.*
21
22 #W
23 i_wb_data\[\d\]
24 i_wb_data\[\d\d\]
25
26
27
28
29
```

Figure 23: designs/wbqspiflash/pin_order.cfg

Command:

➔ (SET:: ENV(FP_PIN_ORDER_CFG) $::ENV(DESIGN_DIR)/PIN_ORDER.CFG)

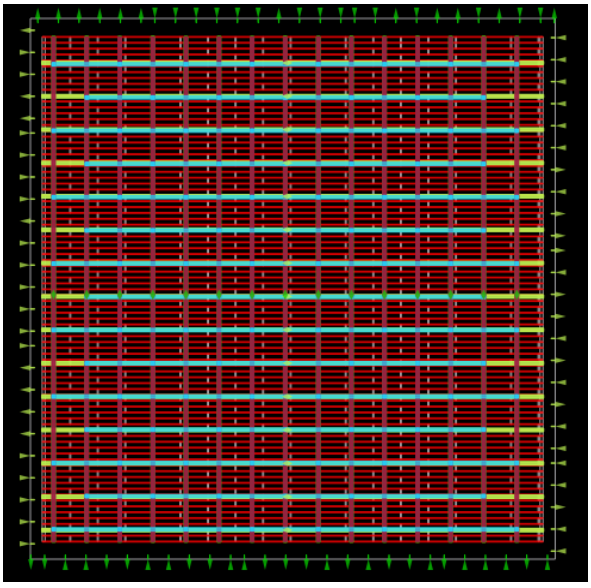


Figure 24: Before pin arrangement

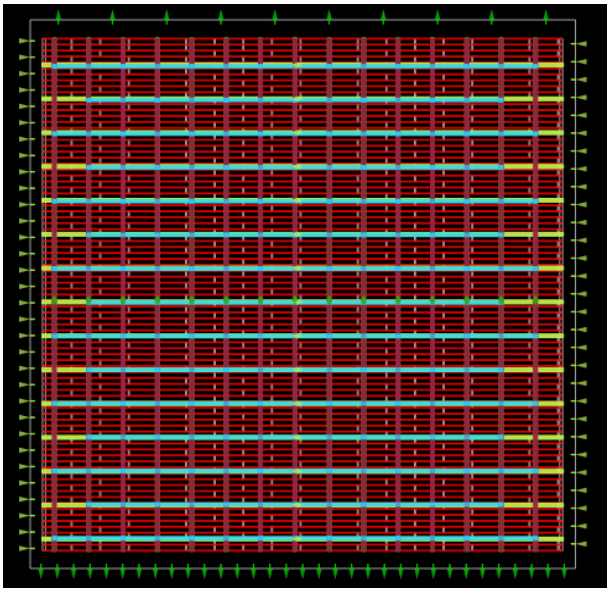


Figure 25: After pin arrangement

patr2- The thickness of the vertical and horizontal pins is to be 1x default width.

```
set ::env(FP_IO_MODE) 1; # 0 matching mode - 1
set ::env(FP_IO_HLENGTH) 2
set ::env(FP_IO_VLENGTH) 2
set ::env(FP_IO_VEXTEND) -1
set ::env(FP_IO_HEXTEND) -1
set ::env(FP_IO_VTHICKNESS_MULT) 1
set ::env(FP_IO_HTHICKNESS_MULT) 1
set ::env(FP_IO_MIN_DISTANCE) 3
set ::env(FP_IO_UNMATCHED_ERROR) 1

```

Figure 26:configurations/floorplan.tcl

Set FB_IO_VTHICKNESS_MULT and FB_IO_HTHICKNESS_MULT to 1 instead of 2

Part3- The length of the pins is to be 2um.

Set FP_IO_HLENGTH to 2 instead of 4 also FP_VLENGTH to 2

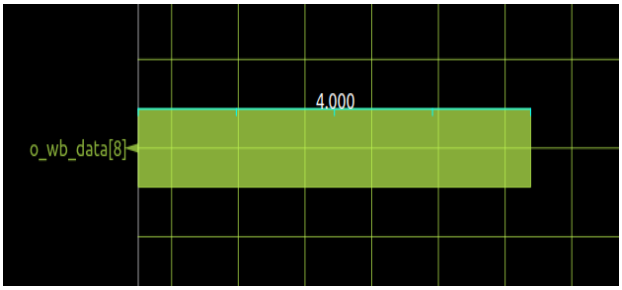


Figure 28: Before modification (4um, x2)

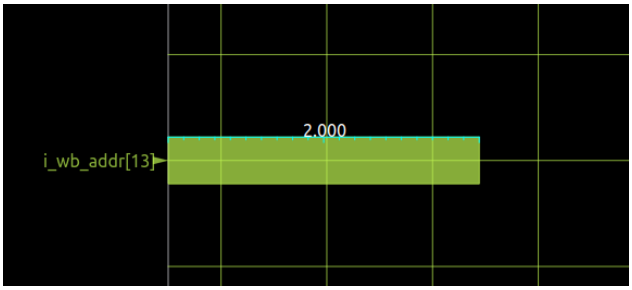


Figure 28:After modification (2um, x1)

Question2:

Edit the power structure to have straps in all metals (met1 to met5):

Firstly, create new grid for the two new stripes (stdcell_grid_2) →

```
##################### grid between met2 , met3 ############################
    define_pdn_grid \
        -name stdcell_grid \
        -starts_with POWER \
        -voltage_domain CORE \
        -pins "$::env(FP_PDN_LOWER_LAYER) $::env(FP_PDN_INTERNAL1_LAYER)"


##################### grid between met4 , met5 ############################
    define_pdn_grid \
        -name stdcell_grid_2 \
        -starts_with POWER \
        -voltage_domain CORE \
        -pins "$::env(FP_PDN_INTERNAL2_LAYER) $::env(FP_PDN_INTERNAL2_LAYER)"


```

Figure 29:Define new grid.

Secondly, add the two new stripes →

```
############################ stripe for met4 ####################
    add_pdn_stripe \
        -grid stdcell_grid_2 \
        -layer $::env(FP_PDN_INTERNAL2_LAYER) \
        -width $::env(FP_PDN_VWIDTH) \
        -pitch $::env(FP_PDN_VPITCH) \
        -offset $::env(FP_PDN_VOFFSET) \
        -starts_with POWER -extend_to_core_ring

############################ stripe for met5 ####################

    add_pdn_stripe \
        -grid stdcell_grid_2 \
        -layer $::env(FP_PDN_UPPER_LAYER) \
        -width $::env(FP_PDN_HWIDTH) \
        -pitch $::env(FP_PDN_HPITCH) \
        -offset $::env(FP_PDN_HOFFSET) \
        -starts_with POWER -extend_to_core_ring
```

Figure 30:Add the two new stripes.

Thirdly, drop vias between:

- **Metal layer 4 ,5**
- **Metal layer 2 ,3**
- **Metal layer 3 ,4**
- **Ralis, Metal layer 2**

```
################### via between met2 , met3 ##########################
    add_pdn_connect \
        -grid stdcell_grid \
        -layers "$::env(FP_PDN_LOWER_LAYER) $::env(FP_PDN_INTERNAL1_LAYER)"


################### via between met4 , met5 ##########################
    add_pdn_connect \
        -grid stdcell_grid_2 \
        -layers "$::env(FP_PDN_INTERNAL2_LAYER) $::env(FP_PDN_UPPER_LAYER)"

################### via between met3 , met4 ##########################
    add_pdn_connect \
        -grid stdcell_grid_2 \
        -layers "$::env(FP_PDN_INTERNAL1_LAYER) $::env(FP_PDN_INTERNAL2_LAYER)"


```

Figure 31:Drop VIAS

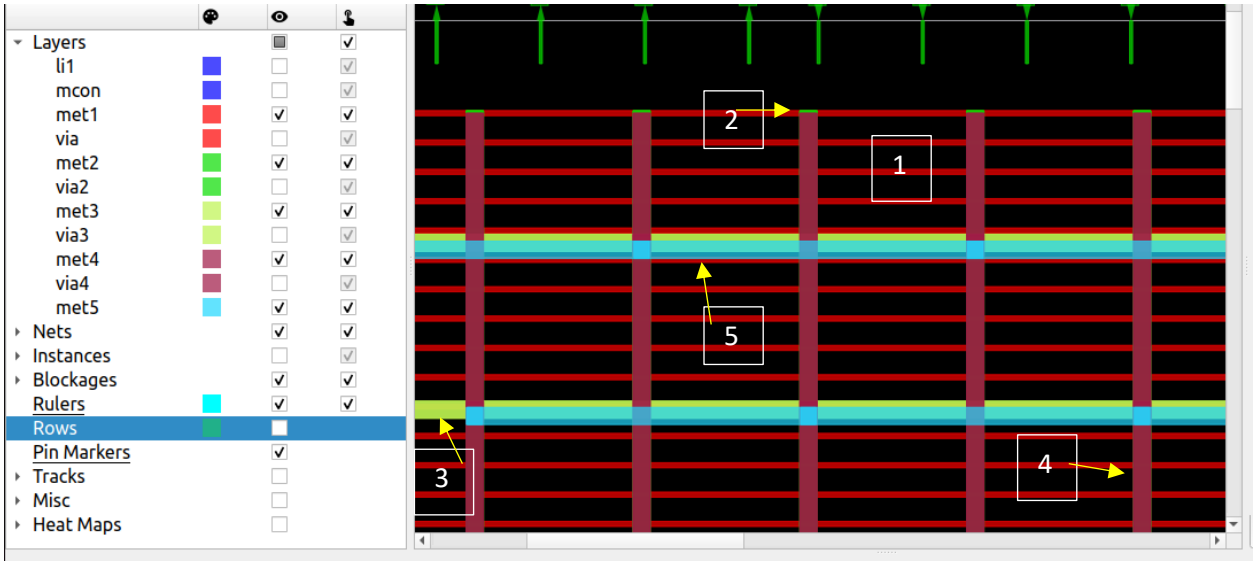


Figure 32:The 5 Metal layers in GUI

And change these values in the floorplan configuration. →

```
14
15 # Floorplan defaults
16 set ::env(FP_SIZING) relative
17 set ::env(FP_CORE_UTIL) 40
18 set ::env(FP_CORE_MARGIN) 0
19 set ::env(FP_ASPECT_RATIO) 1
20
21 set ::env(FP_PDN_HPITCH) {30.8}
22 set ::env(FP_PDN_HOFFSET) {5.65}
23 set ::env(FP_PDN_VOFFSET) {5.32}
24 set ::env(FP_PDN_VPITCH) {30.94}
25 set ::env(FP_PDN_AUTO_ADJUST) 0
26
27 set ::env(FP_PDN_CORE_RING) 0
28 set ::env(FP_PDN_ENABLE_RAILS) 1
29
```

Figure 33: Change PDN parameters

Question3

Part1: Edit Placement configurations to achieve the required target.

- **PL_TARGET_DENISTY → should be suitable.**
- **I tried to make it (0.75) to make cells near to each others and save in timing**
- **But the routing fails and that make much detouring and need more routing resources as the area is congested.**

```
STEP 7]
INFO]: Running Global Placement...
STEP 8]
INFO]: Running Placement Resizer Design Optimizations...
ERROR]: during executing openroad script /home/opentools/OpenLane/scripts/openroad/resi
er.tcl
ERROR]: Exit code: 1
ERROR]: full log: designs/wbqspiflash/runs/final/logs/placement/8-resizer.log
ERROR]: Last 10 lines:
INFO DPL-0035]  _2939_
INFO DPL-0035]  _2939_
INFO DPL-0035]  input53
INFO DPL-0035]  input53
INFO DPL-0035]  input49
INFO DPL-0035]  input49
INFO DPL-0035]  input38
ERROR DPL-0036] Detailed placement failed.
rror: resizer.tcl, 79 DPL-0036
hild process exited abnormally
```

Figure 34:Detailed placement failed.

Finally, I set it to (0.4) to spread the cells over area and have good IR analysis.

Second parameter :

PL_RESIZER_DESIGN_OPTIMIZATIONS also set to 1 as it makes more optimizations at cells to meet timing.

```
Startpoint: i_wb_addr[1] (input port clocked by i_clk)
Endpoint: _3977_ (rising edge-triggered flip-flop clocked by i_clk)
Path Group: i_clk
Path Type: max
Fanout     Cap     Slew   Delay    Time   Description
                   0.15    0.00    0.00   clock i_clk (rise edge)
                           0.00    0.00   clock network delay (ideal)
                           4.40    4.40 v input external delay
                   0.07    0.05    4.45 v i_wb_addr[1] (in)
     5    0.03                             i_wb_addr[1] (net)
                   0.07    0.00    4.45 v _1970_/A (sky130_fd_sc_hd__or2_2)
                   0.07    0.33    4.79 v _1970_/X (sky130_fd_sc_hd__or2_2)
     2    0.01                             _1600_ (net)
                   0.07    0.00    4.79 v _2052_/A (sky130_fd_sc_hd__buf_1)
                   0.15    0.20    4.99 v _2052_/X (sky130_fd_sc_hd__buf_1)
     8    0.03                             _1682_ (net)
                   0.15    0.00    4.99 v _2053_/C (sky130_fd_sc_hd__or4b_2)
                   0.12    0.70    5.69 v _2053_/X (sky130_fd_sc_hd__or4b_2)
     3    0.01                             _1683_ (net)
                   0.12    0.00    5.69 v _2055_/A (sky130_fd_sc_hd__and3_2)
                   0.05    0.24    5.93 v _2055_/X (sky130_fd_sc_hd__and3_2)
     3    0.01                             _1685_ (net)
                   0.05    0.00    5.93 v _3325_/A_N (sky130_fd_sc_hd__and4b_2)
                   0.06    0.28    6.21 ^ _3325_/X (sky130_fd_sc_hd__and4b_2)
     1    0.00                             _1182_ (net)
                   0.06    0.00    6.21 ^ _3326_/D1 (sky130_fd_sc_hd__o2111a_2)
                   0.07    0.21    6.42 ^ _3326_/X (sky130_fd_sc_hd__o2111a_2)
     2    0.01                             _1183_ (net)
                   0.07    0.00    6.42 ^ _3333_/D_N (sky130_fd_sc_hd__or4bb_2)
                   0.14    0.62    7.04 v _3333_/X (sky130_fd_sc_hd__or4bb_2)
     3    0.01                             _1190_ (net)
                   0.14    0.00    7.04 v _3334_/A (sky130_fd_sc_hd__buf_1)
                   0.14    0.23    7.27 v _3334_/X (sky130_fd_sc_hd__buf_1)
     8    0.02                             _1191_ (net)
                   0.14    0.00    7.27 v _3367_/A (sky130_fd_sc_hd__buf_1)
                   0.17    0.26    7.53 v _3367_/X (sky130_fd_sc_hd__buf_1)
     8    0.03                             _1206_ (net)
                   0.17    0.00    7.53 v _3378_/A2 (sky130_fd_sc_hd__a21o_2)
                   0.03    0.26    7.79 v _3378_/X (sky130_fd_sc_hd__a21o_2)
     1    0.00                             _0184_ (net)
                   0.03    0.00    7.79 v _3977_/D (sky130_fd_sc_hd__dfxtp_2)
                           7.79    data arrival time

                   0.15    8.00    8.00   clock i_clk (rise edge)
                           0.00    8.00   clock network delay (ideal)
                          -0.20    7.80   clock uncertainty
                           0.00    7.80   clock reconvergence pessimism
                           7.80 ^ _3977_/CLK (sky130_fd_sc_hd__dfxtp_2)
                          -0.08    7.72   library setup time
                           7.72    data required time
                           7.72    data required time
                          -7.79    data arrival time
-----------------------------------------------------------------------------
                          -0.07    slack (VIOLATED)
```

Figure 36:PL_RESIZER_DESIGN_OPTIMIZATIONS=0

```
Startpoint: i_wb_addr[1] (input port clocked by i_clk)
Endpoint: _3978_ (rising edge-triggered flip-flop clocked by i_clk)
Path Group: i_clk
Path Type: max
Fanout     Cap     Slew   Delay    Time   Description
                   0.15    0.00    0.00   clock i_clk (rise edge)
                           0.00    0.00   clock network delay (ideal)
                           4.40    4.40 v input external delay
                   0.01    0.00    4.40 v i_wb_addr[1] (in)
     1    0.00                             i_wb_addr[1] (net)
                   0.01    0.00    4.40 v input16/A (sky130_fd_sc_hd__buf_2)
                   0.07    0.16    4.56 v input16/X (sky130_fd_sc_hd__buf_2)
     5    0.03                             net16 (net)
                   0.07    0.00    4.56 v _1970_/A (sky130_fd_sc_hd__or2_1)
                   0.07    0.28    4.84 v _1970_/X (sky130_fd_sc_hd__or2_1)
     2    0.01                             _1600_ (net)
                   0.07    0.00    4.84 v _2052_/A (sky130_fd_sc_hd__clkbuf_2)
                   0.09    0.18    5.02 v _2052_/X (sky130_fd_sc_hd__clkbuf_2)
     8    0.02                             _1682_ (net)
                   0.09    0.00    5.02 v _2053_/C (sky130_fd_sc_hd__or4b_1)
                   0.12    0.55    5.57 v _2053_/X (sky130_fd_sc_hd__or4b_1)
     3    0.01                             _1683_ (net)
                   0.12    0.00    5.57 v _2055_/A (sky130_fd_sc_hd__and3_1)
                   0.06    0.20    5.77 v _2055_/X (sky130_fd_sc_hd__and3_1)
     3    0.01                             _1685_ (net)
                   0.06    0.00    5.77 v _3325_/A_N (sky130_fd_sc_hd__and4b_1)
                   0.06    0.25    6.02 ^ _3325_/X (sky130_fd_sc_hd__and4b_1)
     1    0.00                             _1182_ (net)
                   0.06    0.00    6.02 ^ _3326_/D1 (sky130_fd_sc_hd__o2111a_1)
                   0.10    0.22    6.24 ^ _3326_/X (sky130_fd_sc_hd__o2111a_1)
     2    0.01                             _1183_ (net)
                   0.10    0.00    6.24 ^ _3333_/D_N (sky130_fd_sc_hd__or4bb_2)
                   0.14    0.63    6.87 v _3333_/X (sky130_fd_sc_hd__or4bb_2)
     3    0.01                             _1190_ (net)
                   0.14    0.00    6.87 v _3334_/A (sky130_fd_sc_hd__clkbuf_2)
                   0.09    0.21    7.08 v _3334_/X (sky130_fd_sc_hd__clkbuf_2)
     8    0.02                             _1191_ (net)
                   0.09    0.00    7.08 v _3367_/A (sky130_fd_sc_hd__buf_2)
                   0.08    0.21    7.28 v _3367_/X (sky130_fd_sc_hd__buf_2)
     8    0.03                             _1206_ (net)
                   0.08    0.00    7.28 v _3381_/A2 (sky130_fd_sc_hd__a21o_1)
                   0.03    0.19    7.47 v _3381_/X (sky130_fd_sc_hd__a21o_1)
     1    0.00                             _0185_ (net)
                   0.03    0.00    7.47 v _3978_/D (sky130_fd_sc_hd__dfxtp_2)
                           7.47    data arrival time

                   0.15    8.00    8.00   clock i_clk (rise edge)
                           0.00    8.00   clock network delay (ideal)
                          -0.20    7.80   clock uncertainty
                           0.00    7.80   clock reconvergence pessimism
                           7.80 ^ _3978_/CLK (sky130_fd_sc_hd__dfxtp_2)
                          -0.08    7.72   library setup time
                           7.72    data required time
                           7.72    data required time
                          -7.47    data arrival time
-----------------------------------------------------------------------------
                           0.25    slack (MET)
```

Figure 36:PL_RESIZER_DESIGN_OPTIMIZATIONS=1

Part2- Edit CTS configurations to achieve the required target.

```
# cts defaults
set ::env(CLOCK_TREE_SYNTH) 1
set ::env(CTS_TARGET_SKEW) 20
set ::env(CTS_TOLERANCE) 10
set ::env(CTS_SINK_CLUSTERING_SIZE) 25
set ::env(CTS_SINK_CLUSTERING_MAX_DIAMETER) 50
set ::env(CTS_REPORT_TIMING) 1
set ::env(CTS_CLK_MAX_WIRE_LENGTH) 0
```

Figure 37: configurations of CTS

I decreased CTS_TARGET_SKEW (from 200ps to 20ps) and CTS_TOLERANCE (from 100 to 10) to have tight skew and don't make timing violations as I don't have big margin in slack.

Question4

Change DRT_OPT_ITERS variable in routing configuration and report the tradeoff between reported DRCs and runtime.

DRT_OPT_ITERS =1 → 3.5 minutes (1400 line from violations)

DRT_OPT_ITERS =100 → 8 minutes (0 violations)

detailed.drc - /home/opentools/OpenLane/designs/

File Edit Search Preferences Shell Macro Windows

```
violation type: MetSpc
  srcs: net:_0362_
  bbox = ( 22.165, 123.72 ) - ( 22.455, 123.815 ) on Layer met1
violation type: Short
  srcs: net:_1301_ net:_1556_
  bbox = ( 30.52, 91.175 ) - ( 30.66, 91.405 ) on Layer met1
violation type: Short
  srcs: net:_1301_ net:_1556_
  bbox = ( 30.52, 91.22 ) - ( 30.66, 91.36 ) on Layer met1
violation type: MetSpc
  srcs: net:_1187_
  bbox = ( 28.515, 121.68 ) - ( 28.59, 121.775 ) on Layer met1
violation type: Short
  srcs: net:_0386_ net:state\[1\]
  bbox = ( 99.98, 15.4 ) - ( 100.12, 15.54 ) on Layer met1
violation type: MetSpc
  srcs: net:_1634_ net:_1664_
  bbox = ( 93.045, 33.76 ) - ( 93.08, 33.9 ) on Layer met1
violation type: MetSpc
  srcs: net:_1869_
  bbox = ( 124.745, 25.46 ) - ( 125.035, 25.555 ) on Layer met1
violation type: Short
  srcs: net:_1634_ net:_1638_
  bbox = ( 91.24, 33.76 ) - ( 91.38, 33.9 ) on Layer met1
violation type: Short
  srcs: net:_0409_ net:_0412_
  bbox = ( 119.76, 23.56 ) - ( 119.9, 23.7 ) on Layer met1
violation type: Short
  srcs: net:_0384_ net:_1662_
  bbox = ( 126.2, 17.44 ) - ( 126.34, 17.58 ) on Layer met1
violation type: Short
  srcs: net:_0385_ net:_0438_
  bbox = ( 130.34, 20.16 ) - ( 130.48, 20.315 ) on Layer met1
violation type: Short
  srcs: net:_0385_ net:_0438_
  bbox = ( 130.34, 20.16 ) - ( 130.48, 20.3 ) on Layer met1
violation type: Short
  srcs: net:_0385_ net:_0438_
  bbox = ( 130.34, 20.16 ) - ( 130.555, 20.3 ) on Layer met1
violation type: Short
  srcs: net:_0410_ net:net26
  bbox = ( 106.88, 23.56 ) - ( 107.02, 23.7 ) on Layer met1
violation type: Short
  srcs: net:_1673_ net:_1678_
  bbox = ( 106.42, 31.72 ) - ( 106.56, 31.86 ) on Layer met1
violation type: Short
  srcs: net:_1639_ net:_1875_
```

Figure 38:detailed.drc

Question 5

- Open the final GDS and LEF of the design using Klayout and clarify the information represented in each view.

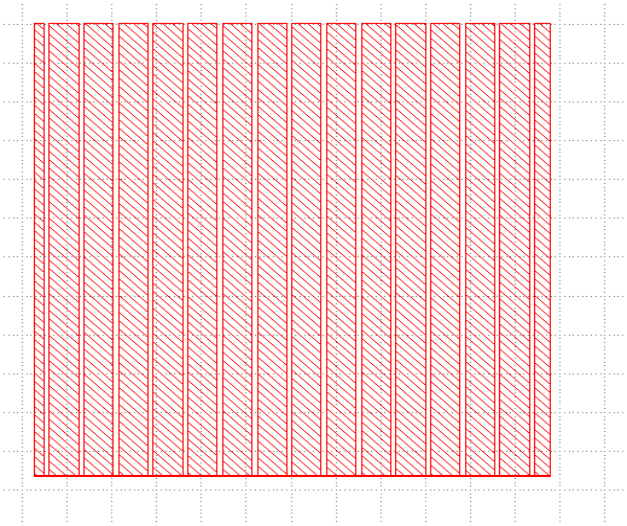


Figure 40: LEF obstructions

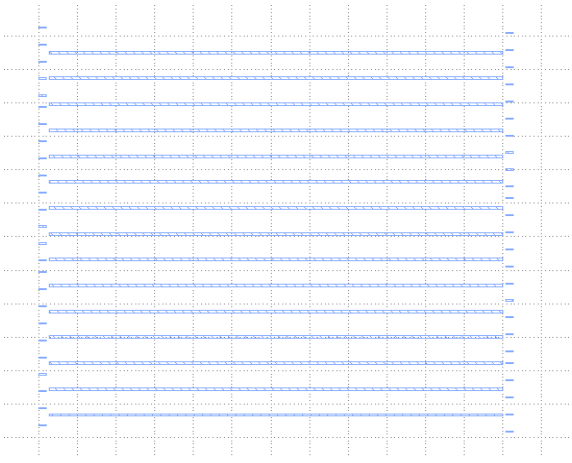


Figure 40: LEF bin locations

LEF contains detailed PIN information that is used by PnR tools to guide routing and Metal blockages (OBS section), that represent internal metal shapes of the cell not to be touched by routing.

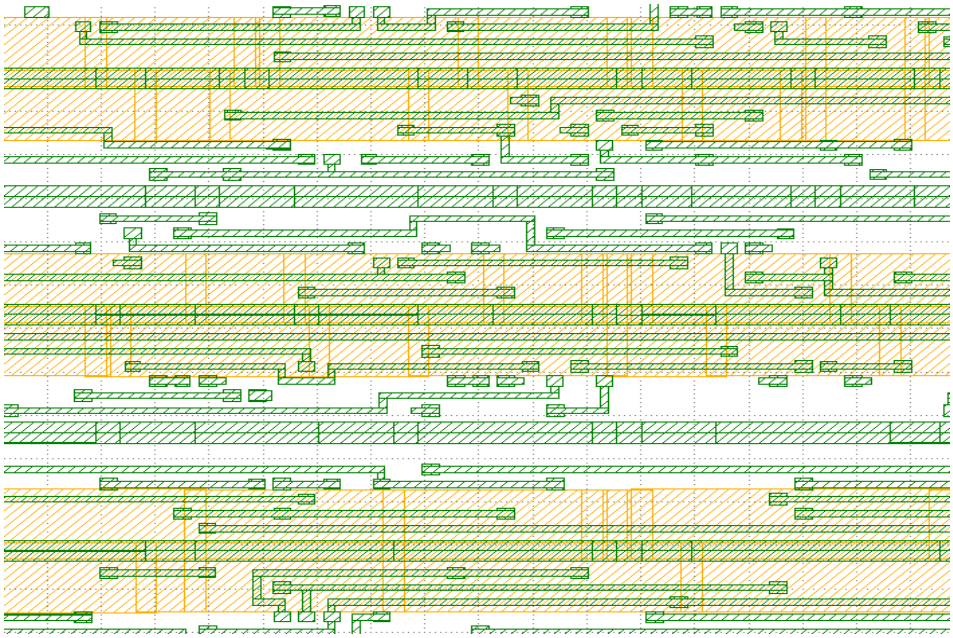


Figure 41: GDS by Klayout

GDS show all shapes and details.

Question 6

Using Klayout, validate the metals used for pins creation.

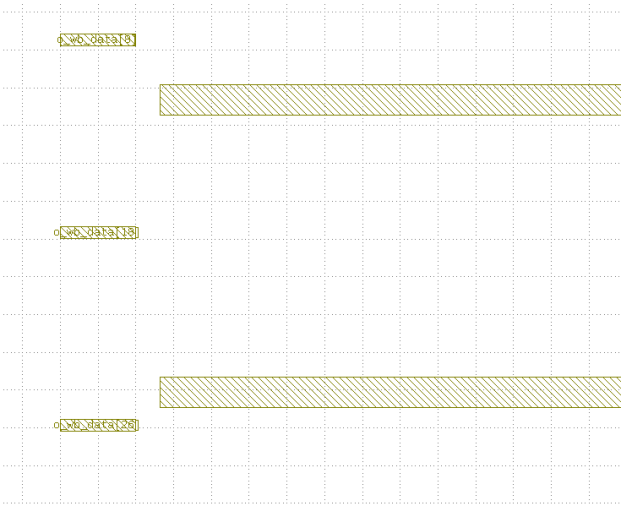


Figure 43: Horizontal bins in met3

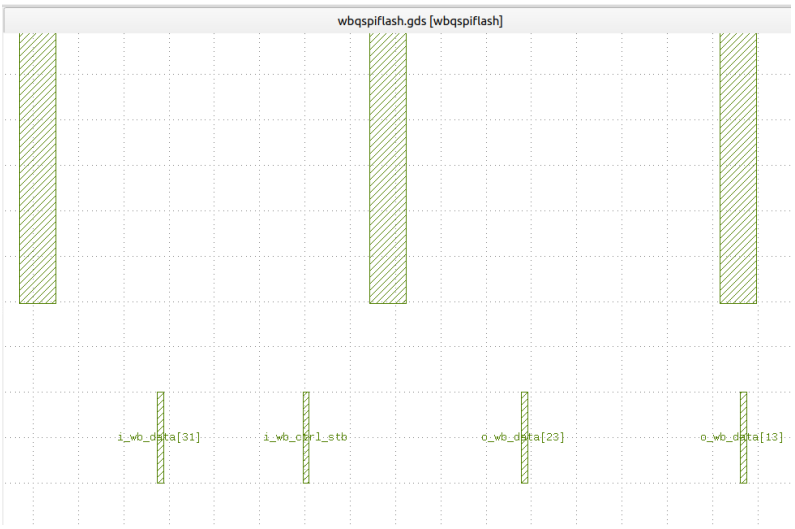


Figure 42: Vertical bins in met2

Which layer numbers map to met2 & met3?

Met2 69 , Met3 70

Question 7

- Validate that the LEF is created with the intended dimensions.

wbqspiflash.lef - /home/opentools/OpenLa

File Edit Search Preferences Shell Macro

```
 1 VERSION 5.7 ;
 2   NOWIREEXTENSIONATPIN ON ;
 3   DIVIDERCHAR "/" ;
 4   BUSBITCHARS "[]" ;
 5 MACRO wbqspiflash
 6   CLASS BLOCK ;
 7   FOREIGN wbqspiflash ;
 8   ORIGIN 0.000 0.000 ;
 9   SIZE 245.380 BY 250.660 ;
10   PIN VGND
11     DIRECTION INOUT ;
12     USE GROUND ;
13     PORT
14       LAYER met2 ;
15         RECT 25.510 7.920 27.1
16     END
```

Figure 44: LEF area

3-initial_fp_die_area.rpt - /home/opentools/Ope

File Edit Search Preferences Shell Macro Wi

```
1 0.0 0.0 245.38 250.66
```

Figure 45: floorplan area

The floorplan and the LEF have the same dimensions.

THANK YOU

I am immensely grateful for the opportunity to learn and grow during this internship. I hope I was responsible and any bad act was beyond my control. Your unwavering confidence in me has been truly inspiring. Thank you for shaping my journey into a valuable experience.