
STM32
CubeMX

1. Description

1.1. Project

Project Name	XC-GP4V1
Board Name	custom
Generated with:	STM32CubeMX 6.0.1
Date	12/28/2020

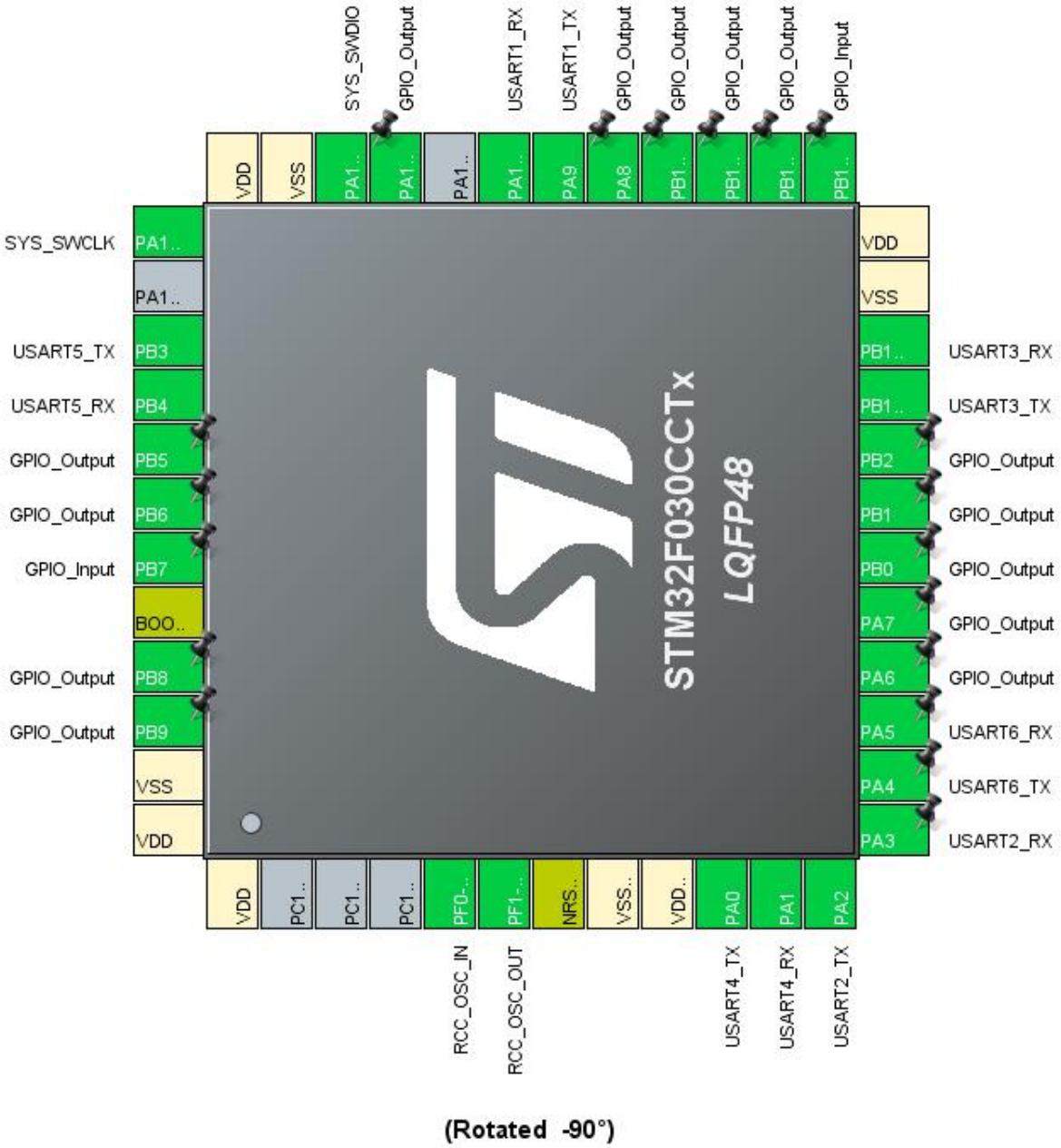
1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x0 Value Line
MCU name	STM32F030CCTx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M0

2. Pinout Configuration



(Rotated -90°)

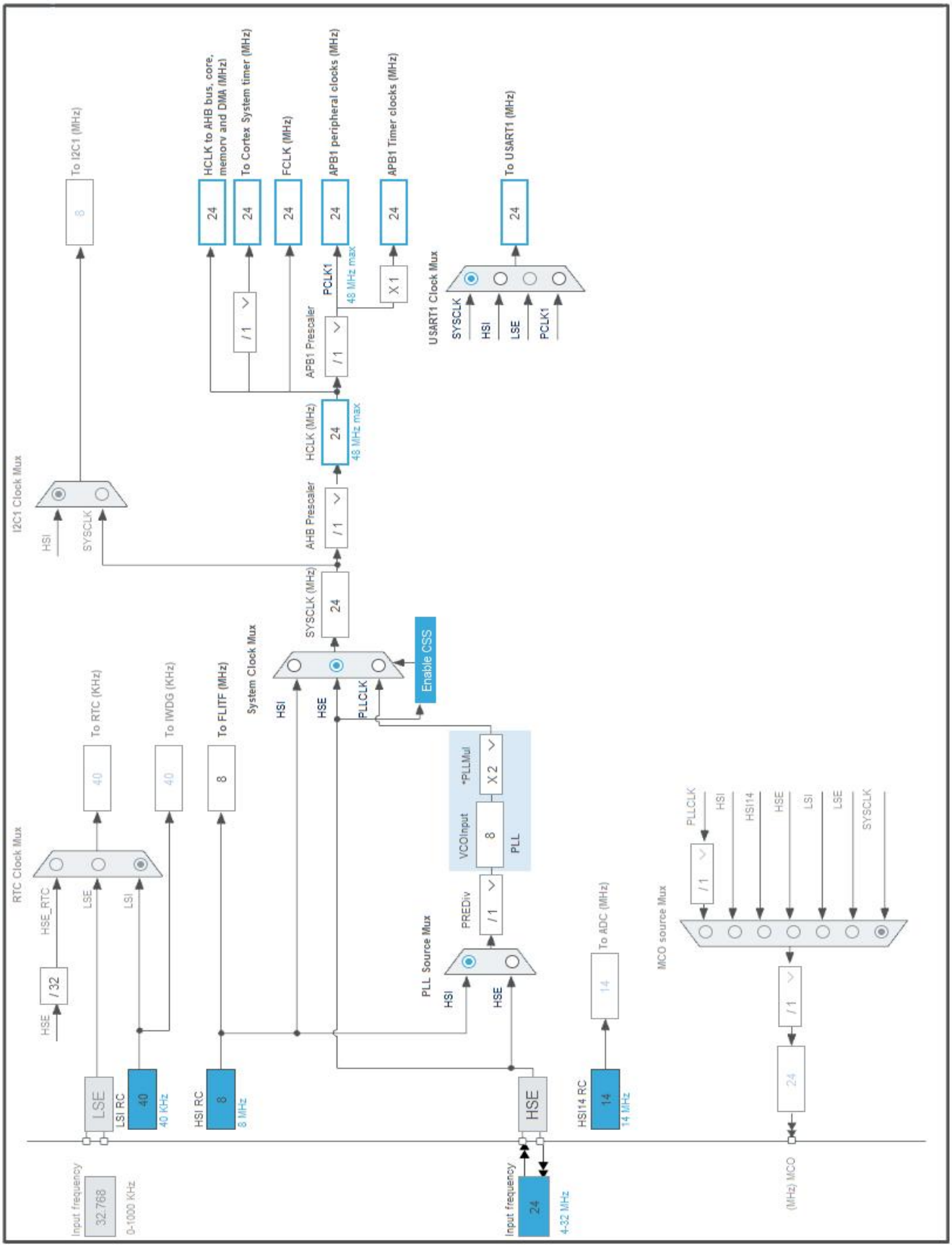
3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0	I/O	USART4_TX	
11	PA1	I/O	USART4_RX	
12	PA2	I/O	USART2_TX	
13	PA3	I/O	USART2_RX	
14	PA4	I/O	USART6_TX	
15	PA5	I/O	USART6_RX	
16	PA6 *	I/O	GPIO_Output	
17	PA7 *	I/O	GPIO_Output	
18	PB0 *	I/O	GPIO_Output	
19	PB1 *	I/O	GPIO_Output	
20	PB2 *	I/O	GPIO_Output	
21	PB10	I/O	USART3_TX	
22	PB11	I/O	USART3_RX	
23	VSS	Power		
24	VDD	Power		
25	PB12 *	I/O	GPIO_Input	
26	PB13 *	I/O	GPIO_Output	
27	PB14 *	I/O	GPIO_Output	
28	PB15 *	I/O	GPIO_Output	
29	PA8 *	I/O	GPIO_Output	
30	PA9	I/O	USART1_TX	
31	PA10	I/O	USART1_RX	
33	PA12 *	I/O	GPIO_Output	
34	PA13	I/O	SYS_SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_SWCLK	
39	PB3	I/O	USART5_TX	
40	PB4	I/O	USART5_RX	
41	PB5 *	I/O	GPIO_Output	

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
42	PB6 *	I/O	GPIO_Output	
43	PB7 *	I/O	GPIO_Input	
44	BOOT0	Boot		
45	PB8 *	I/O	GPIO_Output	
46	PB9 *	I/O	GPIO_Output	
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	XC-GP4V1.0
Project Folder	C:\Users\islam.bedair.ULTIMATRUE\Documents\STM32CubeMX Projects\XC-
Toolchain / IDE	EWARM V8.32
Firmware Package Name and Version	STM32Cube FW_F0 V1.11.2
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	Yes

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_USART1_UART_Init	USART1
4	MX_USART2_UART_Init	USART2
5	MX_USART3_UART_Init	USART3
6	MX_USART4_UART_Init	USART4
7	MX_USART5_UART_Init	USART5
8	MX_USART6_UART_Init	USART6
9	MX_TIM3_Init	TIM3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x0 Value Line
MCU	STM32F030CCTx
Datasheet	DS9773_Rev2

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

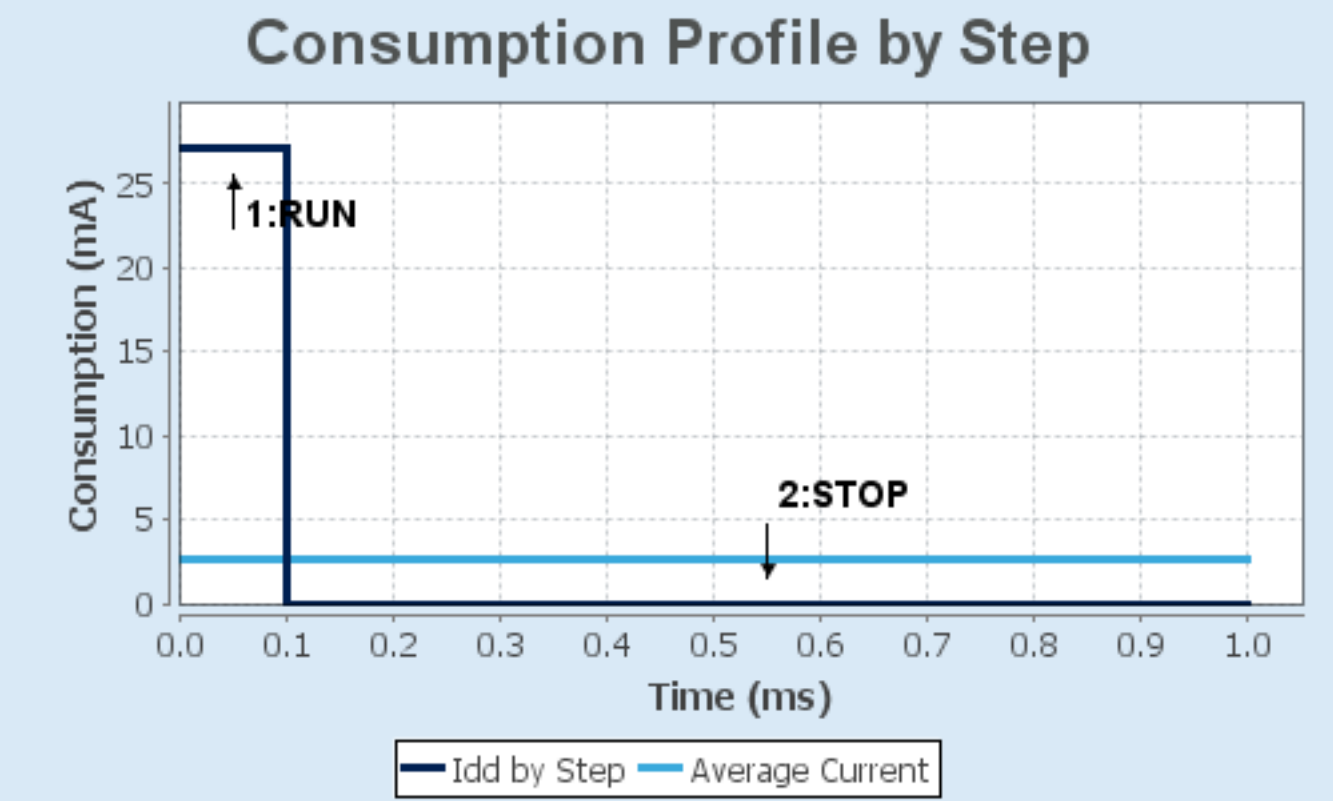
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	48 MHz	0 Hz
Clock Configuration	HSI PLL All IPs ON	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27.03 mA	7.9 µA
Duration	0.1 ms	0.9 ms
DMIPS	0.0	0.0
Ta Max	99.65	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days, 18 hours	Average DMIPS	0.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. GPIO

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.3. SYS

mode: Debug Serial Wire

Timebase Source: SysTick

7.4. TIM3

mode: Clock Source

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**24000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.5. USART1

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	**14400 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	**Enable ***
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

7.6. USART2

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	**14400 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable

RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

7.7. USART3

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	**14400 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	**Enable ***
Overrun	Enable
DMA on RX Error	**Disable ***
MSB First	Disable

7.8. USART4

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	**14400 ***
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	**Enable ***
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

7.9. USART5

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**14400 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	**Enable ***
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

7.10. USART6

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**14400 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	**Enable ***
Overrun	**Disable ***
DMA on RX Error	**Disable ***
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14	SYS_SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USART4	PA0	USART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA1	USART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USART5	PB3	USART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB4	USART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USART6	PA4	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA5	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
GPIO	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM3 global interrupt	true	0	0
USART1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
USART3 to USART6 global interrupts	true	0	0
Flash global interrupt	unused		
RCC global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
System service call via SWI instruction	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
TIM3 global interrupt	true	true	true
USART1 global interrupt	true	true	true
USART2 global interrupt	true	true	true
USART3 to USART6 global interrupts	true	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00088500.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00091010.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00051352.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00091791.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00052530.pdf
Application note	http://www.st.com/resource/en/application_note/DM00053084.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00089834.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00145318.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note	http://www.st.com/resource/en/application_note/DM00210690.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00188145.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00445657.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00483659.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf