CH32V103

Datasheet

WCH, @islandc_

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Table of Contents

Features

- WCH 32-bit RISC-V3A Core
  - RV32IMAC base ISA and extensions
  - 80MHz maximum operating frequency
  - Low-power two-stage instruction pipeline w/ static branch prediction
- Memory
  - 32 or 64kB of FLASH memory
  - 10 or 20kB of SRAM
  - 128B of non-volatile user configuration data
- Low Power
  - Sleep, Stop, Stand-by modes
  - Battery-backed RTC and backup registers
- Clock, Reset and Power Supply
  - Operating supply range: 2.7 to 5.5V
  - Factory-trimmed internal 8MHz RC oscillator
  - Internal 40kHz RC oscillator
  - PLL for system clock generation, up to 80MHz
  - External 4-16MHz XTAL oscillator for system clock
  - External 32.768kHz XTAL oscillator for RTC
  - Power-on/Power-down reset (POR/PDR), Programmable Voltage Detector (PVD)
- 12-bit 1MSps A/D Converter (up to 18 Channels)
  - Conversion range: 0 to V_{DDA} (5.5V max.)
  - Analog watchdog
  - 10/16 external channels, 2 internal channels
  - Temperature Sensor
- 10/16-channel *TouchKey* capacitive touch sensing peripheral
- 7-channel general purpose DMA controller
  - Ring buffer mode
  - Supported peripherals: timers, ADC, com. interfaces
- Up to 7 timers
  - 1 × 16-bit motor control timer with PWM outputs, dead time generation and emergency stop
  - Up to 3 × 16-bit timers, each with up to 4 IC/OC/PWM outputs or pulse counter / quadrature encoder inputs
  - 2 × watchdog timers (independent and window)
  - SysTick timer: 64-bit up-counter
- Up to 8 communication interfaces
  - USBHD 2.0FS host/device interface
  - Up to 2 × I²C interfaces (SMBus/PMBus)
  - Up to 2 × SPI (Master and Slave modes)
  - Up to 3 × USART (ISO 7816 interface, LIN, IrDA, flow control)
- Up to 51 fast I/O
  - 37/51 fast GPIO, mappable to 16 interrupts
- Debug mode: 2-wire serial debug interface (RVSWD)
- CRC calculation unit, 96-bit unique device ID
- Packages
  - QFN48 (7×7mm)
  - LQFP48 (7×7mm)
  - LQFP64 (10×10mm)

Description

CH32V103 series series MCU incorporate a 32-bit *RISC-V* RISC-V3A core based on the RV32IMAC open-standard ISA, high-speed embedded memories (up to 64kB of FLASH memory and up to 20kB of SRAM) with instruction pre-fetch and a wide range of I/O and peripherals. All series parts feature a 12-bit ADC with TouchKey, one advanced 16-bit timer capable of motor control applications plus a minimum of two 16-bit general purpose timers, as well as a range of communication interfaces including SPI, I²C, 2 × USART and USBHD 2.0FS host and device functionality.

The devices operate at a supply range of 2.7 to 5.5V, with a maximum core frequency of 80MHz. Core components and peripherals are interconnected via two APBs and one AHB, and clock supplies can be disabled and core power saving modes can be used for low-power applications. RTC and backup registers can be powered independently through a battery supply input. All series devices are capable of operating across the industrial grade temperature range between -40 and +85°C, and are available in package sizes QFN48, LQFP48 and LQFP64.

CH32V103 series devices are suitable for use in motor control applications, handheld equipment, PC peripheral devices and gaming peripherals, GPS platforms, PLCs, inverters, printers and scanners, video intercom systems and HVAC equipment.

Device overview

CH32V103 series devices are offered in three package variants spanning a set of four device models, each with a specific package, memory and peripherals configuration. All available configurations are shown in Model Comparison. The device internal block structure is shown in System Block Diagram and a more detailed clock distribution tree is shown in Clock Tree.

Model Comparison

Table 1. Model Comparison

	CH32V103C6T6	CH32V103C8T6	CH32V103C8U6	CH32V103R8T6
Number of pins	48	48	48	64
FLASH (bytes)	32K	64K	64K	64K
SRAM (bytes)	10K	20K	20K	20K
GPIO	37	37	37	51

		CH32V103C6T6	CH32V103C8T6	CH32V103C8U6	CH32V103R8T6
Timer	General-Purpose	2	3	3	3
	Advanced	1	1	1	1
	Watchdog (WDT)	2	2	2	2
	SysTick	1	1	1	1
ADC/Tkey Channels		10 + 2[1]	10 + 2[1]	10 + 2[1]	16 + 2[1]
Interfaces	SPI	1	2	2	2
	I²C	1	2	2	2
	USART	2	3	3	3
	USBHD 2.0FS	1	1	1	1
CPU frequency		72MHz typ.			
Operating voltage		2.7 to 5.5V			
Operating temperature		Industrial grade; -40 to +85°C			
Package		LQFP48 (7×7mm)		QFN48 (7×7mm)	LQFP64M (10×10mm)

System Block Diagram

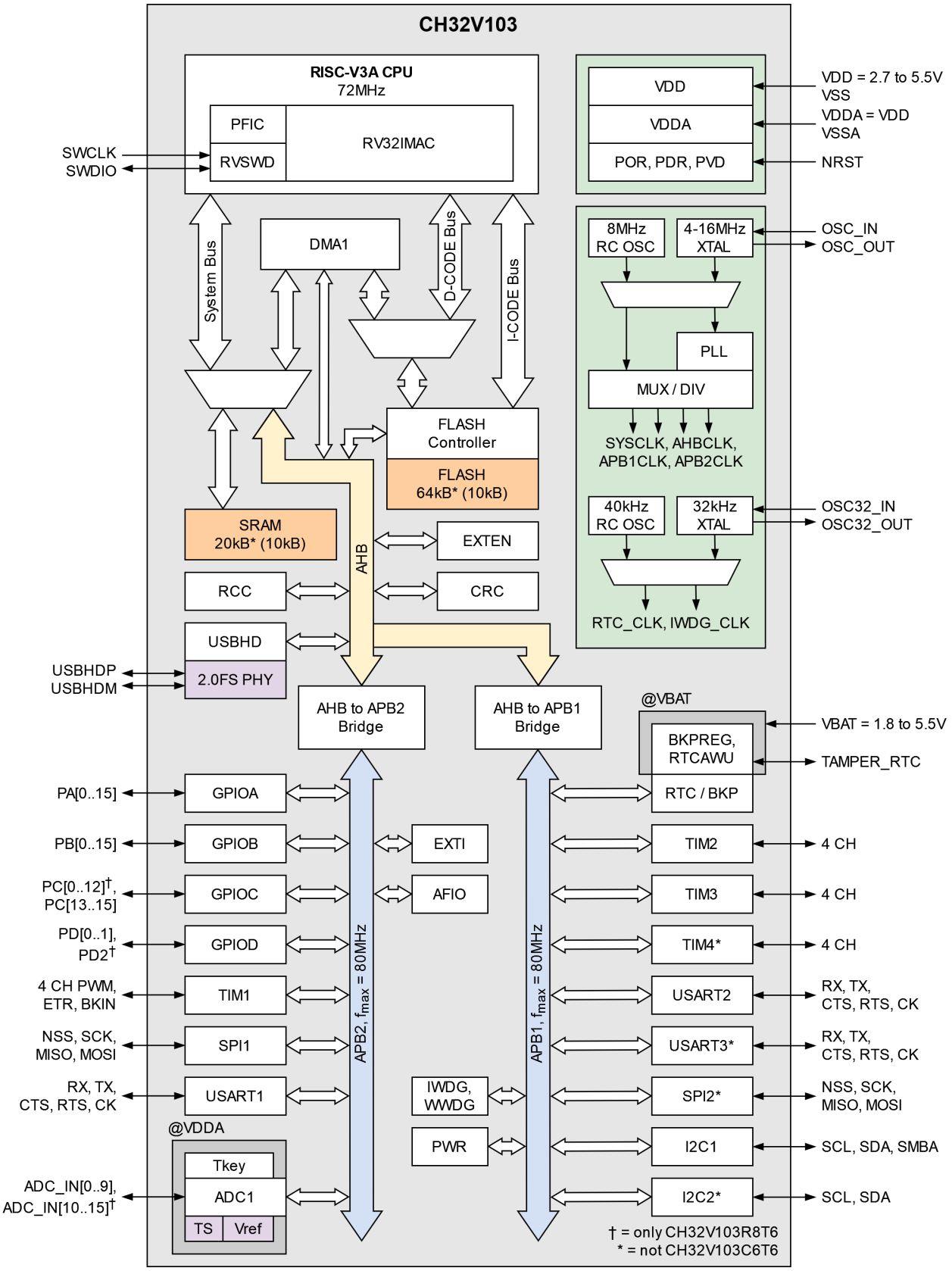

Figure 1. System Block Diagram

Clock Tree

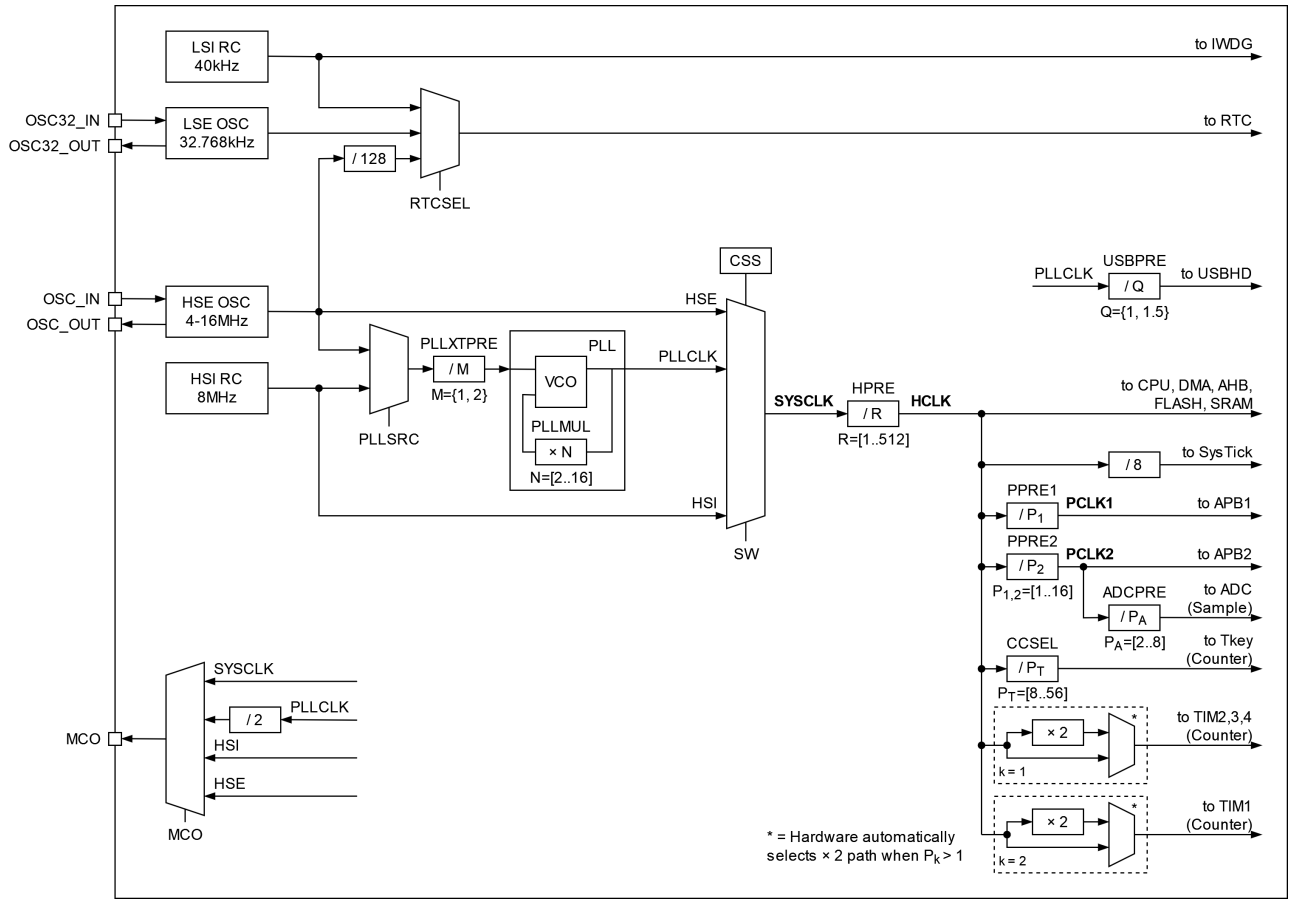

Figure 2. Clock Tree

Systems and features overview

RISC-V3A core

The *RISC-V3A* is a 32-bit RISC processor core developed and maintained in-house at WCH. It implements the RV32I *RISC-V* base ISA with hardware multiplication and division (M), atomic memory access (A) and compressed instructions (C), as well as vendor-specific extensions. *Machine* and *User* privilege levels are supported. Debugging access is provided via a two-wire serial interface.

- RV32IMAC base ISA and extensions
- Low-power 2-stage pipeline with static branch prediction
- Instruction pre-fetch buffer
- *Machine* and *User* privilege levels
- Programmable Fast Interrupt Controller (PFIC)
- Two-wire serial debugging interface

Embedded FLASH memory

Depending on model selection (see Model Comparison), either 32kB or 64kB of embedded FLASH

memory are available for code and read-only data storage. Higher AHB clock speeds may require additional access wait-states.

128 Bytes of persistent, application-defined data can be stored in a separate user configuratioin word.

Embedded SRAM

Up to 20kB of embedded SRAM are available for data and code storage, and can be accessed (read/write) at AHB clock speed without wait-states. Available memory is limited on smaller devices, as shown in Model Comparison.

CRC calculation unit (CRC)

The CRC unit can be used to calculate a CRC value from 32-bit data words and a fixed generator polynomial (CRC-32, `0x04C11DB7`). It can be utilised to verify the integrity of FLASH-memory contents against a known-good signature.

Programmable Fast Interrupt Controller (PFIC)

Incoming peripheral and core interrupt requests are managed by the built-in programmable fast interrupt controller, capable of handling 47 maskable interrupt channels and 16 priority levels.

- 44 peripheral + 3 core maskable interrupts
- Non-maskable core interrupt (NMI)
- Hardware stack management on interrupt entry and exit up to 2-level nesting
- Support for tail-chaining

External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains 20 edge detectors for generating interrupt/event requests. Each interrupt can be masked and configured to select the trigger event independently. Interrupt requests are latched in a pending register. External request lines support pulse widths shorter than the APB2 clock period. Up to 51 general-purpose I/Os can be connected to the 16 external interrupt lines.

Clocks and Startup

At powerup, the internal 8 MHz RC oscillator (HSI) is enabled automatically, and selected as the CPU core clock after reset or if no other clocks are configured. Afterwards, an external clock source (HSE) or PLL can be configured.

A clock monitoring system (CSS) can be enabled for HSE derived system clock. In case the external clock is determined to have failed, the CSS automatically will automatically revert the system clock configuration to HSI, and disable any active HSE or PLL. The CSS will also

automatically switch the clock configuration to HSI after wake-up from a low-power mode. Failure detection will also trigger the *non-maskable interrupt* (NMI).

High-speed and peripheral bus clock frequencies can be configured via a number of prescalers; see Clock Tree for further details on the clock distribution tree.

Boot Modes

The boot mode is set via two input pins `BOOT0` and `BOOT1`, and is latched at reset (reset event or power-on reset). See Table 2 for valid startup configurations.

Table 2. Boot Mode Selection

BOOT0	BOOT1	Mode Description
0	X	Startup from main program FLASH memory
1	0	Startup from System Memory
1	1	Startup from embedded SRAM

Depending on the selected mode, different memories will be remapped to address `0x00000000`:

- When startup from main program FLASH is selected, the FLASH memory starting at `0x08000000` will be remapped.
- When startup from System Memory is selected, the read-only FLASH memory starting at `0x1FFF0000` will be remapped.
- When startup from embedded SRAM is selected, **the memory will not be remapped**. Embedded SRAM can only be addressed directly starting at `0x20000000`.

Power supply and monitoring

Low power

[1] additional 2 channels dedicated to Temperature Sensor and Vref

Pinouts and Pin Description

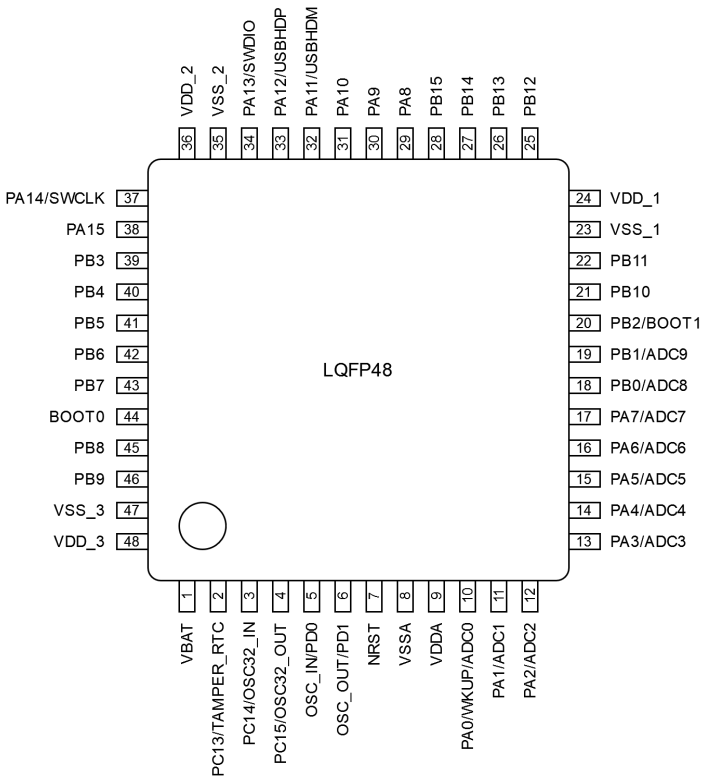

Figure 3. CH32V103CxT6 (LQFP48) pinout

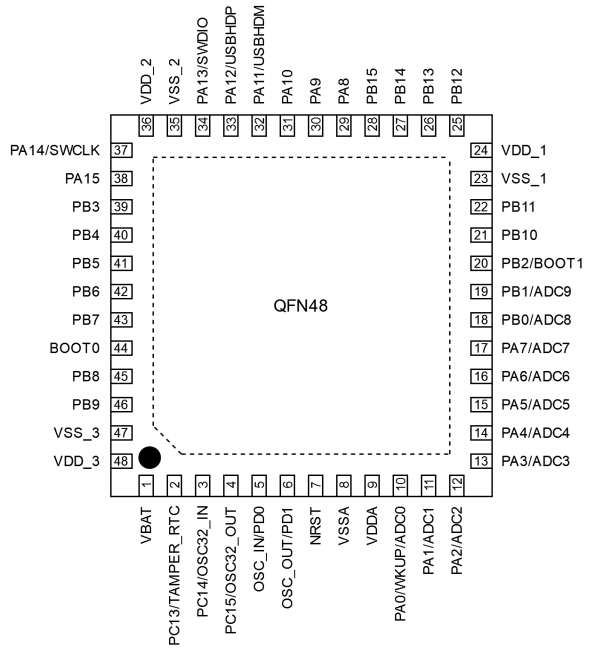

Figure 4. CH32V103C8U6 (QFN48) pinout

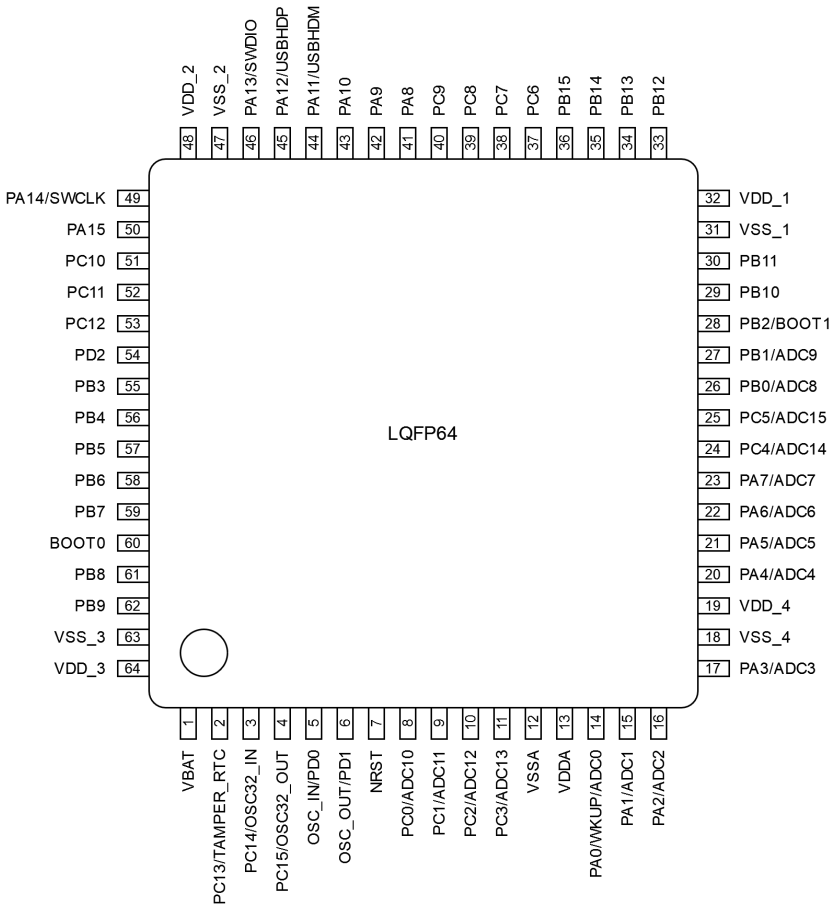

Figure 5. CH32V103R8T6 (LQFP64M) pinout