1. Description

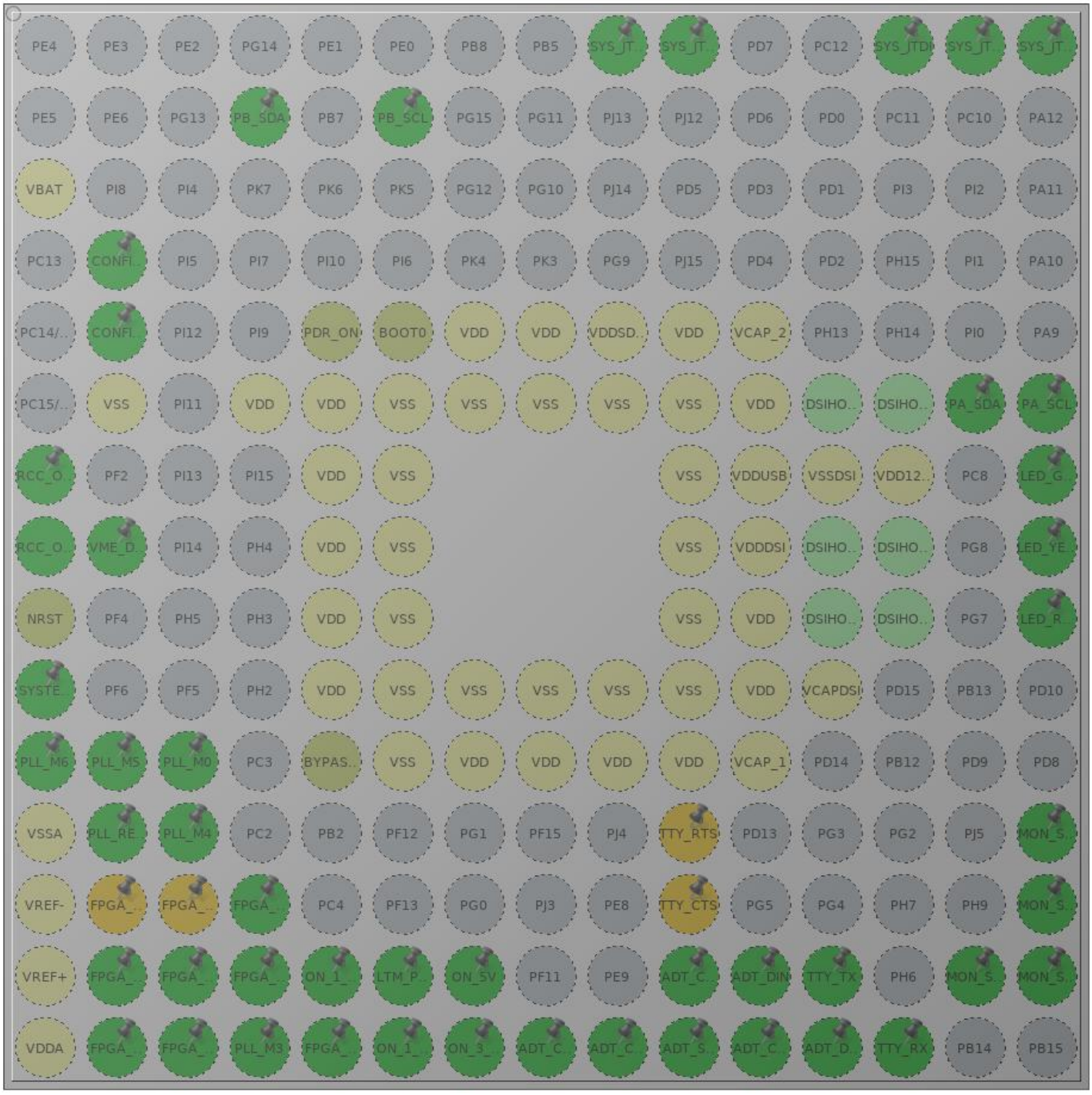
1.1. Project

Project Name	tdc72xvs4-rtos
Board Name	custom
Generated with:	STM32CubeMX 5.1.0
Date	04/01/2019

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x9
MCU name	STM32F769NIHx
MCU Package	TFBGA216
MCU Pin number	216

2. Pinout Configuration



TFBGA216 (Top view)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A9	PB4	I/O	SYS_JTRST	
A10	PB3	I/O	SYS_JTDO-SWO	
A13	PA15	I/O	SYS_JTDI	
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
B4	PB9	I/O	I2C1_SDA	PB_SDA
B6	PB6	I/O	I2C1_SCL	PB_SCL
C1	VBAT	Power		
D2	PF0	I/O	I2C2_SDA	CONFIG_IIC_SDA
E2	PF1	I/O	I2C2_SCL	CONFIG_IIC_SCL
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDDSDMMC	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F14	PC9	I/O	I2C3_SDA	PA_SDA
F15	PA8	I/O	I2C3_SCL	PA_SCL
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G12	VSSDSI	Power		
G13	VDD12DSI	Power		
G15	PC7 *	I/O	GPIO_Output	LED_GREEN_B

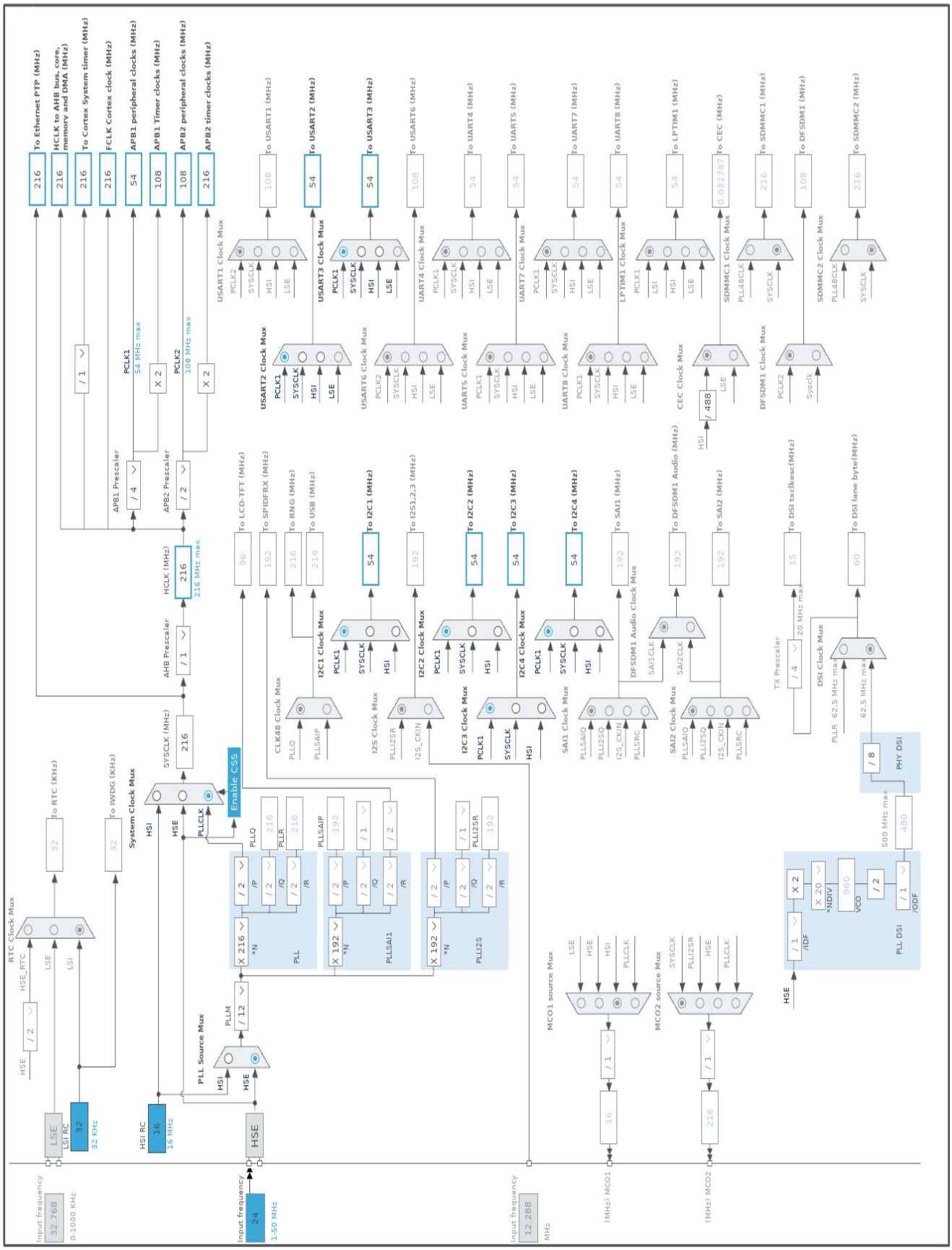
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3 *	I/O	GPIO_Input	VME_DET_B
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDDDSI	Power		
H15	PC6 *	I/O	GPIO_Output	LED_YELLOW_B
J1	NRST	Reset		
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
J15	PG6 *	I/O	GPIO_Output	LED_RED_B
K1	PF7 *	I/O	GPIO_Output	SYSTEM_RDY
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K12	VCAPDSI	Power		
L1	PF10 *	I/O	GPIO_Output	PLL_M6
L2	PF9 *	I/O	GPIO_Output	PLL_M5
L3	PF8	I/O	GPIO_EXTI8	PLL_M0
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
M1	VSSA	Power		
M2	PC0 *	I/O	GPIO_Output	PLL_RESET_B
M3	PC1 *	I/O	GPIO_Output	PLL_M4
M10	PD12 **	I/O	USART3_RTS	TTY_RTS
M15	PH12	I/O	I2C4_SDA	MON_SMB_DAT
N1	VREF-	Power		
N2	PA1 **	I/O	USART2_RTS	FPGA_UART_RTS

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
N3	PA0/WKUP **	I/O	USART2_CTS	FPGA_UART_CTS
N4	PA4 *	I/O	GPIO_Output	FPGA_NSS
N10	PD11 **	I/O	USART3_CTS	TTY_CTS
N15	PH11	I/O	I2C4_SCL	MON_SMB_CLK
P1	VREF+	Power		
P2	PA2	I/O	USART2_TX	FPGA_UART_TX
P3	PA6	I/O	SPI1_MISO	FPGA_MISO
P4	PA5	I/O	SPI1_SCK	FPGA_SCK
P5	PC5 *	I/O	GPIO_Output	ON_1_0V_1_2V
P6	PF14 *	I/O	GPIO_Input	LTM_PGOOD
P7	PJ2 *	I/O	GPIO_Output	ON_5V
P10	PE11 *	I/O	GPIO_Output	ADT_CS_B0
P11	PE14	I/O	SPI4_MOSI	ADT_DIN
P12	PB10	I/O	USART3_TX	TTY_TX
P14	PH8 *	I/O	GPIO_Output	MON_SMB_SW_RST_B
P15	PH10 *	I/O	GPIO_Input	MON_SMB_ALERT_B
R1	VDDA	Power		
R2	PA3	I/O	USART2_RX	FPGA_UART_RX
R3	PA7	I/O	SPI1_MOSI	FPGA_MOSI
R4	PB1 *	I/O	GPIO_Input	PLL_M3
R5	PB0 *	I/O	GPIO_Input	FPGA_CORE_PGOOD
R6	PJ0 *	I/O	GPIO_Output	ON_1_5V
R7	PJ1 *	I/O	GPIO_Output	ON_3_3V
R8	PE7 *	I/O	GPIO_Output	ADT_CS_B1
R9	PE10 *	I/O	GPIO_Output	ADT_CS_B2
R10	PE12	I/O	SPI4_SCK	ADT_SCLK
R11	PE15 *	I/O	GPIO_Output	ADT_CS_B3
R12	PE13	I/O	SPI4_MISO	ADT_DOUT
R13	PB11	I/O	USART3_RX	TTY_RX

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	tdc72xvs4-rtos
Project Folder	/home/islepnev/git/tdc72vxs4_rtos/cubemx
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x9
MCU	STM32F769NIHx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. GFXSIMULATOR

7.1.1. Simulator Graphic:

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	**25 ***
Fall Time (ns)	**25 ***
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00601B5E ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	**0x33 ***

7.3. I2C2

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	**25 ***
Fall Time (ns)	**25 ***
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00601B5E ***

Slave Features:

Clock No Stretch Mode	Disabled

General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. I2C3

I2C: SMBus-two-wire-Interface

7.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

SMBus Features:

Packet Error Check Mode	PEC Disabled
Peripheral Mode	Peripheral Mode Smbus Slave

SMBus Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	1

Timeout configuration:

Extended Clock Timeout	Disabled
Idle Clock Timeout Detection	Disabled
Timeout Time (ns)	25000000
Timeout	**0x00008293 ***

7.5. I2C4

I2C: I2C

7.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.6. RCC

High Speed Clock (HSE): BYPASS Clock Source

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

7.7. SPI1

Mode: Full-Duplex Master

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***

First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**27.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.8. SPI4

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**27.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.9. SYS

Debug: JTAG (5 pins)

Timebase Source: TIM1

7.10. USART2

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.11. USART3

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	**Enable ***
Auto Baudrate Mode	ON START BIT
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable

TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.12. FREERTOS

Interface: CMSIS_V1

7.12.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.0.1
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	**Enabled ***
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	**0x40000 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled

USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	**Enabled ***
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	**Option2 ***

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	**Enabled ***
USE_TRACE_FACILITY	**Enabled ***
USE_STATS_FORMATTING_FUNCTIONS	**Enabled ***

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.12.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	PB_SDA
	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	PB_SCL
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	CONFIG_IIC_SDA
	PF1	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	CONFIG_IIC_SCL
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	PA_SDA
	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	PA_SCL
I2C4	PH12	I2C4_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	MON_SMB_DAT
	PH11	I2C4_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	MON_SMB_CLK
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	FPGA_MISO
	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	FPGA_SCK
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	FPGA_MOSI
SPI4	PE14	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	ADT_DIN
	PE12	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	ADT_SCLK
	PE13	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	ADT_DOUT
SYS	PB4	SYS_JTRST	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
	PA15	SYS_JTDI	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	FPGA_UART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	FPGA_UART_RX
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TTY_TX
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TTY_RX
Single Mapped Signals	PD12	USART3_RTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TTY_RTS
	PA1	USART2_RTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	FPGA_UART_RTS
	PA0/WKUP	USART2_CTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	FPGA_UART_CTS
	PD11	USART3_CTS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TTY_CTS
GPIO	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN_B
	PF3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	VME_DET_B
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_YELLOW_B
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED_B
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SYSTEM_RDY
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_M6
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_M5
	PF8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	PLL_M0
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_RESET_B
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PLL_M4
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FPGA_NSS
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ON_1_0V_1_2V
	PF14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LTM_PGOOD
	PJ2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ON_5V
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADT_CS_B0
	PH8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MON_SMB_SW_RST_B

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PH10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	MON_SMB_ALERT_B
	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PLL_M3
	PB0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	FPGA_CORE_PGOOD
	PJ0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ON_1_5V
	PJ1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ON_3_3V
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADT_CS_B1
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADT_CS_B2
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADT_CS_B3

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
I2C1 event interrupt	true	5	0
I2C1 error interrupt	true	5	0
USART3 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line[9:5] interrupts	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
USART2 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		

*** User modified value**

9. Software Pack Report