ST75256

4 Level Gray Scale Dot Matrix LCD Controller/Driver

Datasheet

Version 0.4

Sitronix Technology Corporation

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1 INTRODUCTION

ST75256 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. It contains 256-segment and 162-common with 1-icon-common driver circuits. This chip can be connected directly to a microprocessor which accepts 8-bit parallel interface (8080-series or 6800-series type), 4-Line serial or I^2C interface. Display data is stored into an on-chip Display Data RAM (DDRAM). It performs the Display Data RAM read/write operation without external operating clock, and the power consumption can be minimized. In addition, since all necessary power supply circuits for LCD system are built-in, ST75256 constructs a LCD display system with the fewest components.

2 FEATURES

Single-chip LCD controller/driver

Driver Output Circuits

- 256-segment / 162-common + 1-icon-common

On-chip Display Data RAM

- Capacity: 256x 163x 2 = 83,456bits (Max)

Various Partial Display Features

- Applicable partial duty
- Partial window moving & data scrolling

Microprocessor Interface

- 8-bit parallel bi-directional interface supports 6800-series or 8080-series MPU
- 4-Line serial interface
- I^2C interface

On-chip Low Power Analog Circuit

- On-chip oscillator circuit
- Voltage booster with built-in boost-capacitors
- Extremely few external components: 4 capacitors
- Built-in voltage regulator with programmable contrast
- Built-in voltage follower supports LCD bias voltage
  Available bias: 1/9 ~ 1/14

Operating Voltage Range

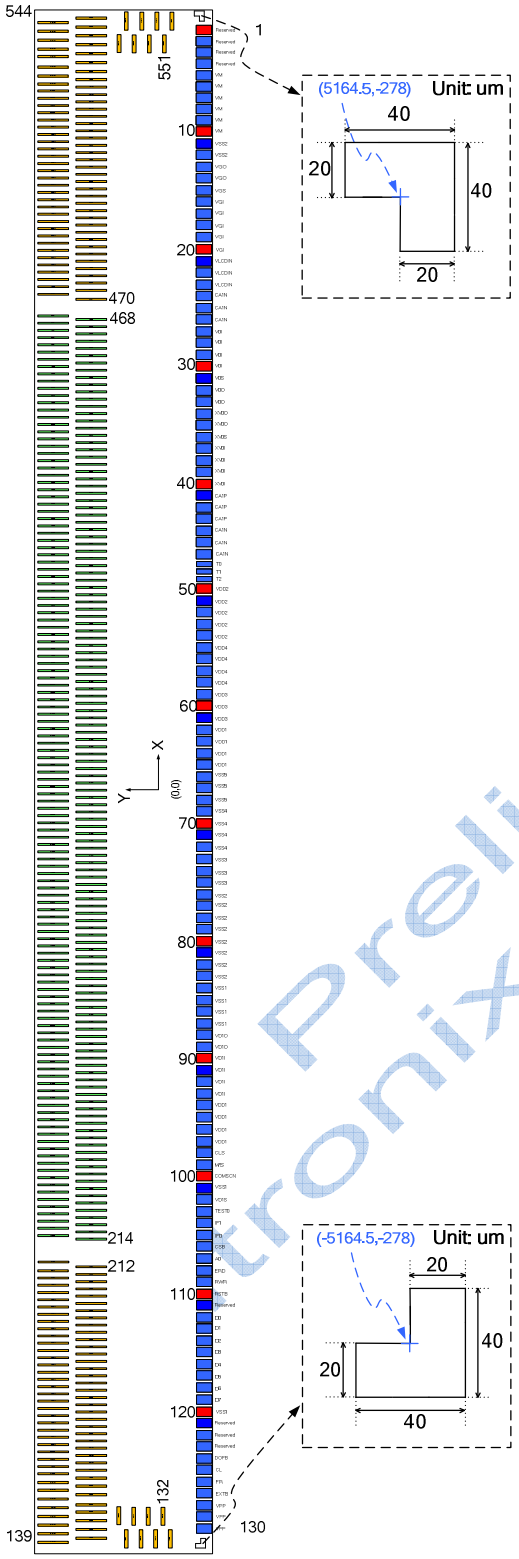
- Digital Power (VDD1): 1.8V ~ 3.3V (TYP.)
- Analog Power (VDD2~VDD4):
  2.8V ~ 3.3V (TYP.)
- LCD operation voltage (Vop = V0-XV0): 16V(Max.)

Built-in OTP−ROM for LCD Vop Optimization

Package Type: COG

ST75256	**6800 , 8080 , 4-Line Interface (without I^2C Interface)**	
ST75256i	**I^2C Interface**	

3 PAD ARRANGEMENT



Chip Size		10500x725	
Chip Thickness	480	Gold Bump	12
PAD No.		**Bump Size**	
1~46, 50~97, 128~130,		62x63	
98~105, 110~127		60x63	
47~49		22x63	
106~109		72x63	
131~138, 545~552		111x14	
139~544		14x111	
PAD No.		**Bump Pitch**	
1~46, 50~97, 128~130,		80	
46~47, 49~50		60	
47~49		40	
97~98, 127~128		79	
98~105, 110~127		78	
105~106, 109~110		84	
106~109		90	
131~552		25	
* Refer to “PAD CENTER COORDINATES” for ITO layout			

Unit: um

Figure 1 Chip Outline

4 PAD CENTER COORDINATES

PAD	NAME	X	Y
1	Reserved	5094	-273.5
2	Reserved	5014	-273.5
3	Reserved	4934	-273.5
4	Reserved	4854	-273.5
5	VM	4774	-273.5
6	VM	4694	-273.5
7	VM	4614	-273.5
8	VM	4534	-273.5
9	VM	4454	-273.5
10	VM	4374	-273.5
11	VSS2	4294	-273.5
12	VSS2	4214	-273.5
13	VGO	4134	-273.5
14	VGO	4054	-273.5
15	VGS	3974	-273.5
16	VGI	3894	-273.5
17	VGI	3814	-273.5
18	VGI	3734	-273.5
19	VGI	3654	-273.5
20	VGI	3574	-273.5
21	VLCDIN	3494	-273.5
22	VLCDIN	3414	-273.5
23	VLCDIN	3334	-273.5
24	CA1N	3254	-273.5
25	CA1N	3174	-273.5
26	CA1N	3094	-273.5
27	V0I	3014	-273.5
28	V0I	2934	-273.5
29	V0I	2854	-273.5
30	V0I	2774	-273.5
31	V0S	2694	-273.5
32	V0O	2614	-273.5
33	V0O	2534	-273.5

PAD	NAME	X	Y
34	XV0O	2454	-273.5
35	XV0O	2374	-273.5
36	XV0S	2294	-273.5
37	XV0I	2214	-273.5
38	XV0I	2134	-273.5
39	XV0I	2054	-273.5
40	XV0I	1974	-273.5
41	CA1P	1894	-273.5
42	CA1P	1814	-273.5
43	CA1P	1734	-273.5
44	CA1N	1654	-273.5
45	CA1N	1574	-273.5
46	CA1N	1494	-273.5
47	T0	1434	-273.5
48	T1	1394	-273.5
49	T2	1354	-273.5
50	VDD2	1294	-273.5
51	VDD2	1214	-273.5
52	VDD2	1134	-273.5
53	VDD2	1054	-273.5
54	VDD2	974	-273.5
55	VDD4	894	-273.5
56	VDD4	814	-273.5
57	VDD4	734	-273.5
58	VDD4	654	-273.5
59	VDD3	574	-273.5
60	VDD3	494	-273.5
61	VDD3	414	-273.5
62	VDD1	334	-273.5
63	VDD1	254	-273.5
64	VDD1	174	-273.5
65	VDD1	94	-273.5
66	VSS5	14	-273.5

PAD	NAME	X	Y
67	VSS5	-66	-273.5
68	VSS5	-146	-273.5
69	VSS4	-226	-273.5
70	VSS4	-306	-273.5
71	VSS4	-386	-273.5
72	VSS4	-466	-273.5
73	VSS3	-546	-273.5
74	VSS3	-626	-273.5
75	VSS3	-706	-273.5
76	VSS2	-786	-273.5
77	VSS2	-866	-273.5
78	VSS2	-946	-273.5
79	VSS2	-1026	-273.5
80	VSS2	-1106	-273.5
81	VSS2	-1186	-273.5
82	VSS2	-1266	-273.5
83	VSS2	-1346	-273.5
84	VSS1	-1426	-273.5
85	VSS1	-1506	-273.5
86	VSS1	-1586	-273.5
87	VSS1	-1666	-273.5
88	VD1O	-1746	-273.5
89	VD1O	-1826	-273.5
90	VD1I	-1906	-273.5
91	VD1I	-1986	-273.5
92	VD1I	-2066	-273.5
93	VD1I	-2146	-273.5
94	VDD1	-2226	-273.5
95	VDD1	-2306	-273.5
96	VDD1	-2386	-273.5
97	VDD1	-2466	-273.5
98	CLS	-2545	-273.5
99	M/S	-2623	-273.5
100	COMSCN	-2701	-273.5
101	VSS1	-2779	-273.5

PAD	NAME	X	Y
102	VD1S	-2857	-273.5
103	TEST0	-2935	-273.5
104	IF1	-3013	-273.5
105	IF0	-3091	-273.5
106	CSB	-3175	-273.5
107	A0	-3265	-273.5
108	ERD	-3355	-273.5
109	RWR	-3445	-273.5
110	RSTB	-3529	-273.5
111	Reserved	-3607	-273.5
112	D0	-3685	-273.5
13	D1	-3763	-273.5
114	D2	-3841	-273.5
115	D3	-3919	-273.5
116	D4	-3997	-273.5
117	D5	-4075	-273.5
118	D6	-4153	-273.5
119	D7	-4231	-273.5
120	VSS1	-4309	-273.5
121	Reserved	-4387	-273.5
122	Reserved	-4465	-273.5
123	Reserved	-4543	-273.5
124	DOFB	-4621	-273.5
125	CL	-4699	-273.5
126	FR	-4777	-273.5
127	EXTB	-4855	-273.5
128	VPP	-4934	-273.5
129	VPP	-5014	-273.5
130	VPP	-5094	-273.5
131	COMS	-5136	-186
132	COM161	-5005	-161
133	COM159	-5136	-136
134	COM157	-5005	-111
135	COM155	-5136	-86
136	COM153	-5005	-61

PAD	NAME	X	Y
137	COM151	-5136	-36
138	COM149	-5005	-11
139	COM147	-5157.5	249.5
140	COM145	-5132.5	118.5
141	COM143	-5107.5	249.5
142	COM141	-5082.5	118.5
143	COM139	-5057.5	249.5
144	COM137	-5032.5	118.5
145	COM135	-5007.5	249.5
146	COM133	-4982.5	118.5
147	COM131	-4957.5	249.5
148	COM129	-4932.5	118.5
149	COM127	-4907.5	249.5
150	COM125	-4882.5	118.5
151	COM123	-4857.5	249.5
152	COM121	-4832.5	118.5
153	COM119	-4807.5	249.5
154	COM117	-4782.5	118.5
155	COM115	-4757.5	249.5
156	COM113	-4732.5	118.5
157	COM111	-4707.5	249.5
158	COM109	-4682.5	118.5
159	COM107	-4657.5	249.5
160	COM105	-4632.5	118.5
161	COM103	-4607.5	249.5
162	COM101	-4582.5	118.5
163	COM99	-4557.5	249.5
164	COM97	-4532.5	118.5
165	COM95	-4507.5	249.5
166	COM93	-4482.5	118.5
167	COM91	-4457.5	249.5
168	COM89	-4432.5	118.5
169	COM87	-4407.5	249.5
170	COM85	-4382.5	118.5
171	COM83	-4357.5	249.5

PAD	NAME	X	Y
172	COM81	-4332.5	118.5
173	COM79	-4307.5	249.5
174	COM77	-4282.5	118.5
175	COM75	-4257.5	249.5
176	COM73	-4232.5	118.5
177	COM71	-4207.5	249.5
178	COM69	-4182.5	118.5
179	COM67	-4157.5	249.5
180	COM65	-4132.5	118.5
181	COM63	-4107.5	249.5
182	COM61	-4082.5	118.5
183	COM59	-4057.5	249.5
184	COM57	-4032.5	118.5
185	COM55	-4007.5	249.5
186	COM53	-3982.5	118.5
187	COM51	-3957.5	249.5
188	COM49	-3932.5	118.5
189	COM47	-3907.5	249.5
190	COM45	-3882.5	118.5
191	COM43	-3857.5	249.5
192	COM41	-3832.5	118.5
193	COM39	-3807.5	249.5
194	COM37	-3782.5	118.5
195	COM35	-3757.5	249.5
196	COM33	-3732.5	118.5
197	COM31	-3707.5	249.5
198	COM29	-3682.5	118.5
199	COM27	-3657.5	249.5
200	COM25	-3632.5	118.5
201	COM23	-3607.5	249.5
202	COM21	-3582.5	118.5
203	COM19	-3557.5	249.5
204	COM17	-3532.5	118.5
205	COM15	-3507.5	249.5
206	COM13	-3482.5	118.5

PAD	NAME	X	Y
207	COM11	-3457.5	249.5
208	COM9	-3432.5	118.5
209	COM7	-3407.5	249.5
210	COM5	-3382.5	118.5
211	COM3	-3357.5	249.5
212	COM1	-3332.5	118.5
213	COMS	-3307.5	249.5
214	SEG255	-3187.5	118.5
215	SEG254	-3162.5	249.5
216	SEG253	-3137.5	118.5
217	SEG252	-3112.5	249.5
218	SEG251	-3087.5	118.5
219	SEG250	-3062.5	249.5
220	SEG249	-3037.5	118.5
221	SEG248	-3012.5	249.5
222	SEG247	-2987.5	118.5
223	SEG246	-2962.5	249.5
224	SEG245	-2937.5	118.5
225	SEG244	-2912.5	249.5
226	SEG243	-2887.5	118.5
227	SEG242	-2862.5	249.5
228	SEG241	-2837.5	118.5
229	SEG240	-2812.5	249.5
230	SEG239	-2787.5	118.5
231	SEG238	-2762.5	249.5
232	SEG237	-2737.5	118.5
233	SEG236	-2712.5	249.5
234	SEG235	-2687.5	118.5
235	SEG234	-2662.5	249.5
236	SEG233	-2637.5	118.5
237	SEG232	-2612.5	249.5
238	SEG231	-2587.5	118.5
239	SEG230	-2562.5	249.5
240	SEG229	-2537.5	118.5
241	SEG228	-2512.5	249.5

PAD	NAME	X	Y
242	SEG227	-2487.5	118.5
243	SEG226	-2462.5	249.5
244	SEG225	-2437.5	118.5
245	SEG224	-2412.5	249.5
246	SEG223	-2387.5	118.5
247	SEG222	-2362.5	249.5
248	SEG221	-2337.5	118.5
249	SEG220	-2312.5	249.5
250	SEG219	-2287.5	118.5
251	SEG218	-2262.5	249.5
252	SEG217	-2237.5	118.5
253	SEG216	-2212.5	249.5
254	SEG215	-2187.5	118.5
255	SEG214	-2162.5	249.5
256	SEG213	-2137.5	118.5
257	SEG212	-2112.5	249.5
258	SEG211	-2087.5	118.5
259	SEG210	-2062.5	249.5
260	SEG209	-2037.5	118.5
261	SEG208	-2012.5	249.5
262	SEG207	-1987.5	118.5
263	SEG206	-1962.5	249.5
264	SEG205	-1937.5	118.5
265	SEG204	-1912.5	249.5
266	SEG203	-1887.5	118.5
267	SEG202	-1862.5	249.5
268	SEG201	-1837.5	118.5
269	SEG200	-1812.5	249.5
270	SEG199	-1787.5	118.5
271	SEG198	-1762.5	249.5
272	SEG197	-1737.5	118.5
273	SEG196	-1712.5	249.5
274	SEG195	-1687.5	118.5
275	SEG194	-1662.5	249.5
276	SEG193	-1637.5	118.5

PAD	NAME	X	Y
277	SEG192	-1612.5	249.5
278	SEG191	-1587.5	118.5
279	SEG190	-1562.5	249.5
280	SEG189	-1537.5	118.5
281	SEG188	-1512.5	249.5
282	SEG187	-1487.5	118.5
283	SEG186	-1462.5	249.5
284	SEG185	-1437.5	118.5
285	SEG184	-1412.5	249.5
286	SEG183	-1387.5	118.5
287	SEG182	-1362.5	249.5
288	SEG181	-1337.5	118.5
289	SEG180	-1312.5	249.5
290	SEG179	-1287.5	118.5
291	SEG178	-1262.5	249.5
292	SEG177	-1237.5	118.5
293	SEG176	-1212.5	249.5
294	SEG175	-1187.5	118.5
295	SEG174	-1162.5	249.5
296	SEG173	-1137.5	118.5
297	SEG172	-1112.5	249.5
298	SEG171	-1087.5	118.5
299	SEG170	-1062.5	249.5
300	SEG169	-1037.5	118.5
301	SEG168	-1012.5	249.5
302	SEG167	-987.5	118.5
303	SEG166	-962.5	249.5
304	SEG165	-937.5	118.5
305	SEG164	-912.5	249.5
306	SEG163	-887.5	118.5
307	SEG162	-862.5	249.5
308	SEG161	-837.5	118.5
309	SEG160	-812.5	249.5
310	SEG159	-787.5	118.5
311	SEG158	-762.5	249.5

PAD	NAME	X	Y
312	SEG157	-737.5	118.5
313	SEG156	-712.5	249.5
314	SEG155	-687.5	118.5
315	SEG154	-662.5	249.5
316	SEG153	-637.5	118.5
317	SEG152	-612.5	249.5
318	SEG151	-587.5	118.5
319	SEG150	-562.5	249.5
320	SEG149	-537.5	118.5
321	SEG148	-512.5	249.5
322	SEG147	-487.5	118.5
323	SEG146	-462.5	249.5
324	SEG145	-437.5	118.5
325	SEG144	-412.5	249.5
326	SEG143	-387.5	118.5
327	SEG142	-362.5	249.5
328	SEG141	-337.5	118.5
329	SEG140	-312.5	249.5
330	SEG139	-287.5	118.5
331	SEG138	-262.5	249.5
332	SEG137	-237.5	118.5
333	SEG136	-212.5	249.5
334	SEG135	-187.5	118.5
335	SEG134	-162.5	249.5
336	SEG133	-137.5	118.5
337	SEG132	-112.5	249.5
338	SEG131	-87.5	118.5
339	SEG130	-62.5	249.5
340	SEG129	-37.5	118.5
341	SEG128	-12.5	249.5
342	SEG127	12.5	118.5
343	SEG126	37.5	249.5
344	SEG125	62.5	118.5
345	SEG124	87.5	249.5
346	SEG123	112.5	118.5

PAD	NAME	X	Y
347	SEG122	137.5	249.5
348	SEG121	162.5	118.5
349	SEG120	187.5	249.5
350	SEG119	212.5	118.5
351	SEG118	237.5	249.5
352	SEG117	262.5	118.5
353	SEG116	287.5	249.5
354	SEG115	312.5	118.5
355	SEG114	337.5	249.5
356	SEG113	362.5	118.5
357	SEG112	387.5	249.5
358	SEG111	412.5	118.5
359	SEG110	437.5	249.5
360	SEG109	462.5	118.5
361	SEG108	487.5	249.5
362	SEG107	512.5	118.5
363	SEG106	537.5	249.5
364	SEG105	562.5	118.5
365	SEG104	587.5	249.5
366	SEG103	612.5	118.5
367	SEG102	637.5	249.5
368	SEG101	662.5	118.5
369	SEG100	687.5	249.5
370	SEG99	712.5	118.5
371	SEG98	737.5	249.5
372	SEG97	762.5	118.5
373	SEG96	787.5	249.5
374	SEG95	812.5	118.5
375	SEG94	837.5	249.5
376	SEG93	862.5	118.5
377	SEG92	887.5	249.5
378	SEG91	912.5	118.5
379	SEG90	937.5	249.5
380	SEG89	962.5	118.5
381	SEG88	987.5	249.5

PAD	NAME	X	Y
382	SEG87	1012.5	118.5
383	SEG86	1037.5	249.5
384	SEG85	1062.5	118.5
385	SEG84	1087.5	249.5
386	SEG83	1112.5	118.5
387	SEG82	1137.5	249.5
388	SEG81	1162.5	118.5
389	SEG80	1187.5	249.5
390	SEG79	1212.5	118.5
391	SEG78	1237.5	249.5
392	SEG77	1262.5	118.5
393	SEG76	1287.5	249.5
394	SEG75	1312.5	118.5
395	SEG74	1337.5	249.5
396	SEG73	1362.5	118.5
397	SEG72	1387.5	249.5
398	SEG71	1412.5	118.5
399	SEG70	1437.5	249.5
400	SEG69	1462.5	118.5
401	SEG68	1487.5	249.5
402	SEG67	1512.5	118.5
403	SEG66	1537.5	249.5
404	SEG65	1562.5	118.5
405	SEG64	1587.5	249.5
406	SEG63	1612.5	118.5
407	SEG62	1637.5	249.5
408	SEG61	1662.5	118.5
409	SEG60	1687.5	249.5
410	SEG59	1712.5	118.5
411	SEG58	1737.5	249.5
412	SEG57	1762.5	118.5
413	SEG56	1787.5	249.5
414	SEG55	1812.5	118.5
415	SEG54	1837.5	249.5
416	SEG53	1862.5	118.5

PAD	NAME	X	Y
417	SEG52	1887.5	249.5
418	SEG51	1912.5	118.5
419	SEG50	1937.5	249.5
420	SEG49	1962.5	118.5
421	SEG48	1987.5	249.5
422	SEG47	2012.5	118.5
423	SEG46	2037.5	249.5
424	SEG45	2062.5	118.5
425	SEG44	2087.5	249.5
426	SEG43	2112.5	118.5
427	SEG42	2137.5	249.5
428	SEG41	2162.5	118.5
429	SEG40	2187.5	249.5
430	SEG39	2212.5	118.5
431	SEG38	2237.5	249.5
432	SEG37	2262.5	118.5
433	SEG36	2287.5	249.5
434	SEG35	2312.5	118.5
435	SEG34	2337.5	249.5
436	SEG33	2362.5	118.5
437	SEG32	2387.5	249.5
438	SEG31	2412.5	118.5
439	SEG30	2437.5	249.5
440	SEG29	2462.5	118.5
441	SEG28	2487.5	249.5
442	SEG27	2512.5	118.5
443	SEG26	2537.5	249.5
444	SEG25	2562.5	118.5
445	SEG24	2587.5	249.5
446	SEG23	2612.5	118.5
447	SEG22	2637.5	249.5
448	SEG21	2662.5	118.5
449	SEG20	2687.5	249.5
450	SEG19	2712.5	118.5
451	SEG18	2737.5	249.5

PAD	NAME	X	Y
452	SEG17	2762.5	118.5
453	SEG16	2787.5	249.5
454	SEG15	2812.5	118.5
455	SEG14	2837.5	249.5
456	SEG13	2862.5	118.5
457	SEG12	2887.5	249.5
458	SEG11	2912.5	118.5
459	SEG10	2937.5	249.5
460	SEG9	2962.5	118.5
461	SEG8	2987.5	249.5
462	SEG7	3012.5	118.5
463	SEG6	3037.5	249.5
464	SEG5	3062.5	118.5
465	SEG4	3087.5	249.5
466	SEG3	3112.5	118.5
467	SEG2	3137.5	249.5
468	SEG1	3162.5	118.5
469	SEG0	3187.5	249.5
470	COMS	3307.5	118.5
471	COM0	3332.5	249.5
472	COM2	3357.5	118.5
473	COM4	3382.5	249.5
474	COM6	3407.5	118.5
475	COM8	3432.5	249.5
476	COM10	3457.5	118.5
477	COM12	3482.5	249.5
478	COM14	3507.5	118.5
479	COM16	3532.5	249.5
480	COM18	3557.5	118.5
481	COM20	3582.5	249.5
482	COM22	3607.5	118.5
483	COM24	3632.5	249.5
484	COM26	3657.5	118.5
485	COM28	3682.5	249.5
486	COM30	3707.5	118.5

PAD	NAME	X	Y
487	COM32	3732.5	249.5
488	COM34	3757.5	118.5
489	COM36	3782.5	249.5
490	COM38	3807.5	118.5
491	COM40	3832.5	249.5
492	COM42	3857.5	118.5
493	COM44	3882.5	249.5
494	COM46	3907.5	118.5
495	COM48	3932.5	249.5
496	COM50	3957.5	118.5
497	COM52	3982.5	249.5
498	COM54	4007.5	118.5
499	COM56	4032.5	249.5
500	COM58	4057.5	118.5
501	COM60	4082.5	249.5
502	COM62	4107.5	118.5
503	COM64	4132.5	249.5
504	COM66	4157.5	118.5
505	COM68	4182.5	249.5
506	COM70	4207.5	118.5
507	COM72	4232.5	249.5
508	COM74	4257.5	118.5
509	COM76	4282.5	249.5
510	COM78	4307.5	118.5
511	COM80	4332.5	249.5
512	COM82	4357.5	118.5
513	COM84	4382.5	249.5
514	COM86	4407.5	118.5
515	COM88	4432.5	249.5
516	COM90	4457.5	118.5
517	COM92	4482.5	249.5
518	COM94	4507.5	118.5
519	COM96	4532.5	249.5
520	COM98	4557.5	118.5
521	COM100	4582.5	249.5
522	COM102	4607.5	118.5
523	COM104	4632.5	249.5
524	COM106	4657.5	118.5
525	COM108	4682.5	249.5
526	COM110	4707.5	118.5
527	COM112	4732.5	249.5
528	COM114	4757.5	118.5
529	COM116	4782.5	249.5
530	COM118	4807.5	118.5
531	COM120	4832.5	249.5
532	COM122	4857.5	118.5
533	COM124	4882.5	249.5
534	COM126	4907.5	118.5
535	COM128	4932.5	249.5
536	COM130	4957.5	118.5
537	COM132	4982.5	249.5
538	COM134	5007.5	118.5
539	COM136	5032.5	249.5
540	COM138	5057.5	118.5
541	COM140	5082.5	249.5
542	COM142	5107.5	118.5
543	COM144	5132.5	249.5
544	COM146	5157.5	118.5
545	COM148	5005	-11
546	COM150	5136	-36
547	COM152	5005	-61
548	COM154	5136	-86
549	COM156	5005	-111
550	COM158	5136	-136
551	COM160	5005	-161
552	COMS	5136	-186

Unit : um

5 BLOCK DIAGRAM

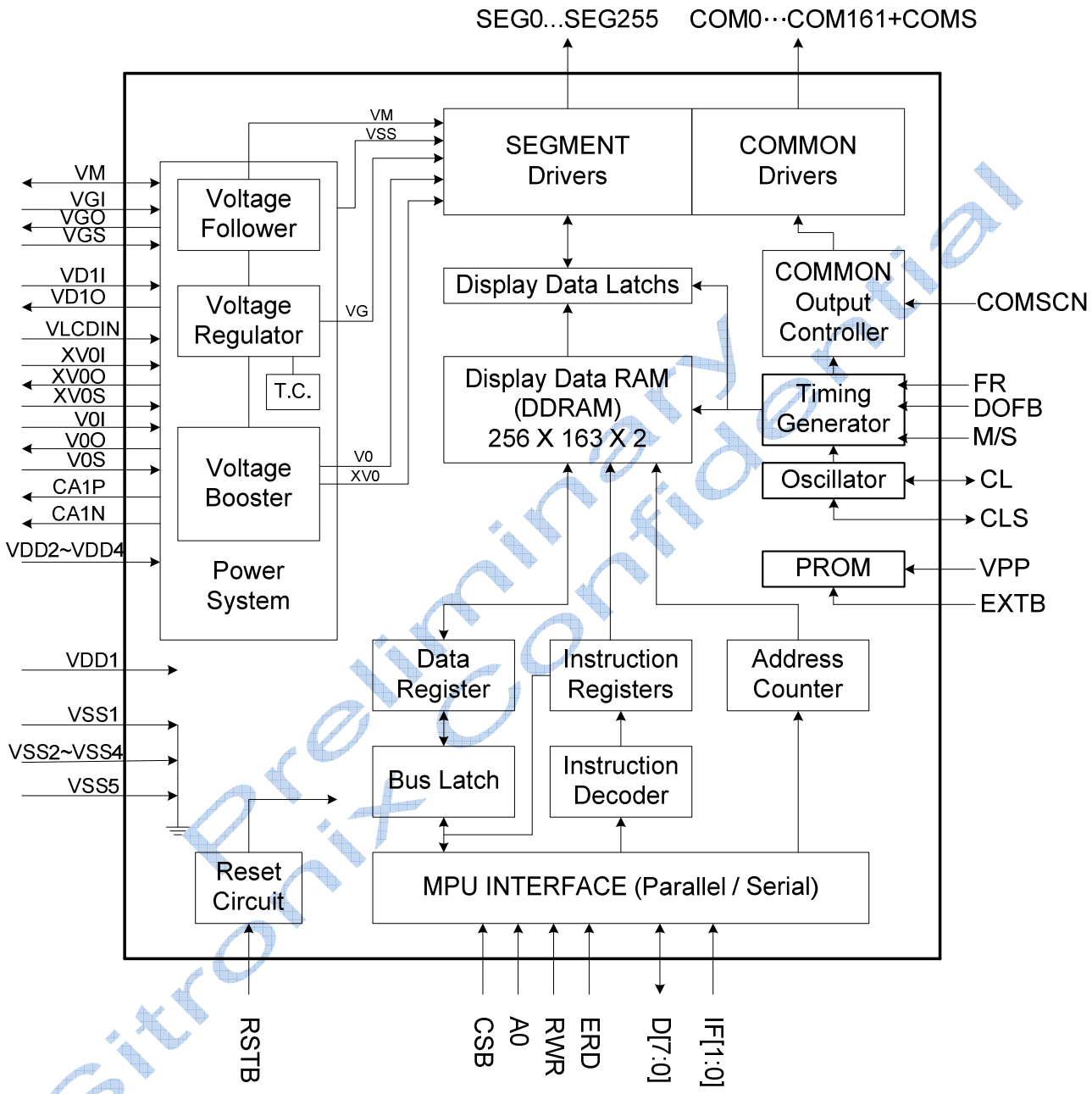


Figure 2 Block Diagram

6 PIN DESCRIPTION

6.1 Power Supply Pins

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>VDD1</td><td>Power</td><td>Digital power. If VDD1=VDD2, connect to VDD2 externally.</td></tr>
<tr><td>VDD2</td><td>Power</td><td>Analog power for internal booster. If VDD1=VDD2, connect to VDD1 externally.</td></tr>
<tr><td>VDD3</td><td>Power</td><td>Analog power for temperature compensation circuit.</td></tr>
<tr><td>VDD4</td><td>Power</td><td>Analog power for follower circuit.</td></tr>
<tr><td>VSS1</td><td>Power</td><td>Digital ground. Ground system should be connected together.</td></tr>
<tr><td>VSS2
VSS3
VSS4</td><td>Power</td><td>Analog ground. Ground system should be connected together.</td></tr>
<tr><td>VSS5</td><td>Power</td><td>Analog ground for external power supply and should be connected with VSS1~VSS4.</td></tr>
<tr><td>VD1S</td><td>Input</td><td>Digital power source selection.
VD1S = “L”: the power source of digital circuit is VDD1.
VD1S = “H”: the power source of digital circuit is internal regulator.
<table>
<tr><th>VDD1 (TYP.)</th><th>Level of VD1S</th></tr>
<tr><td>1.8V</td><td>VSS1</td></tr>
<tr><td>2.8V</td><td>VDD1</td></tr>
<tr><td>3.0V</td><td>VDD1</td></tr>
<tr><td>3.3V</td><td>VDD1</td></tr>
</table></td></tr>
<tr><td>VD1I
VD1O</td><td>Power</td><td>VD1I is the power source of digital circuits.
VD1O is the VD1 output. VD1I and VD1O should be connected together.</td></tr>
<tr><td>CA1P
CA1N</td><td>Output</td><td>DC/DC voltage converter. Connect a capacitor between CA1P and CA1N.</td></tr>
<tr><td>VLCDIN</td><td>Power</td><td>External voltage supply for power system.
If the internal voltage generator is used, VLCDIN has to be left open.</td></tr>
<tr><td>V0O
V0I
V0S</td><td>Power</td><td>Positive operating voltage of COM-drivers.
V0O is the output of the positive Vop generator.
V0I is the positive Vop supply of LCD drivers.
V0S is the sensor of the positive Vop generator.
V0O, V0I & V0S should be connected together by ITO.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>XV0O
XV0I
XV0S</td><td>Power</td><td>Negative operating voltage of COM-drivers.
XV0O is the output of the negative Vop generator.
XV0I is the negative Vop supply of LCD drivers.
XV0S is the sensor of the negative Vop generator.
XV0O, XV0I & XV0S should be connected together by ITO.</td></tr>
<tr><td>VGO
VGI
VGS
VM</td><td>Power</td><td>VG is the power of SEG-drivers. VM is the non-select voltage level of COM-drivers.
VGO is the output of the VG regulator.
VGI is the supply of SEG-drivers.
VGS is the sensor of the VG regulator.
VGO, VGI & VGS should be connected together by ITO.
VM is the I/O pin of LCD bias supply voltage.
Be sure the relationships (as shown below) among the LCD driving voltages:
V0 ≥ VG ≥ VM ≥ VSS ≥ XV0;
VDD2-0.7 ≥ VM ≥ 0.9V;
VDD2-0.7 ≥ VG ≥ 1.8V
When this IC is operating, VG and VM are generated according to the bias setting shown below:
<table>
<tr><th>LCD Bias</th><th>VG</th><th>VM</th></tr>
<tr><td>1/N Bias</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
Note: N = 9~14</td></tr>
</table>

6.2 Driver Output Pins

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG255</td><td>O</td><td>LCD SEG-driver outputs.
The display data and the polar-signal (M) control the output voltage of SEG-driver.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">M</th><th colspan="2">Segment Driver Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>H</td><td>H</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>H</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>L</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Display OFF, Sleep-In mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM161</td><td>O</td><td>LCD COM-driver outputs.
The internal scanning data and the polar-signal (M) control the output voltage of COM-driver.
<table>
<tr><th>Scan data</th><th>M</th><th>Common Driver Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>XV0</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>VM</td></tr>
<tr><td>L</td><td>L</td><td>VM</td></tr>
<tr><td colspan="2">Display OFF, Sleep-In mode</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>LCD common driver outputs for icons. There are four pins to choose if using icon. When icon is not used, left these pins open.</td></tr>
<tr><td>COMSCN</td><td>I</td><td>Set scan direction of COM.
COMSCN=”L” ; COM0→COMX
COMSCN=”H” ; COMX→COM0
Note: COMX is determined by the DUTY setting.</td></tr>
</table>

6.3 Clock System Input

Name	Type	Description
CLS	I	Clock source selection pin. CLS="H": enable internal clock. CLS="L": disable internal clock and use external clock.
CL	I/O	For external clock. If CLS="H": this pin is the output of oscillator. If CLS="L": this pin is the input of oscillator.

6.4 Interface Logic Pins

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin. When RSTB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>IF[1:0]</td><td>I</td><td>These pins select interface operation mode.
<table>
<tr><th>IF1</th><th>IF0</th><th>MPU interface type</th></tr>
<tr><td>L</td><td>L</td><td>4-line serial interface</td></tr>
<tr><td>L</td><td>H</td><td>I2C serial interface</td></tr>
<tr><td>H</td><td>L</td><td>8-bit 6800 parallel interface</td></tr>
<tr><td>H</td><td>H</td><td>8-bit 8080 parallel interface</td></tr>
</table>
Note: Refer to ““Parallel / Serial Interface” for detailed information.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pin.
CSB=“L”: This chip is selected and the MPU interface is active.
CSB=“H”: This chip is not selected and the MPU interface is disabled (D[7:0] are high impedance).
<u>There is no CSB pin in I2C interface and it should be fixed to “L” by VSS1.</u></td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the access is related to data or command.
A0 = "H": Indicates that D[7:0] are display data;
A0 = "L": Indicates that D[7:0] are control data.
There is no A0 pin in I2C interface and it should be fixed to “H” by VDD1.</td></tr>
<tr><td>RWR</td><td>I</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table>
<tr><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>R/W</td><td>Read / Write control input pin
R/W = “H” : read
R/W = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable input pin.
The data are latched at the rising edge of the /WR signal.</td></tr>
</table>
This pin is not used in serial interfaces and should be connected to VDD1.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>ERD</td><td>I</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table>
<tr><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin.
R/W = “H”: When E is “H”, data bus is in output status.
R/W = “L”: The data are latched at the falling edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, data bus is in output status.</td></tr>
</table>
This pin is not used in serial interfaces and should be connected to VDD1.</td></tr>
<tr><td rowspan="3">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: 8080 or 6800 mode
8 bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When CSB is “H” , D[7:0] are high impedance.</td></tr>
<tr><td>I/O</td><td>When using serial interface : 4-line SPI mode
D[7:4] : fix to “H” by VDD1.
D[3:1] : serial input/output data (SDA).
D[0] : serial input clock (SCL).
<u>D1 to D3 must be connected together (SDA)</u>
When CSB is “H” , D[7:0] are high impedance.</td></tr>
<tr><td>I/O</td><td>When using serial interface : I2C interface
D[7] : SA[1], I2C slave address bit. Must be connected to VDD1 or VSS1.
D[6] : SA[0], I2C slave address bit. Must be connected to VDD1 or VSS1.
D[5:4] : fix to “H” by VDD1.
D[3:2] : SDA_OUT, serial data and acknowledge output for the I2C interface.
D[1] : SDA_IN, serial input data
D[0] : SCL, serial input clock .
<u>D1 to D3 must be connected together (SDA)</u>
<u>CSB must be fixed to “L” by VSS1.</u></td></tr>
</table>

Note:

1. After VDD1 is turned ON, all MPU interface pins should not be left OPEN.
2. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I^2C interface compatible. Separating acknowledge-output from serial data input is advantageous for chip-on-glass (COG) applications. In COG applications, the ITO resistance and the pull-up resistor will form a voltage divider, which affects acknowledge-signal level. Larger ITO resistance will raise the acknowledged-signal level and system cannot recognize this level as a valid logic "0" level. By separating SDA_IN from SDA_OUT, the IC can be used in a mode that ignores the acknowledge-bit. For applications which check acknowledge-bit, it is necessary to minimize the ITO resistance of the SDA_OUT trace to guarantee a valid low level

6.5 Master/Slave Pins

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>FR</td><td>I/O</td><td>This is the liquid crystal alternating current signal terminal.</td></tr>
<tr><td>DOFB</td><td>I/O</td><td>This is the LCD synchronous control terminal.</td></tr>
<tr><td>M/S</td><td>I</td><td>This terminal selects the master/slave operation for the ST75256.
Master operation outputs the timing signals that are required for the LCD display, while slave operation input the timing signals required for the liquid crystal display.
That synchronized the liquid crystal display system between Master and Slave.
M/S = "H" Master operation
M/S = "L" Slave operation
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>DOFB</th></tr>
<tr><td rowspan="2">"H"</td><td>"H"</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>"L"</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">"L"</td><td>"H"</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr>
<tr><td>"L"</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table>
</td></tr>
</table>

6.6 OTP Pins

Name	Type	Description
VPP	Power	The programming power supply of the built-in OTP. Apply external power (6.5~6.75V) here when programming (> 8mA for successful programming).
EXTB	Input	EXTB="L": Enable the extension operation mode. When programming OTP, connect EXTB to VSS1 externally. This pin has an internal pull-high resistor. Please leave this pin OPEN after special operation.

6.7 Test Pins

Name	Type	Description
T0-T2	Test	Reserved for test only. T0 must be connected to VSS1. T1-T2 must be floating.
TEST0	Test	Reserved for testing only. Recommend setting to VSS1.
Reserved	Test	Reserved for test only, recommend setting to floating.

6.8 ITO Resistance Limitation

Pin Name	ITO Resister
VDD1~VDD4, VSS1~VSS5, V0I, V0O, V0S, XV0I, XV0O, XV0S, VM,CA1P,CA1N , V_{LCDIN}	<100Ω
VPP, VGI, VGO, VGS	<50Ω
A0, ERD, RWR, CSB, D[7:0], (SDA), (SCL)	<700Ω
RSTB	1~3KΩ
IF[1:0], FR,DOFB,M/S,COMSCN,CLS,EXTB,T0,TEST0,VD1S	<1KΩ
CL, T[2:1], Reserved	Floating

Note:

1. Make sure that the ITO resistance of COM0 ~ COM161 is equal, and so is it of SEG0 ~ SEG255.
2. These Limitations include the bottleneck of ITO layout.
3. Refer to the application note for ITO layout guideline.

6.9 ITO Layout Guide

For V0, XV0, VG, VDD and VSS- The ITO layout suggestion is shown as below:

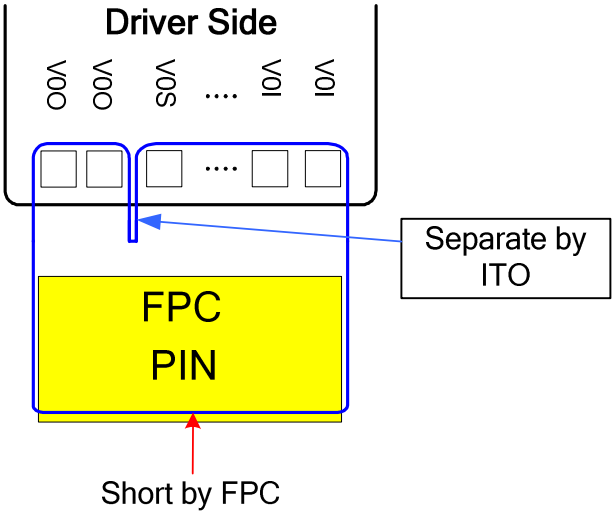


Figure 3 V0 ITO Layout

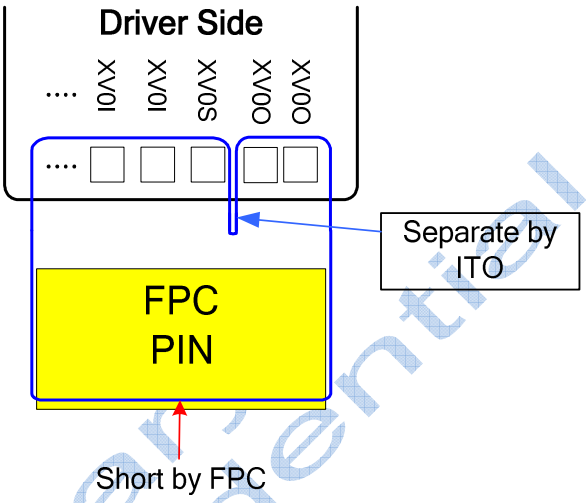


Figure 4 XV0 ITO Layout

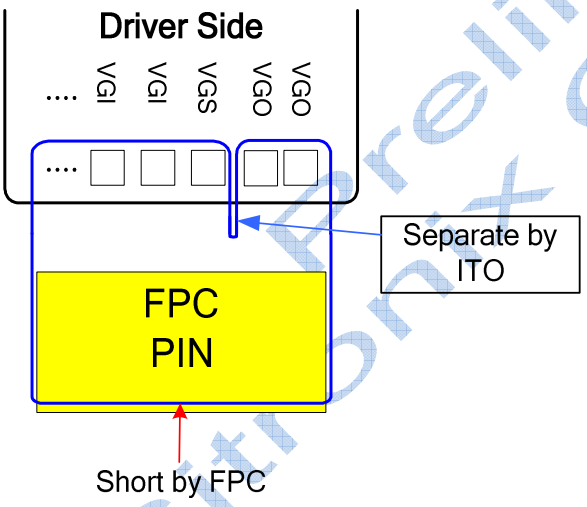


Figure 5 VG ITO Layout

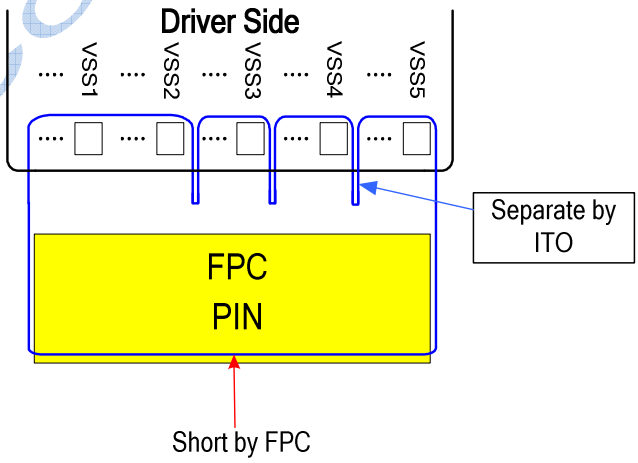


Figure 6 VSS ITO Layou

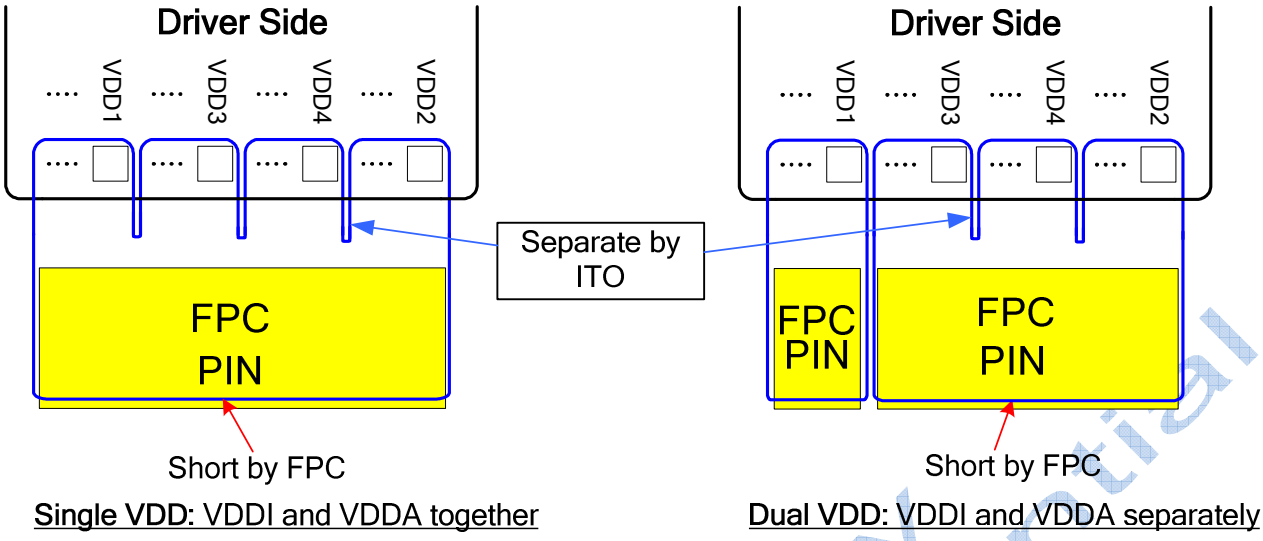


Figure 7 VDD ITO Layout

6.10 For VPP

This is the power source for programming the internal OTP. If the ITO resistance is too high, the operation current will cause the voltage drop while programming OTP. Please try to keep the ITO resistance as low as possible.

6.11 Enhance ESD performance for COG application

1. Increase RSTB resistance:

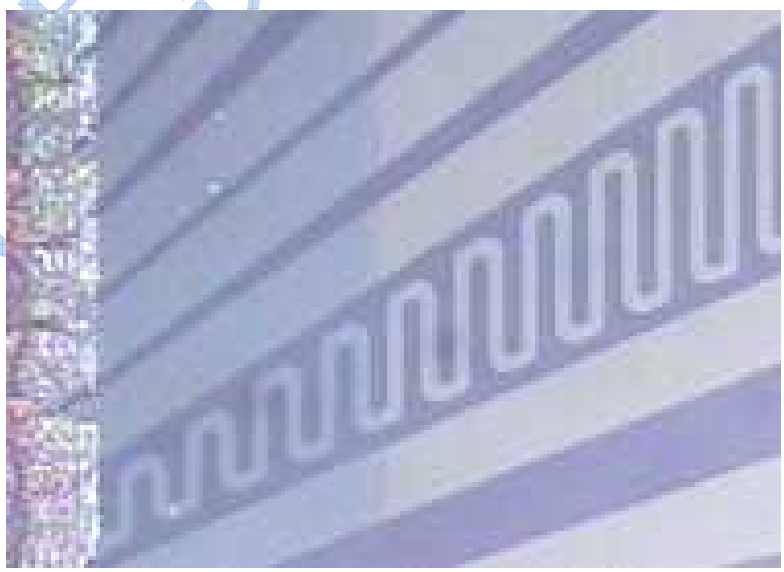


Figure 8 RSTB ITO Layout

2. Add ESD protection ring:

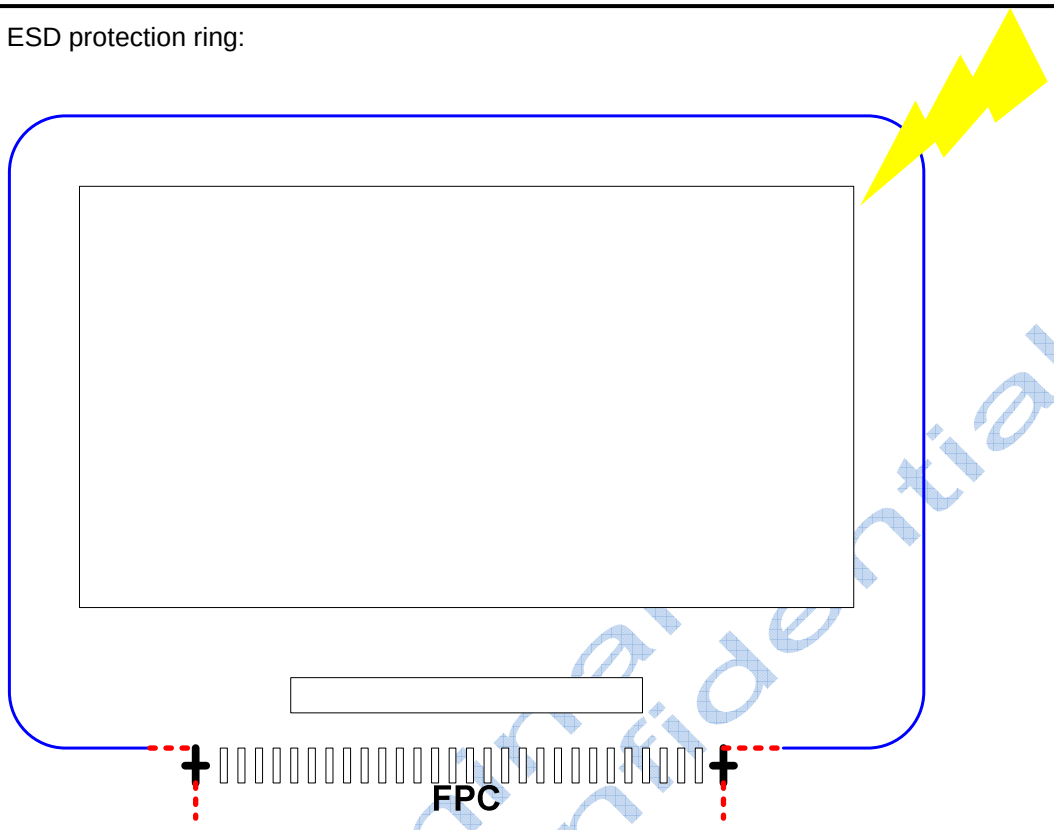


Figure 9 Air ESD Protection Ring

Note: DO NOT short the ground of ESD protection ring to VSS of driver IC.

7 FUNCTION DESCRIPTION

7.1 Microprocessor Interface

7.1.1 Chip Select Input

CSB pin is used for chip selection. ST75256 can interface with an MPU when CSB is "L". If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 4-Line serial and I^2C interface, the internal shift register and serial counter are reset when CSB is “H”.

7.1.2 Parallel / Serial Interface

ST75256 has four types of interface for kinds of MPU. The MPU interface is selected by IF[1:0] pins as shown in **Table 1**.

Table 1 Parallel/Serial Interface Mode

Type	IF1	IF0	Interface mode
Serial	L	L	4-line serial interface
	L	H	I^2C serial interface
Parallel	H	L	8bit 6800-series MPU mode
	H	H	8bit 8080-series MPU mode

7.1.3 Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by IF[1:0] as shown in **Table 2**. The data transfer type is determined by signals of A0, ERD and RWR as shown in **Table 3**.

Table 2 Microprocessor Selection for Parallel Interface

IF1	IF0	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
H	L	CSB	A0	E	R/W	D[7:0]	6800-series
H	H			/RD	/WR		8080-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Internal status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: In 6800-series interface mode, fixing E (ERD) pin at high can use CSB as enable signal instead. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0 and R/W (RWR) pins as defined in 6800-series mode.

7.1.4 Setting Serial Interface

Interface	CSB	A0	ERD	RWR	D[7:0]
4-Line SPI	CSB	A0	---	---	D[0]= SCL,, D[1:3]=SDA, D[4:7]= ---
I^2C interface	L	---	---	---	D[0]=SCL, D1=SDA_IN, D[3:2]=SDA_OUT, D[5:4]= ---, D[7:6]=SA[1:0]. Refer to I^2C interface.

* The un-used pins are marked as "---" and should be fixed to "H" by VDD1.

Note:

1. The option setting to be "H" should connect to VDD1.
2. The option setting to be "L" should connect to VSS1.

7.1.5 4-Line Serial Interface

ST75256 is active when CSB is "L", and serial data (SDA) and serial clock (SCL) inputs are enabled. When CSB is "H", ST75256 is not active, and the internal 8-bit shift register and 3-bit counter are reset. Some specified information (status byte) can be read out in this mode. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCL). After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

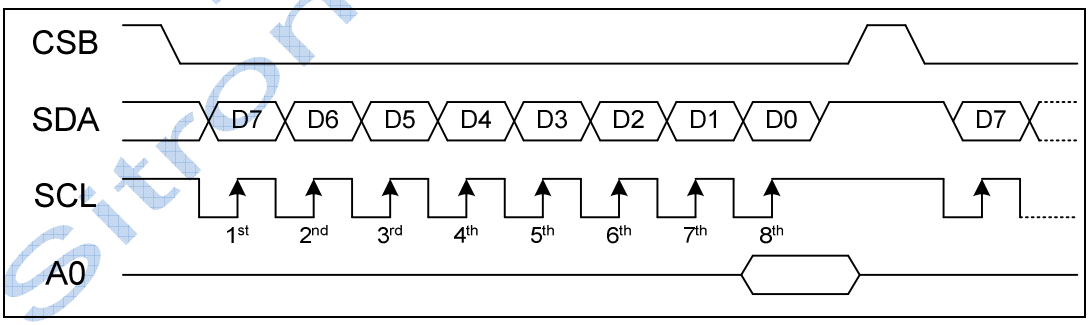


Figure 10 4-Line SPI Access

7.1.6 I²C Interface

The I²C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in **Figure 11**.

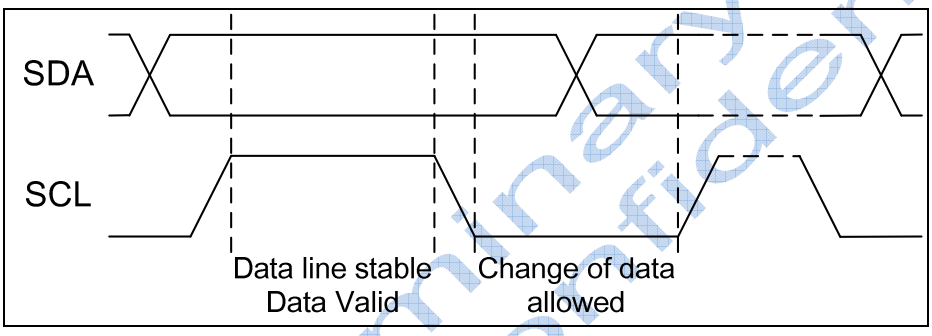


Figure 11 Bit Transfer

START AND STOP CONDITIONS

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in **Figure 12**.

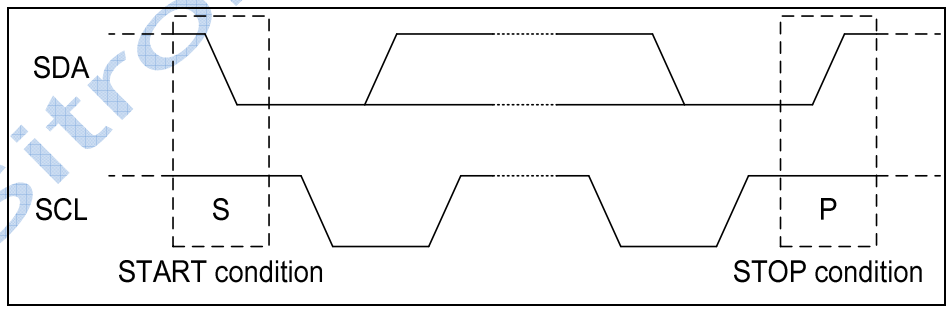


Figure 12 Definition of START and STOP Condition

SYSTEM CONFIGURATION

The system configuration is illustrated in **Figure 13** and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

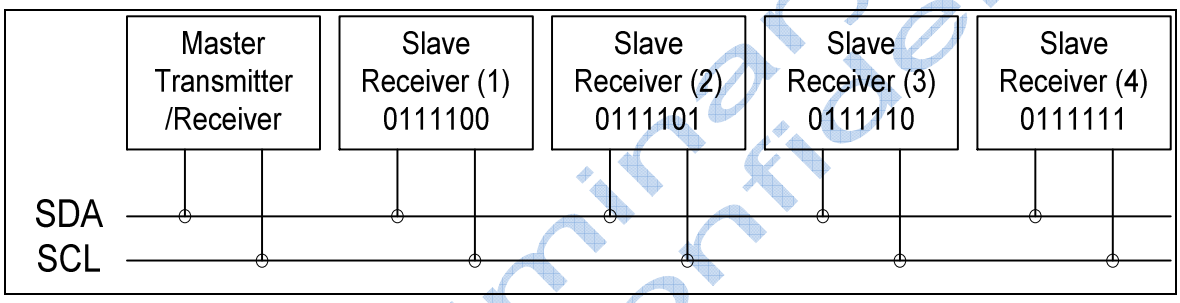


Figure 13 System Configuration

ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I^2C Interface is illustrated in **Figure 14**.

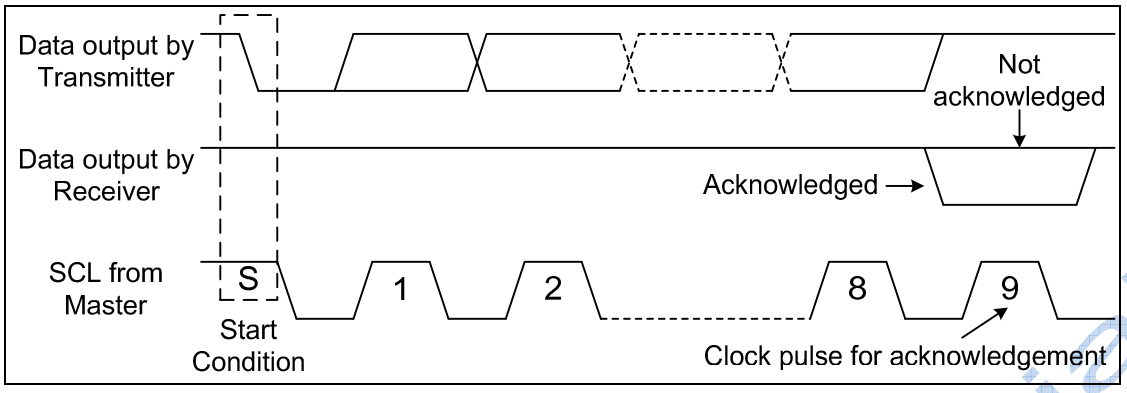


Figure 14 Acknowledgement of I²C Interface

I²C INTERFACE PROTOCOL

ST75256 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for ST75256. The least significant 2 bits of the slave address is set by connecting SA0 and SA1 to either logic 0 (VSS1) or logic 1 (VDD1).The I²C Interface protocol is illustrated in **Figure 15**.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address and A0. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST75256 device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST75256 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

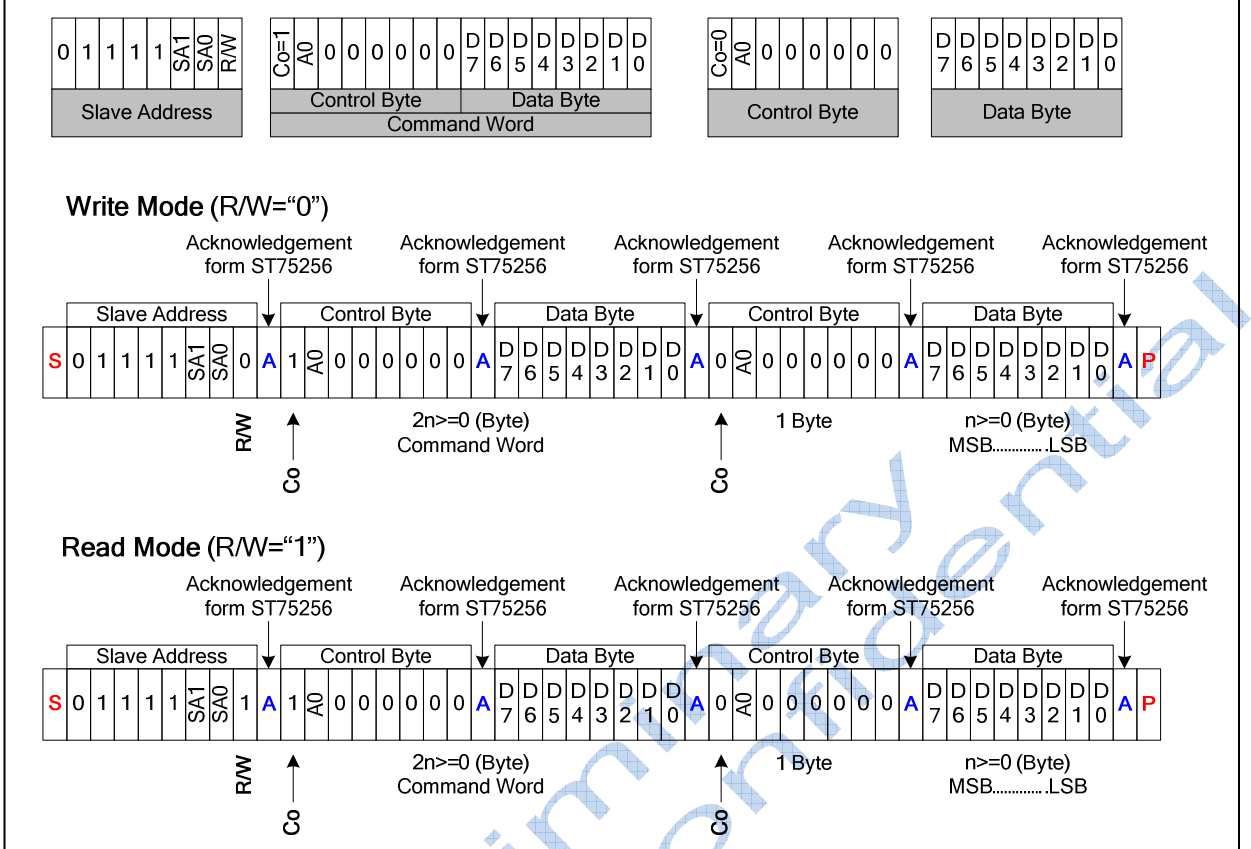


Figure 15 I²C Interface Protocol

Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

7.2 Data Transfer

ST75256 uses bus holder and internal data bus for data transfer with MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in **Figure 16**. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in **Figure 17**. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

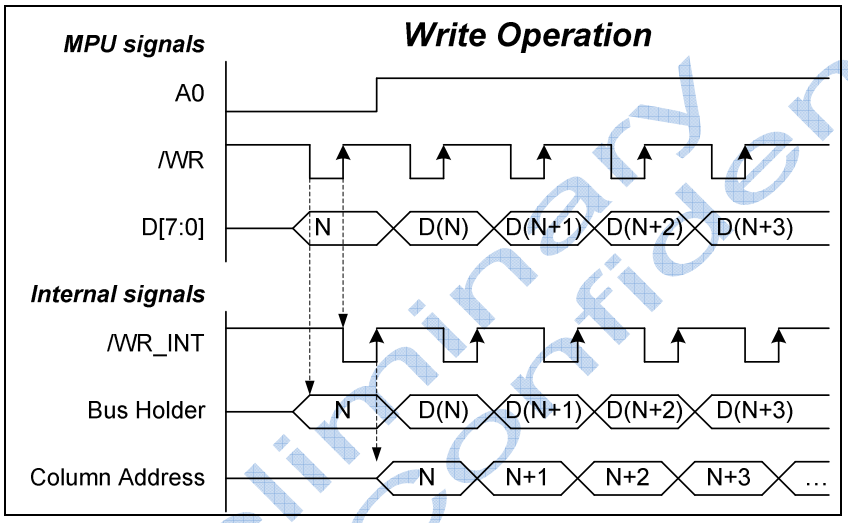


Figure 16 Data Transfer: Write

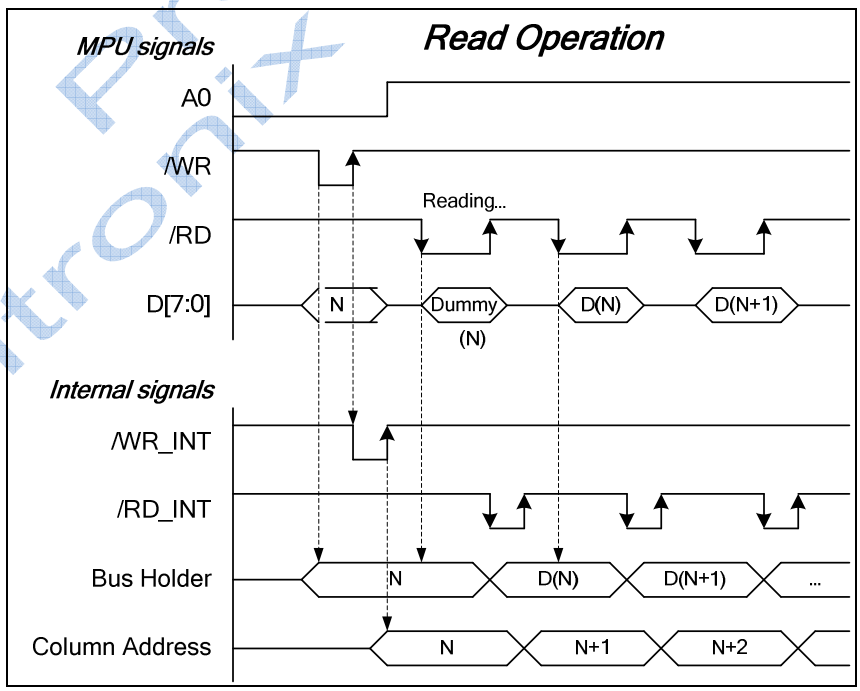
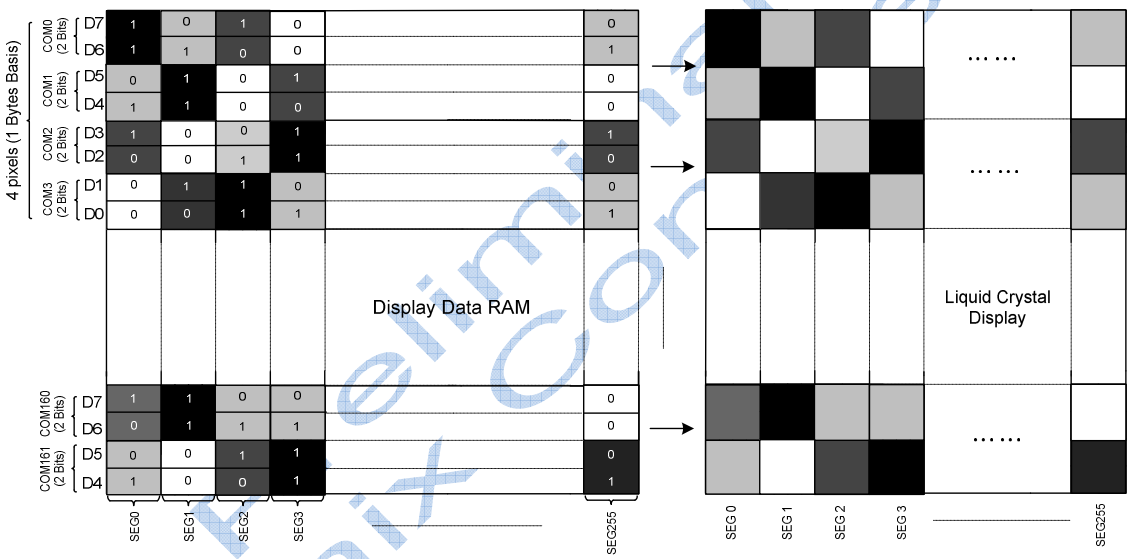


Figure 17 Data Transfer: Read

7.3 Display Data RAM (DDRAM)

ST75256 containing a 256x163x2 bit static RAM stores the display data. The display data RAM (DDRAM) stores the pixel data of the LCD. The built-in DDRAM is an addressable memory array with 256 columns by 163 rows. ST75256 provides 2 kinds of display modes (4-Gray/Monochrome scale mode) and a fast-addressing mode for fast updating display data. Each page address represents different sub-COMs in different display mode. For example, in 4-Gray/Monochrome scale mode setting the page address to “00h” means that upcoming 8 bits data is addressing to COM0~COM3/COM0~COM7 (refer to **Figure 18**, **Figure 19**). The column address is directly related to the SEG output number. The LCD controller reads the pixel data in DDRAM, and then it outputs to COM/SEG pad. While the LCD controller operates independently, display data can be written into DDRAM at the same time and data is also being displayed on LCD panel without causing the abnormal display.



2 Bits Data N=0~3		DDRAM		LCD
D2N+1	D2N			
1	1	1	1	
0	0	0	0	
1	0	1	0	
0	1	0	1	

Figure 18 DDRAM Mapping (4-Level Gray Scale Mode)

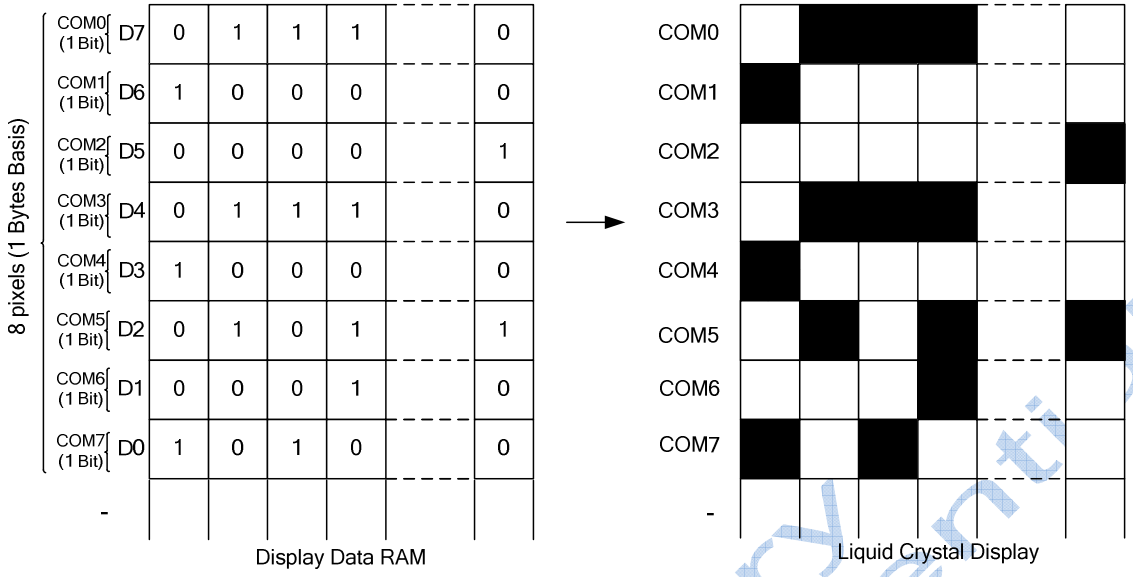


Figure 19 DDRAM Mapping (Monochrome Mode)

7.3.1 Page Address Circuit

Use the set page address command and set column address command to specify DDRAM address to be accessed as shown in **Figure 24**. This circuit controls the address in the page direction when MPU accesses the DDRAM or read the DDRAM to display image on the LCD. When the page-direction scan is specified with Data scan direction command and the address are increased from the start up to the end page, the column address is increased by 1 and the page address returns to the start page.

In the READ operation, as the end page is reached, the column address is automatically increased by 1 and the page address returns to the start page.

User may inverse the correspondence between the DDRAM address and common output via the address normal/inverse parameter of Data scan direction command.

7.3.2 Column Address Circuit

This circuit is to control the address in the column direction when MPU accesses the DDRAM. When the column-direction scan is specified with Data scan direction command and the address are increased from the start up to the end column, the page address is increased by 1 and the column address returns to the start column.

In the READ operation, the column address is also automatically increased by 1 and returns to the start page as the end column is reached.

Just like the page address control circuit, users may inverse the correspondence between the DDRAM column address and segment output via the column address normal/inverse parameter of Data scan direction command. This arrangement makes the chip layout on the LCD module flexible.

7.3.3 I/O Buffer Circuit

It is the bi-directional buffer when MPU reads or writes the DDRAM. Since the READ or WRITE operation of MPU to DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM while the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.4 Display Data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.3.5 Data Orientation

By setting control flag “DO” (Refer to Data Format Select Command), the input Data written into DDRAM can have the LSB on top (DO=0, **Figure 20** & **Figure22**) or at bottom (DO=1, **Figure 21** & **Figure23**)

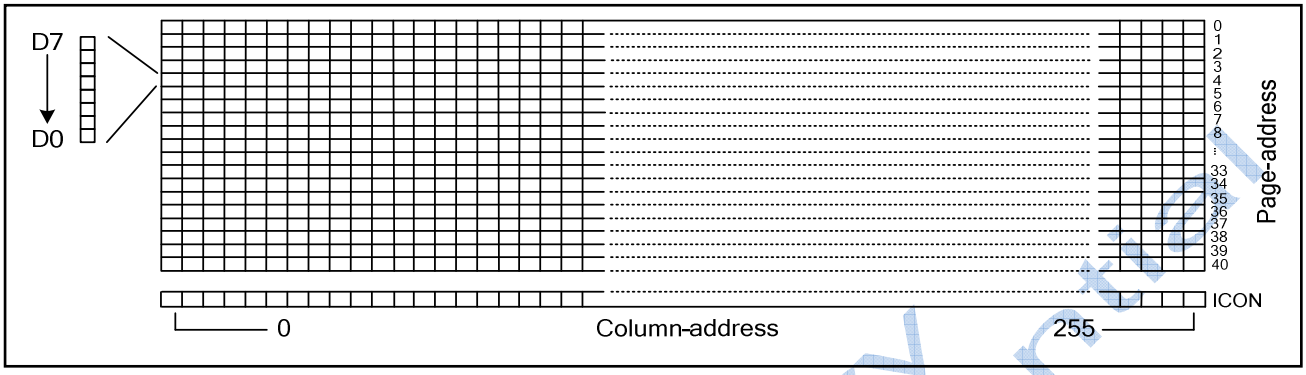


Figure 20 RAM format and addressing, if DO=0 (4-Level Gray Scale Mode)

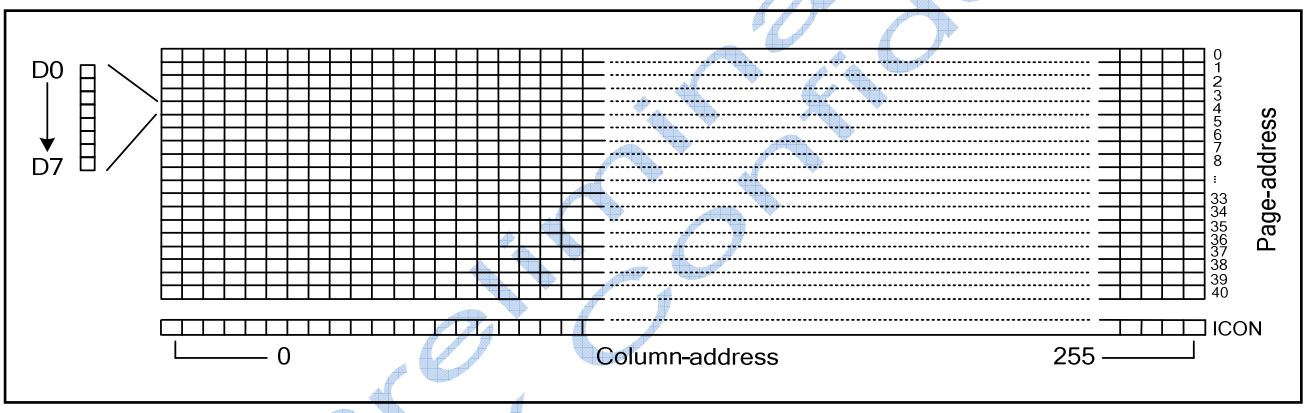


Figure 21 RAM format and addressing, if DO=1 (4-Level Gray Scale Mode)

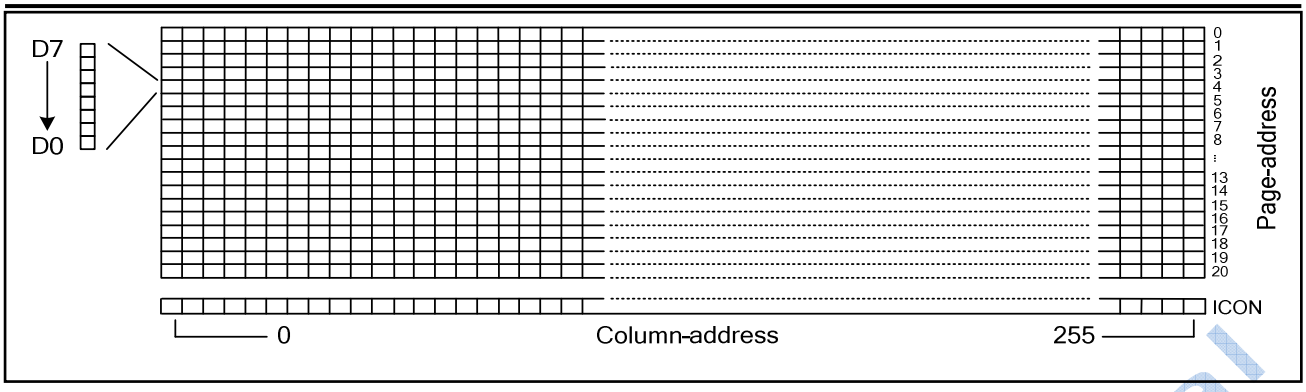


Figure 22 RAM format and addressing, if DO=0 (Monochrome Mode)

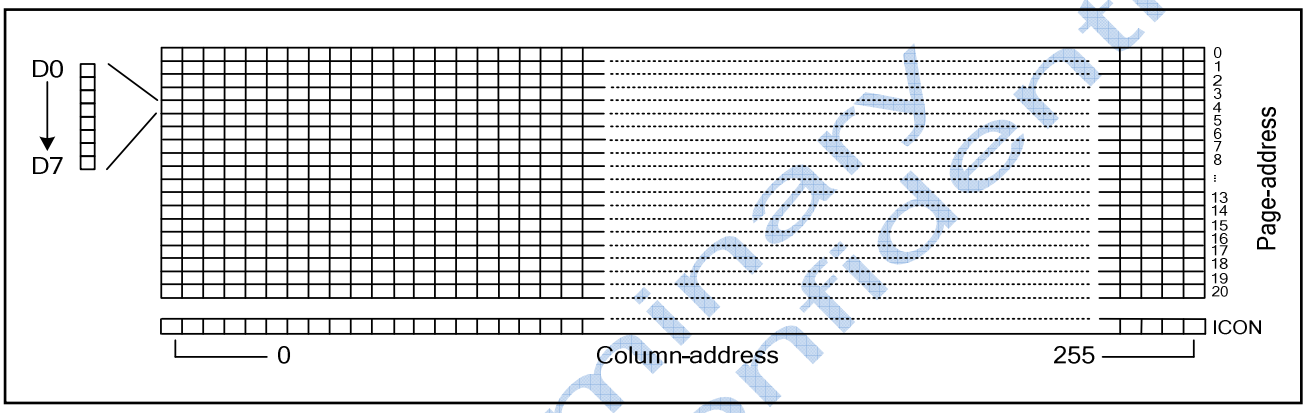


Figure 23 RAM format and addressing, if DO=1 (Monochrome Mode)

7.3.6 DDRAM Map to LCD Driver Output

The internal relation between DDRAM and LCD driver circuit (SEG/COM output path) with different MX or MY setting is illustrated below.

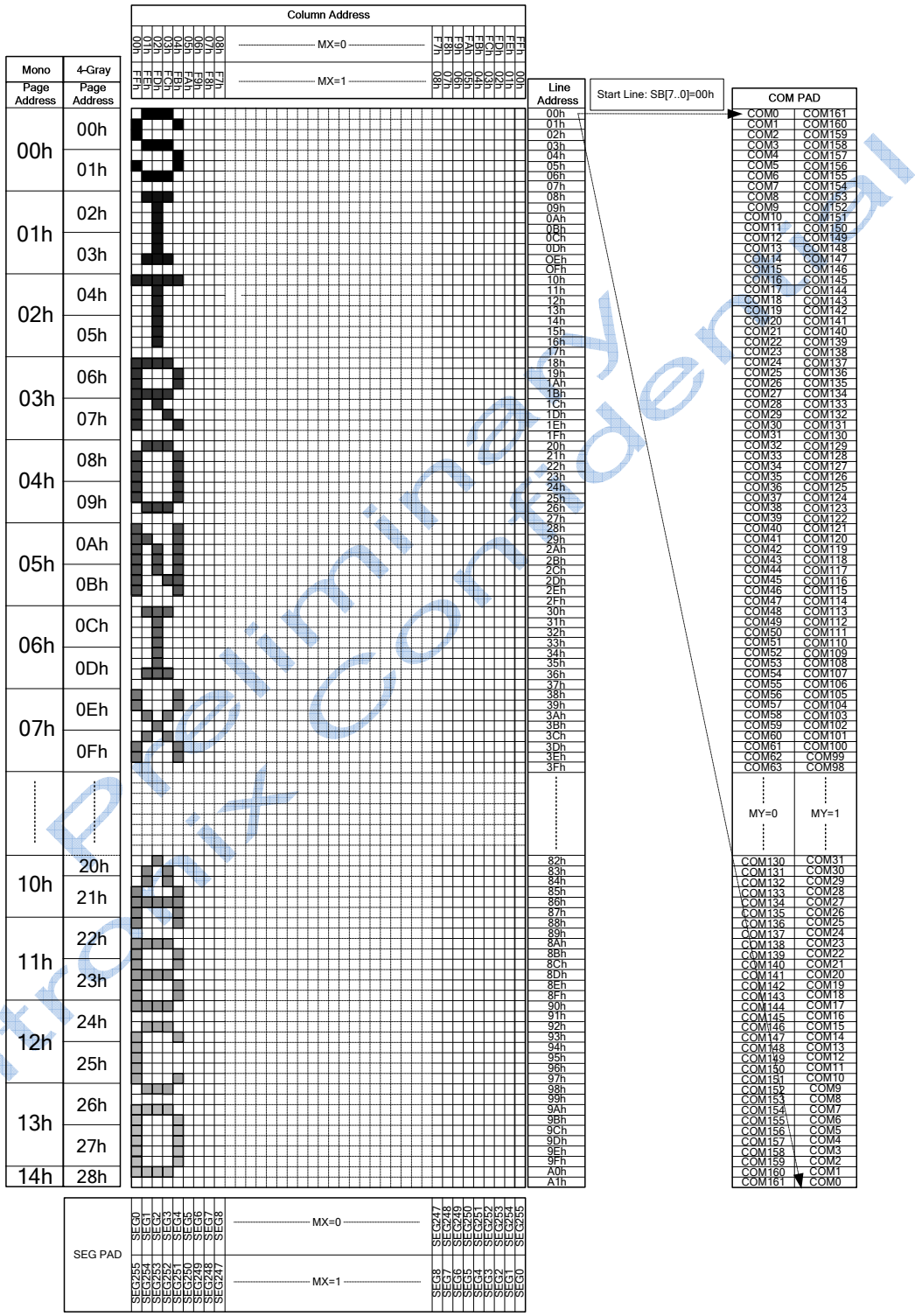


Figure 24 DDRAM Display Direction

7.3.7 Partial Display

This function is defining the visible display area as illustrated in Figure 25. The different partial display area setting will be changing frame rate or Vop to avoid abnormal display. This mode consumes less current than the whole screen display and is suitable for the equipment in the standby state. If the partial display region is out of the maximum display range, it will be no operation.

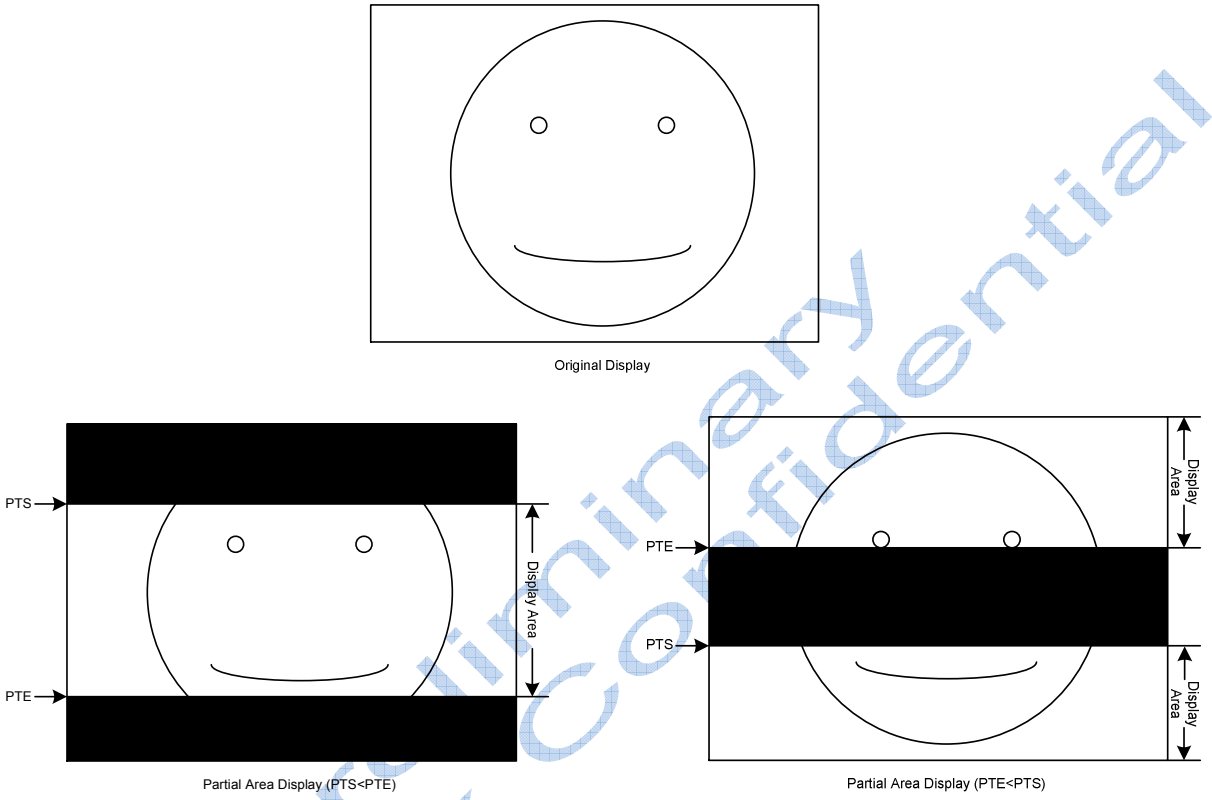


Figure 25 Partial Display Definition

7.3.8 Area Scroll Display

The user may scroll the display screen partially in any one of the following four scroll pattern via partial mode

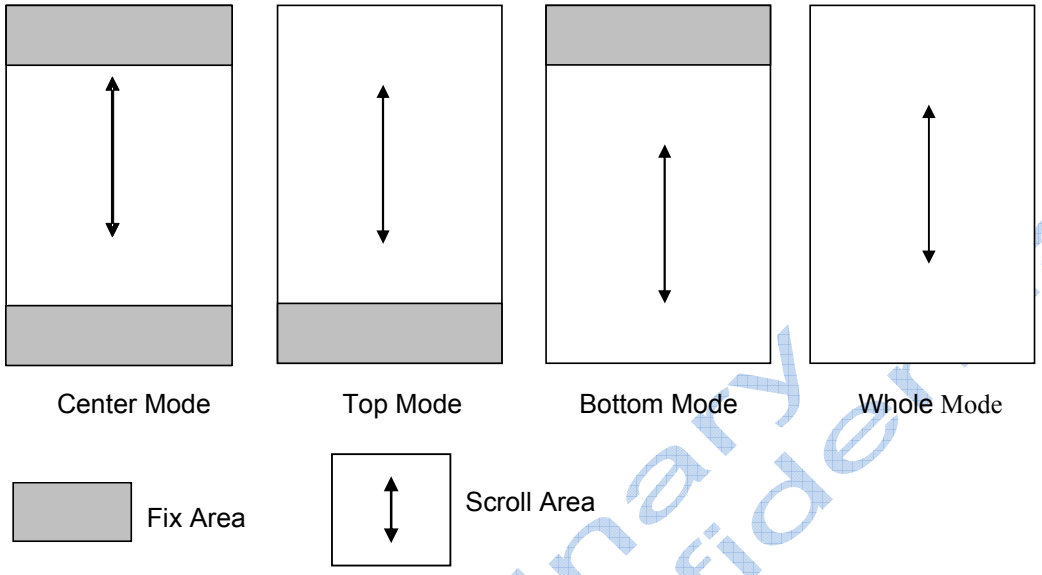


Figure 26 Scroll Definition

7.4 Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. It consumes low power with the fewest external component. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. Before power ST75256 is OFF, a Power OFF procedure is needed. Please refer to the OPERATION FLOW selection.

7.4.1 External Component of Power Circuit

The recommended external power components need only four capacitors. The detailed values of these four capacitors are determined by panel size and loading.

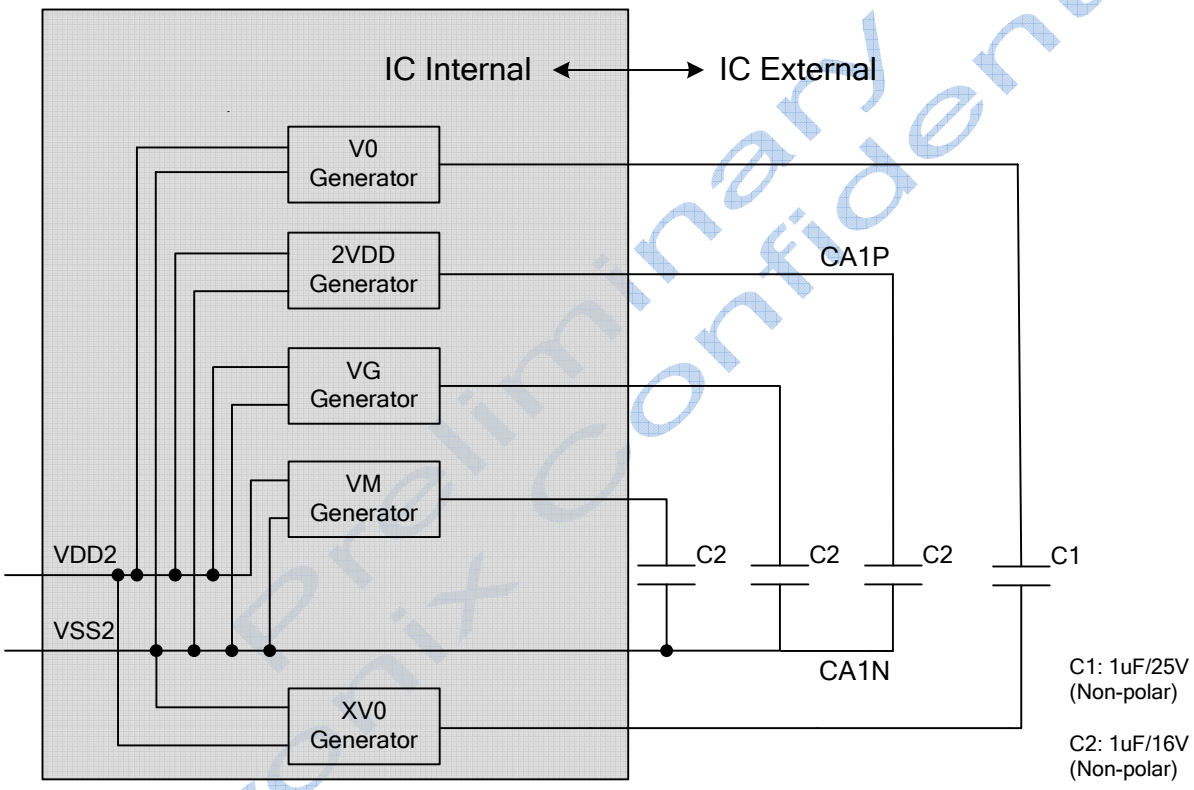


Figure 27 Power Circuit

7.4.2 Voltage Regulator Circuits

The set V_{OP} function is to program the optimum LCD supply voltage V_0.

- **SET VOP (Temperature = 24℃)**

The V_0 value is programmed via the VPR[8:0] register.

V_0 = a + (VPR[8:0]) x b

Ex: VPR[5:0]=000001, VPR[8:6]=100

→ VPR[8:0]=100000001

→ 3.6+257x0.04=13.88

where **a** is a fixed constant value 3.6, **b** is a fixed constant value 0.04, VPR[8:0] is the programmed **V_0** value with programming range from 5 to 310 (136_{HEX}), and VPR[5:0] is the set contrast value which can be set via the interface and is in two's complement format.(See command Vop Control)

The VPR[8:0] value must be in the V_0 programming range as given in **Figure 28** Evaluating equation (1).

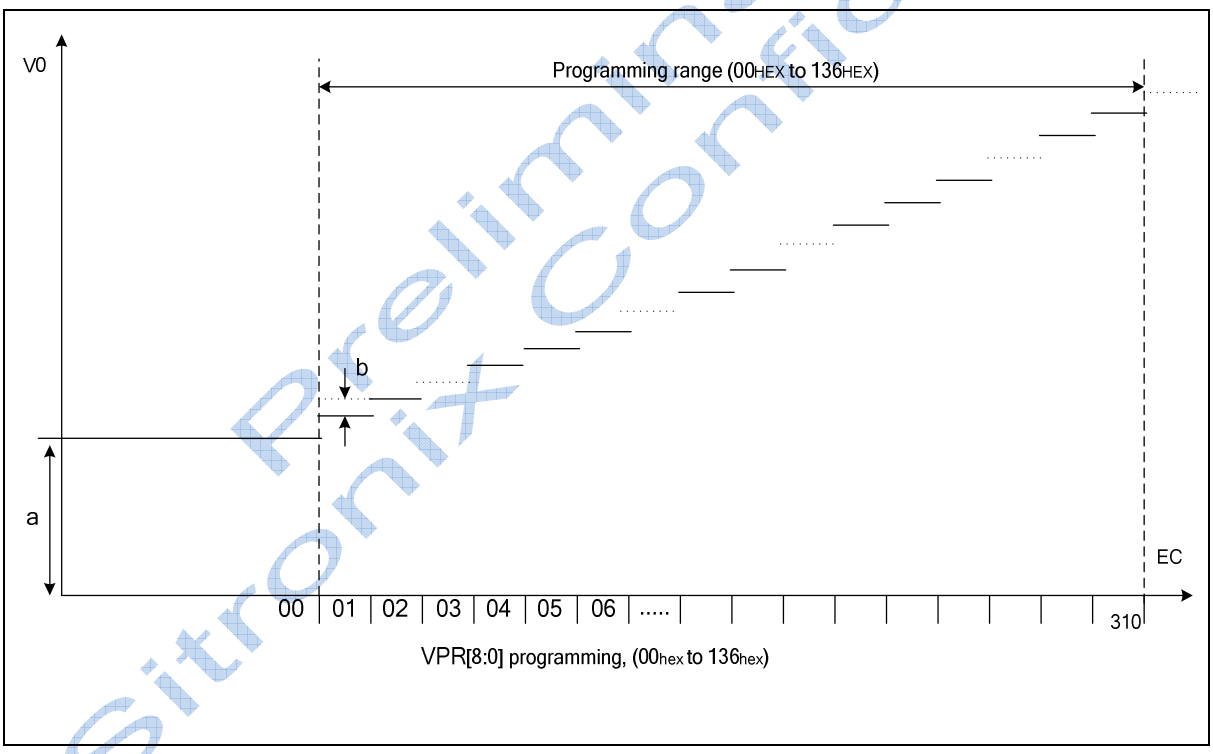


Figure 28 V0 programming range

Although the programming range for the internally generated V_0 allows values above the maximum allowed V_0, the customer has to ensure setting the V_{PR} register and selecting the temperature compensation under all condition and including all tolerances that the maximum allowed V_0 (16V) will never be exceeded.

- **V0 Restriction**

Because VG should larger than 1.8V, V0 value should be higher than 1.8 x Bias / 2 (V) and lower than 16V. V0 value outside the available range is undefined. User has to ensure while selecting the temperature compensation that under all conditions and including all tolerances that V0 voltage remains in the range.

7.5 Temperature Gradient Selection Circuit

7.5.1 SET V0 with temperature compensation (Temperature ≠ 24℃)

There are 16-line slopes in each temperature step, and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8℃. Please see **Figure 29** as below.

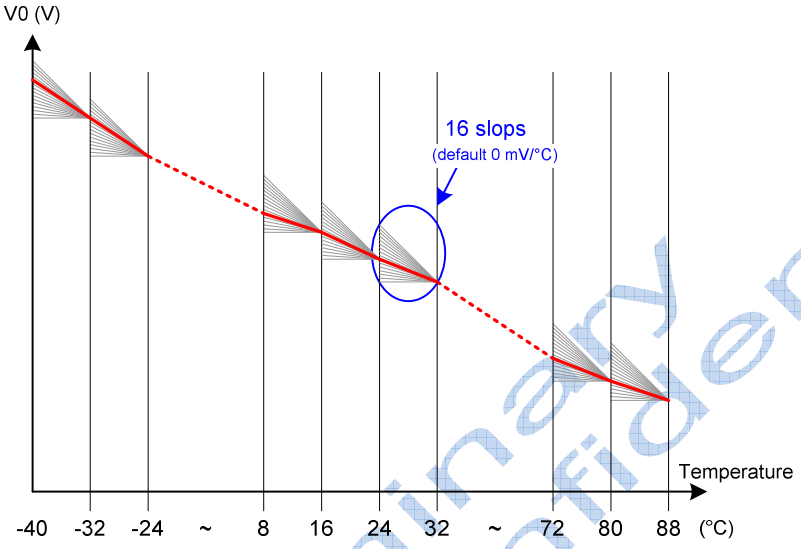


Figure 29 Temperature Compensation Coefficient Selection

In instruction Temperature Gradient Compensation each parameter MTx, where x=0, 1, 2,…, E, F has a setting value between 0 and 15. MTx=0 results in Mx=0V increment on V0, MTx=1 results in Mx=5mV increment,…, MTx=15 results in Mx=15x5mV=75mV increment. Note that each MTx individually corresponds to a temperature interval; the Mx means temperature gradient slope coefficient. The relations between Mx and V0 quantity due to temperature V0(T) are described in the equation shown in **Table 4**.

Temperature Range	Equation V0(T) at temperature=T℃
-40℃ ≦ T < -32℃	V0(T) = V0(T24) + (-32 - T) x M0 + (M1 + M2 + M3 + M4 + M5 + M6 + M7) x 8
-32℃ ≦ T < -24℃	V0(T) = V0(T24) + (-24 - T) x M1 + (M2 + M3 + M4 + M5 + M6 + M7) x 8
-24℃ ≦ T < -16℃	V0(T) = V0(T24) + (-16 - T) x M2 + (M3 + M4 + M5 + M6 + M7) x 8
-16℃ ≦ T < -8℃	V0(T) = V0(T24) + (-8 - T) x M3 + (M4 + M5 + M 6 + M7) x 8
-8℃ ≦ T < 0℃	V0(T) = V0(T24) + (0 - T) x M4 + (M5 + M6 + M7) x 8
0℃ ≦ T < 8℃	V0(T) = V0(T24) + (8 - T) x M5 + (M6 + M7) x 8
8℃ ≦ T < 16℃	V0(T) = V0(T24) + (16 - T) x M6 + M7 x 8
16℃ ≦ T < 24℃	V0(T) = V0(T24) + (24 - T) x M7
24℃ ≦ T < 32℃	V0(T) = V0(T24) - (T - 24) x M8
32℃ ≦ T < 40℃	V0(T) = V0(T24) - (T - 32) x M9 – M8 x 8
40℃ ≦ T < 48℃	V0(T) = V0(T24) - (T - 40) x M10 – (M9 + M8) x 8
48℃ ≦ T < 56℃	V0(T) = V0(T24) - (T - 48) x M11 – (M10 + M9 + M8) x 8
56℃ ≦ T < 64℃	V0(T) = V0(T24) - (T - 56) x M12 – (M11 + M10 + M9 + M8) x 8
64℃ ≦ T < 72℃	V0(T) = V0(T24) - (T - 64) x M13 – (M12 + M11 + M10 + M9 + M8) x 8
72℃ ≦ T < 80℃	V0(T) = V0(T24) - (T - 72) x M14 – (M13 + M12 + M11 + M10 + M9 + M8) x 8
80℃ ≦ T < 88℃	V0(T) = V0(T24) - (T - 80) x M15 – (M14 + M13 + M12 + M11 + M10 + M9 + M8) x 8

Table 4 Equation V0(T) at different temperature

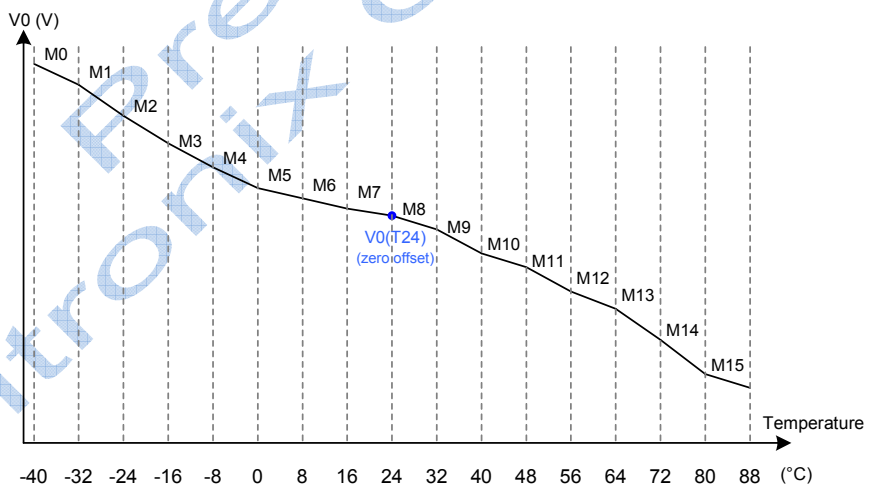


Figure 30 Temperature Gradient Compensation

Note:

- Please make sure to avoid any kind of heating source near ST75256 such as back light, to prevent Vop is not anticipative because of temperature compensation circuit is working.

7.6 Frequency Temperature Gradient Compensation Coefficient

7.6.1 Register Loading Detection

ST75256 will auto-switch frame rate in different temperature such as Figure 31. TA, TB and TC are frame rate switching temperature which can be defined by customer with instruction Temperature Range. FRA, FRB, FRC and FRD are switched frame rate which also can be defined by customer with instruction Frame Rate. The frame rate range is from 38.5Hz to 153Hz.

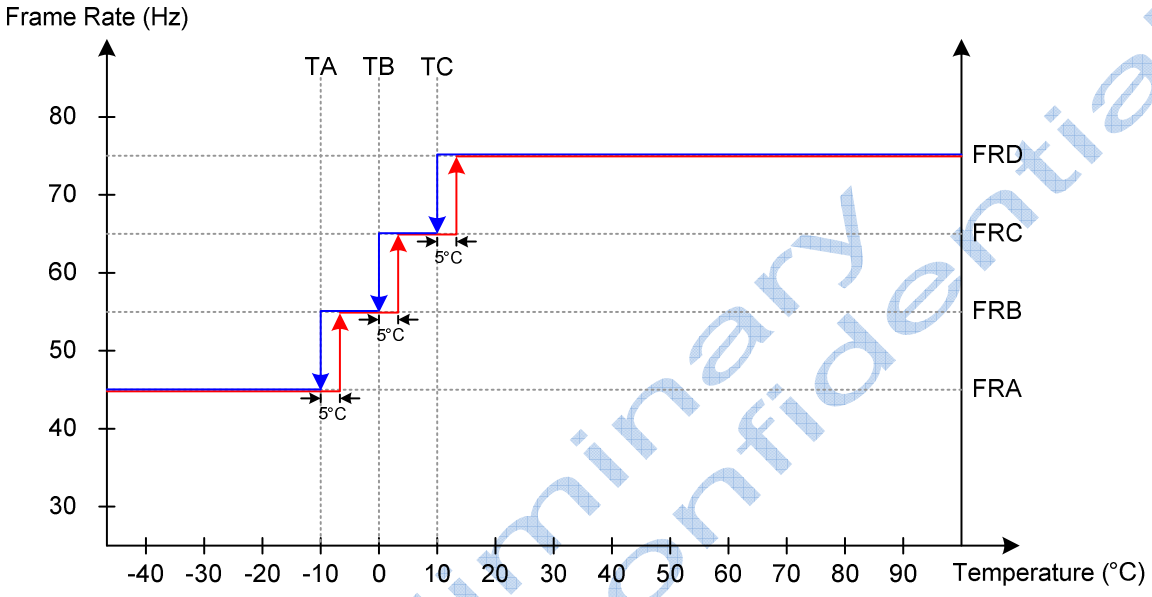


Figure 31 Frame Rate

8 RESET CIRCUIT

Setting RSTB pin to “L” can initialize internal function. While RSTB is “L”, no instruction can be accepted. RSTB pin must connect to the reset pin of MPU and initialization by RSTB pin is essential before operating. After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write a display pattern) before turning the Display ON.

The default values of registers are listed below:

Procedure		Hardware Reset
DDRAM Content		No Change
Setting Clock Dividing ratio		Not Divide
Duty Setting		1 Duty
N-Line Inversion		Frame Inversion
N-Line Inversion Mode		Inversion is independent from frame
Oscillation Mode		Oscillation OFF
Electronic Volume Control		VPR[8:0]=000h
Power Control		VB=0, VR=0, VF=0
Normal/Inverse Display		Normal
Partial Mode		Partial Mode OFF
Power Save Mode		Sleep in Mode
Display ON/OFF		Display OFF
Area Scroll Mode		Whole screen scroll
Start Line		00h
Normal/Reverse Direction of the Line Address		Normal
Normal/Reverse Direction of the Column Address		Normal
Address Scan Direction		Column direction
Column Address	Start Address	00h
	End Address	00h
Page Address	Start Address	00h
	End Address	00h
Partial Display Area	Start Address	00h
	End Address	00h
Read Modify Write		Disable
BIAS		1/14
Booster Level		X10

Table 5 The Default Values of Registers

9 COMMAND

9.1 INSTRUCTION TABLE

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
1.Extension Command	0	0	0	0	1	1	EXT1	0	0	EXT0	Set extension instruction
Ext[1:0]=0,0 (Extension Command 1)											
2.Display ON/OFF	0	0	1	0	1	0	1	1	1	DSP	Set LCD display DSP=0: Display off DSP=1: Display on
3.Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display INV=0: Normal display INV=1: Inverse display
4.All Pixel ON/OFF	0	0	0	0	1	0	0	0	1	AP	Set all pixel on mode AP=0: All pixel off mode AP=1: All pixel on mode
5.Display Control	0	0	1	1	0	0	1	0	1	0	Set display control CLD :Set CL dividing ratio LF[4:0] : Set N-line inversion counter DT[7:0] : Set the number of duty FI : Set the inversion type of frame at the end of common scan cycle
	1	0	0	0	0	0	0	CLD	0	0	
	1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	
	1	0	0	0	LF4	FI	LF3	LF2	LF1	LF0	
6.Power Save	0	0	1	0	0	1	0	1	0	SLP	Set power save mode SLP=0: Sleep out mode SLP=1: Sleep in mode
7.Set Page Address	0	0	0	1	1	1	0	1	0	1	Set Page Address Starting Page address: 00h≦YS≦28h Ending Page address: YS≦YE≦28h
	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
8.Set Column Address	0	0	0	0	0	1	0	1	0	1	Set Column Address Starting Column address: 00h≦XS≦FFh Ending Column address: XS≦XE≦FFh
	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
9.Data Scan Direction	0	0	1	0	1	1	1	1	0	0	Set normal/ inverse display of address and address scan direction
	1	0	0	0	0	0	0	C/L	MX	MY	
10.Write Data	0	0	0	1	0	1	1	1	0	0	Write data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
11.Read Data	0	0	0	1	0	1	1	1	0	1	Read data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
12.Partial In	0	0	1	0	1	0	1	0	0	0	Set partial area Starting partial display address: 00h≦PTS≦A1h Ending partial display address: 00h≦PTE≦A1h
	1	0	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	
	1	0	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
13.Partial Out	0	0	1	0	1	0	1	0	0	1	Exit the partial mode
14.Read/Modify/Write In	0	0	1	1	1	0	0	0	0	0	Enable read modify write
15.Read/Modify/Write Out	0	0	1	1	1	0	1	1	1	0	Disable read modify write
16.Scroll Area	0	0	1	0	1	0	1	0	1	0	Set scroll area
	1	0	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	
	1	0	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	
	1	0	NSL7	NSL6	NSL5	NSL4	NSL3	NSL2	NSL1	NSL0	
	1	0	0	0	0	0	0	0	SCM1	SCM0	
17.Set Start Line	0	0	1	0	1	0	1	0	1	1	Set scroll start address 00h≦SL≦A1h
	1	0	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	
18.OSC ON	0	0	1	1	0	1	0	0	0	1	Turn on the internal oscillator
19.OSC OFF	0	0	1	1	0	1	0	0	1	0	Turn off the internal oscillator
20.Power Control	0	0	0	0	1	0	0	0	0	0	Power circuit operation VB=0: OFF, VB=1: ON VF=0: OFF, VF=1: ON VR=0: OFF, VR=1: ON
	1	0	0	0	0	0	VB	0	VF	VR	
21.Set Vop	0	0	1	0	0	0	0	0	0	1	Set Vop
	1	0	0	0	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
	1	0	0	0	0	0	0	Vop8	Vop7	Vop6	
22.Vop Control	0	0	1	1	0	1	0	1	1	VOL	Control Vop VOL=0: Vop increase one step VOL=1: Vop decrease one step
23.Read Register Mode	0	0	0	1	1	1	1	1	0	REG	Set read register mode REG=0: read the register value of VPR[5:0] REG=1: read the register value of VPR[8:6]
24.Nop	0	0	0	0	1	0	0	1	0	1	No operation
25.Read Status	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Read status byte
26.Data Format Select	0	0	0	0	0	0	1	DO	0	0	DO=0; LSB on bottom (Default) DO=1; LSB on top
27. Display Mode	0	0	1	1	1	1	0	0	0	0	Set display mode DM=0 :Mono(Default) DM=1 :4Gray Scale Mode
	1	0	0	0	0	1	0	0	0	DM	
28.ICON Control	0	0	0	1	1	1	0	1	1	ICON	Enable/Disable ICON ICON=1 ; Enable ICON=0 ; Disable

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Ext[1:0]=0,1 (Extension Command 2)											
29.Analog Circuit Set	0	0	0	0	1	1	0	0	1	0	Set analog set BE[1:0]: Booster efficiency set BS[2:0]: Set bias ratio
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	BE1	BE0	
	1	0	0	0	0	0	0	BS2	BS1	BS0	
30.Booster Level	0	0	0	1	0	1	0	0	0	1	Set booster level
	1	0	1	1	1	1	1	0	BST1	BST0	
31. Driving Select	0	0	0	1	0	0	0	0	0	DS	Power type DS=0: Internal (Default) DS=1 :External
32.High Power Mode	0	0	0	1	0	0	1	0	0	HPM	Set high power mode HPM=0 ; Normal Mode HPM =1 ; High Power Mode
33.Auto Read Control	0	0	1	1	0	1	0	1	1	1	Set auto-read instruction XARD=0: Enable auto read XARD=1: Disable auto read
	1	0	1	0	0	XARD	1	1	1	1	
34.OTP WR/RD Control	0	0	1	1	1	0	0	0	0	0	OTP WR/RD control WR/RD=0: Enable OTP read WR/RD=1: Enable OTP write
	1	0	0	0	WR/ RD	0	0	0	0	0	
35.OTP Control Out	0	0	1	1	1	0	0	0	0	1	OTP control out
36.OTP Write	0	0	1	1	1	0	0	0	1	0	OTP write
37.OTP Read	0	0	1	1	1	0	0	0	1	1	OTP read
38.OTP Selection Control	0	0	1	1	1	0	0	1	0	0	OTP selection control Ctrl=1: Disable OTP Ctrl=0: Enable OTP
	1	0	1	Ctrl	0	1	1	0	0	1	
39.OTP Programming Setting	0	0	1	1	1	0	0	1	0	1	OTP programming setting
	1	0	0	0	0	0	1	1	1	1	
40.Frame Rate	0	0	1	1	1	1	0	0	0	0	Frame rate setting in different temperature range
	1	0	0	0	0	FRA4	FRA3	FRA2	FRA1	FRA0	
	1	0	0	0	0	FRB4	FRB3	FRB2	FRB1	FRB0	
	1	0	0	0	0	FRC4	FRC3	FRC2	FRC1	FRC0	
	1	0	0	0	0	FRD4	FRD3	FRD2	FRD1	FRD0	
41.Temperature Range	0	0	1	1	1	1	0	0	1	0	Temperature range setting
	1	0	0	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	0	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	0	TC6	TC5	TC4	TC3	TC2	TC1	TC0	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
42.Temperature Gradient Compensation	0	0	1	1	1	1	0	1	0	0	Set temperature gradient compensation coefficient
	1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	
	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	
	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	
	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	
	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	
	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	
	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	
	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	
Ext[1:0]=1,0(Extension Command 3)											
43.Set ID	0	0	1	1	0	1	0	1	0	1	Set ID
	1	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
44 Read ID	0	0	0	1	1	1	1	1	1	RID	Read ID RID=1 ; Enable RID=0 ; Disable
	0	1	D7	D6	D5	D4	D3	D2	D1	D0	

9.2 INSTRUCTION DESCRIPTION

9.2.1 Extension Command

This instruction sets the extension instruction mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	EXT1	0	0	EXT0

Flag	Description
EXT[1:0]	Extension command mode. EXT[1:0]=[0,0]: Extension command 1. EXT[1:0]=[0,1]: Extension command 2. EXT[1:0]=[1,0]: Extension command 3.

"Extension Command 1"

9.2.2 Display ON/OFF

This instruction turns the display ON or OFF. When ST75256 enters display off, the display output is blank regardless of the content of DDRAM. When ST75256 enters display on (exit display off), the display output is according to content of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	1	1	DSP	DSP=0: Display off mode DSP=1: Display on mode

9.2.3 Inverse Display

This instruction would inverse the scanned data without recover the content of DDRAM. As the result, the ON and OFF status of all pixels are interchanged.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	1	INV	INV=0: Normal display INV=1: Inverse display

9.2.4 All Pixel ON/OFF

When ST75256 enters all pixels on or off mode, all display pixels are turned on or off regardless of the content of DDRAM. The content of DDRAM is not changed by setting All Pixel ON/OFF. After execute the instruction of Partial Mode, the display mode will exit all pixel on/off mode then enter normal mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	1	AP	AP=0: All pixel off mode AP=1: All pixel on mode

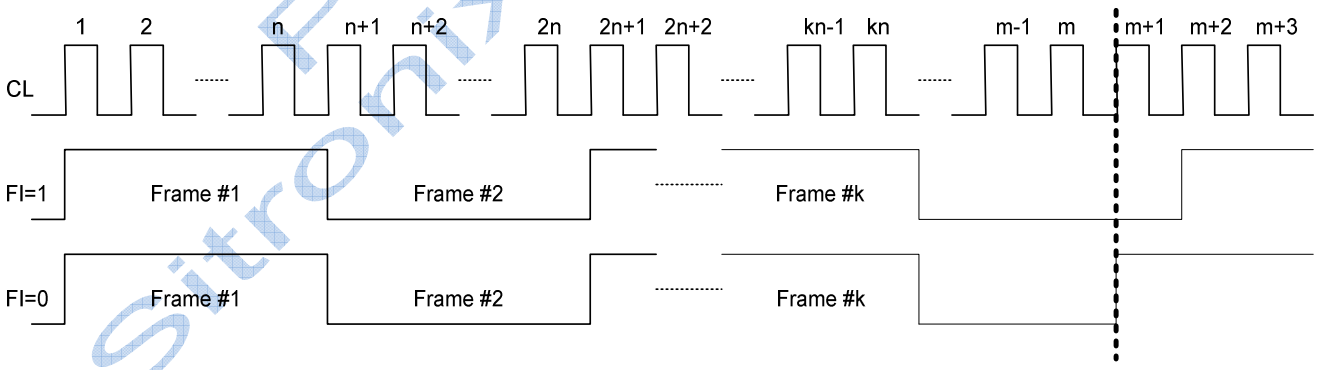
9.2.5 Display Control

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	1	0	1	0	CLD: CL Dividing ratio
1	0	0	0	0	0	0	CLD	0	0	DT: Duty of the module
1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	LF: Line cycles in a frame
1	0	0	0	LF4	FI	LF3	LF2	LF1	LF0	FI: Inversion type of frame

CLD: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.
CLD=0: not divide, CLD=1: 2 divisions.

DT [7:0] specifies the duty of the module.
The parameter setting of duty is the number of physical display duty decreasing by one(-1). For example, the parameter must set A1h when the LCD display duty is 162.

LF[4:0] specifies number of line cycles (range from 2 to 32) in a frame.
Number of line cycles-1 = LF4 x 2^4 + LF3 x 2^3 + LF2 x 2^2 + LF1 x 2^1 + LF0 x 2^0
For example, 11 line cycles in a frame → 11-1=10 → (LF4, LF3, LF2, LF1, LF0) = (0, 1, 0, 1, 0)
In the default, 11 line cycles in a frame is selected.
FI decides the inversion type of frame at the end of common scan cycle while the number of duty is not divisible by the number of line cycles per frame. For example, in the application of 1/m duty and n line cycles in a frame set, the difference of the choice in FI is shown as the following figure.
m = n x k + r, where m, n, k, and r are all whole numbers, and r is the remainder of m divided by n (r < n).



9.2.6 Power Save

When ST75256 enters the sleep in mode, the mode causes the LCD module entering the minimum power consumption mode. All of operations (e.g. the DC/DC converter, internal oscillator and panel scanning) are stopped. When ST75256 enters sleep out mode (exit sleep in mode), the DC/DC converter and internal oscillator are started.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	1	0	SLP	SLP=0: Sleep out mode SLP=1: Sleep in mode

9.2.7 Set Page Address

This instruction is used to define area of DDRAM where MCU can access. The page address is automatically increased by one (+1) after column address counter is over XE[7..0]. The page address will return to starting page address YS[7..0] immediately when the page address increases one over the ending page address YE[7..0]. The YS[7..0] setting must be equal to or less than YE[7..0]. When YS[7..0] or YE[7..0] is great than 28h, out of DDRAM range will be ignored.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	1	0	1	0	1	YS: Starting page address YE: Ending page address
1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

Note: The range of address is 00h~28h.

9.2.8 Set Column Address

This instruction is used to define area of DDRAM where MCU can access. The column address is automatically increased by one (+1) after each DDRAM access. After the ending column address XE[15..0], column address returns to starting column address XS[15..0]. The XS[15..0] setting that must be equal to or less than XE[15..0]. When XS[15..0] or XE[15..0] is great than FFh, out of DDRAM range will be ignored.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	0	1	0	1	XS: Starting column address XE: Ending column address
1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

Note: The range of address is 00h~FFh.

9.2.9 Data Scan Direction

This instruction defines the write/read scanning direction of DDRAM.

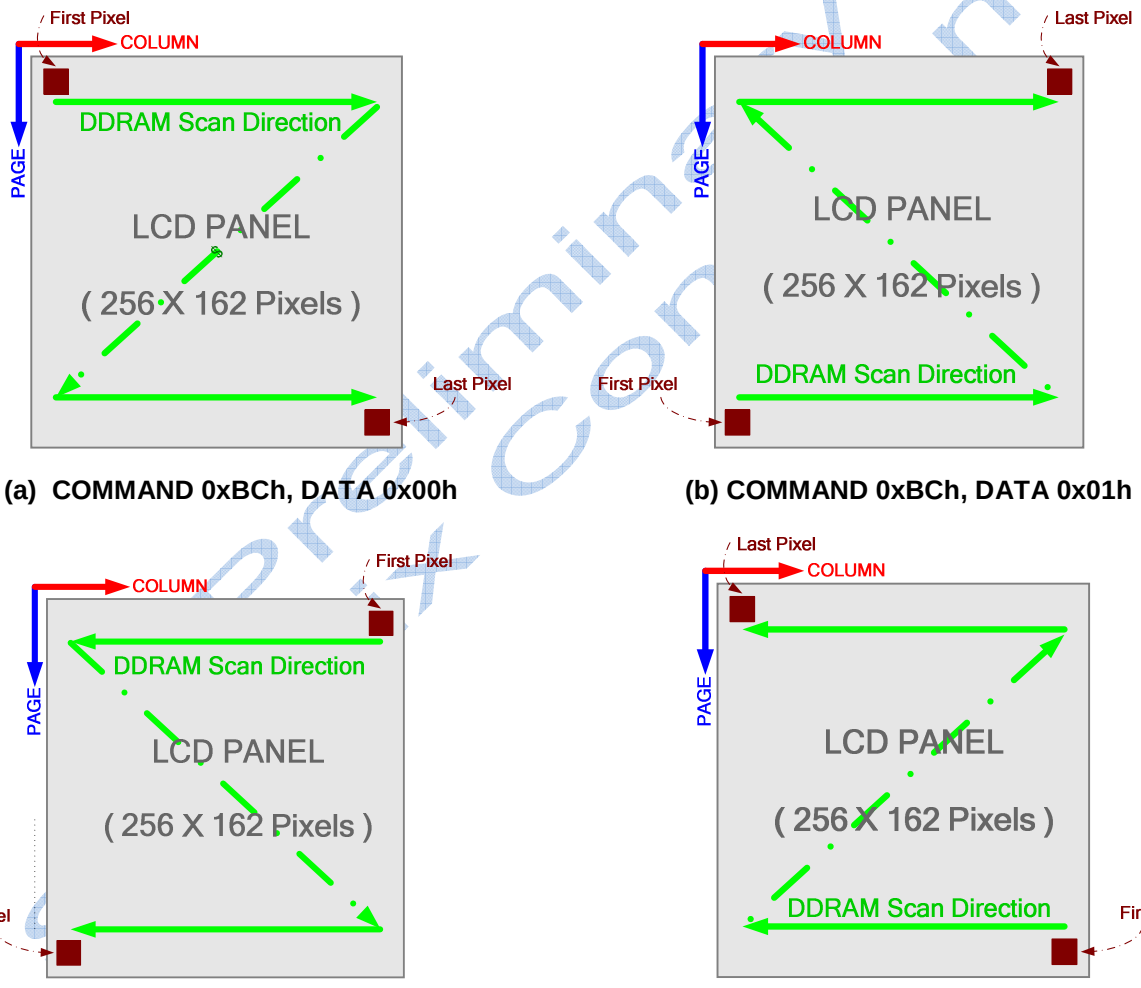
A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	1	1	0	0	Specify COM scan direction
1	0	0	0	0	0	0	CL	MX	MY	

CL: Address-scan direction. CL =0: In the column direction, CL =1: In the page direction

MX: Normal/reverse direction of the column address. MX =0: Normal, MX =1: Reverse

MY: Normal/inverse direction of the page address. MY =0: Normal, MY =1: Inverse

"CL=0"



(a) COMMAND 0xBCh, DATA 0x00h

(b) COMMAND 0xBCh, DATA 0x01h

(c) COMMAND 0xBCh, DATA 0x02h

(d) COMMAND 0xBCh, DATA 0x03h

Figure 32 Different RAM accessing setup under COMMAND 0xBCh

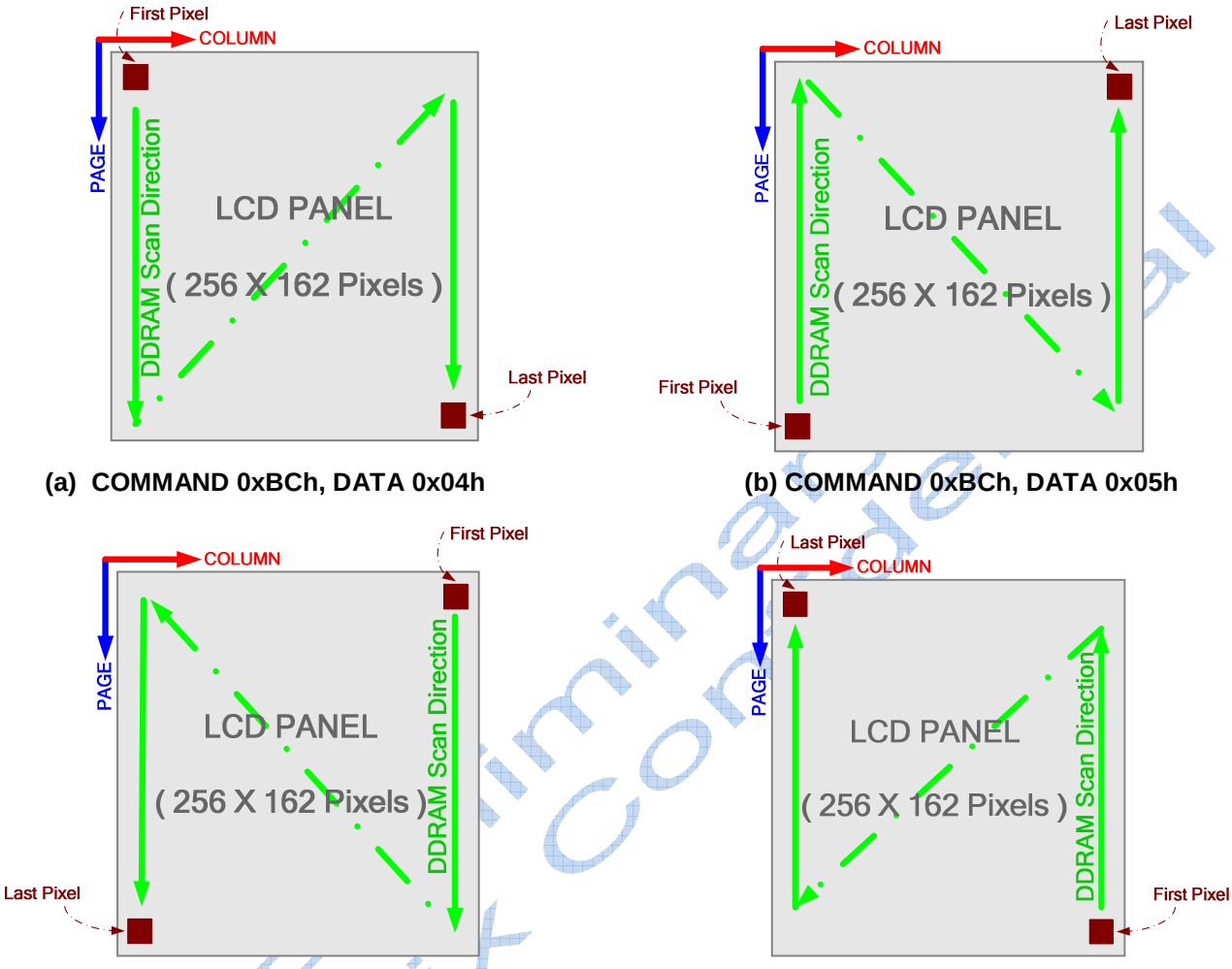
(a) DATA 0x00h (CL=0, MX=0, MY=0)

(b) DATA 0x01h (CL=0, MX=0, MY=1)

(c) DATA 0x02h (CL=0, MX=1, MY=0)

(d) DATA 0x03h (CL=0, MX=1, MY=1)

"CL=1"



(a) COMMAND 0xBCh, DATA 0x04h

(b) COMMAND 0xBCh, DATA 0x05h

(c) COMMAND 0xBCh, DATA 0x06h

(d) COMMAND 0xBCh, DATA 0x07h

Figure 33 Different RAM accessing setup under COMMAND 0xBCh

(e) DATA 0x04h (CL=1, MX=0, MY=0)

(f) DATA 0x05h (CL=1, MX=0, MY=1)

(g) DATA 0x06h (CL=1, MX=1, MY=0)

(h) DATA 0x07h (CL=1, MX=1, MY=1)

9.2.10 Write Data

This instruction is used to transfer data from MCU to DDRAM without changing status of ST75256. The column address and page address will be reset to starting column address (XS) and starting page address (YS) when this instruction is accepted. The pre-instruction is defined to enter write DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. Write Display Data would be stopped when any other instruction is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	1	1	0	0	Write display data to DDRAM
1	0	D7	D6	D5	D4	D3	D2	D1	D0	

9.2.11 Read Data

The instruction is used to transfer data from DDRAM to MCU without changing status of ST75256. The column address and page address will be reset to staring column address (XS) and starting page address (YS) when this instruction is accepted. The pre-instruction is defined to enter read DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. Read Display Data would be stopped when any other instruction is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	1	1	0	1	Read data from DDRAM
1	1	D7	D6	D5	D4	D3	D2	D1	D0	

9.2.12 Partial In

This instruction is to specify the partial display area. It will turn on partial display of the screen (dividing screen by lines) to save power.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	0	0	PTS: Start line address PTE: End line address
1	0	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	
1	0	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	

Only the address of the display line can be specified for the partial display. Do not specify an address not to be displayed when scrolled

9.2.13 Partial Out

This instruction is used to exit the PARTIAL DISPLAY MODE.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	0	1	Exit the partial display mode

9.2.14 Read /Modify/Write In

This command is used paired with the “Read/Modify/Write Out” command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	0	Enable read/modify/write

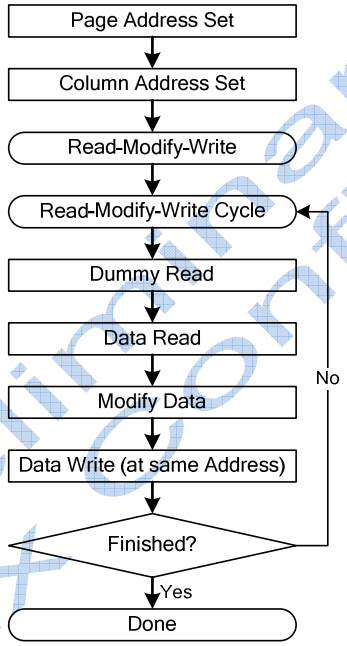


Figure 34 Command Sequence for Read/Modify/Write

9.2.15 Read /Modify/Write Out

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	1	0	Disable read/modify/write

9.2.16 Scroll Area

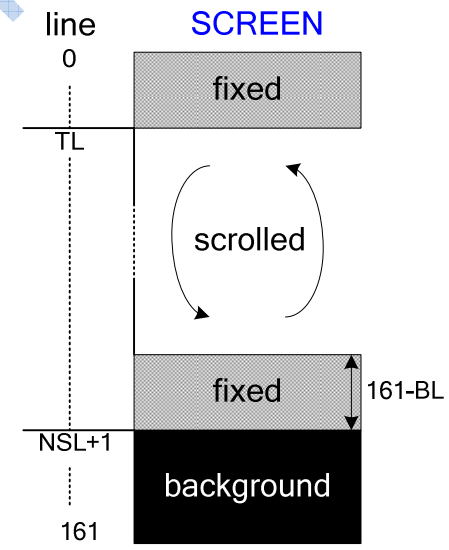
This command specifies the scrolling type of area, fixed area and scrolled area.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	1	0	TL: Top line address
1	0	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	BL: Bottom line address
1	0	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	NSL: Number of specified
1	0	NSL7	NSL6	NSL5	NSL4	NSL3	NSL2	NSL1	NSL0	lines
1	0	0	0	0	0	0	0	SCM1	SCM0	SCM: Area scroll mode

SCM[1:0]: It is used to specify the scrolling mode.

SCM1	SCM0	Scrolling Mode	Settings		
			Top line address (TL)	Bottom line address (BL)	Number of specified lines (NSL)
0	0	Center mode	Top(fixed area) height = Top address	Bottom(fixed area) height = 161-Bottom address	Bottom start address = Specified number
0	1	Top mode	0	Bottom(fixed area) height = 161-Bottom address	Bottom start address = Specified number
1	0	Bottom mode	Top(fixed area) height = Top address	161	161
1	1	Whole mode	0	161	161

DDRAM address of the top fixed area is set in the line address increasing direction starting with the 0th line. DDRAM address of the bottom fixed area is set in the line address decreasing direction starting with 161st line. The DDRAM addresses of other line fixed areas are assigned to the scrolled + background areas.



TL[7:0] is to specify the top line address of the scrolled + background areas. Specify the 0th line for the top screen scroll or whole screen scroll.

BL[7:0] specifies the bottom line address of the scroll + background areas. Specify the 161th line for the bottom or whole screen scroll. The relation that top line address < bottom line address must be maintained.

NSL[7:0] specifies a specific number of lines {Numbers of (Top fixed area +Scroll area) line-1}. In the case of the bottom scroll or whole screen scroll, the value is identical with BL[7:0].

The user can turn on the area scroll function by executing the area scroll set command first and then specifying the display start block of the scroll area with the scroll start address set command.

9.2.17 Scroll Start Address Set

This command is to specify which line address of DDRAM to be the start line content shown on screen. Note that you must execute this command after executing the area scroll set command. Scroll becomes available by dynamically changing the start line address.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	1	1	SL: Start line address
1	0	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	

Note : Don't repeat "Scroll Area (AAH)" instruction when "Scroll Start Address" is executed.

9.2.18 OSC ON

This command is used to turns on the internal oscillation circuit. It is valid only when the internal oscillation circuit CLS = HIGH

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	0	0	1	Turn on the internal OSC

9.2.19 OSC OFF

It turns off the internal oscillation circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	0	Turn off the internal OSC	

9.2.20 Power Control

This command is used to turn on or off the Booster circuit, voltage regulator circuit, and reference voltage.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	0	0	Power circuit control
1	0	0	0	0	0	VB	0	VF	VR	

Flag	Description
VB	VC=0: Internal booster is turned OFF VC=1: Internal booster is turned ON
VR	VR=0: Internal regulator is turned OFF VR=1: Internal regulator is turned ON
VF	VF=0: Internal follower is turned OFF VF=1: Internal follower is turned ON

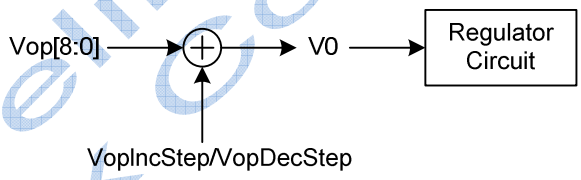
9.2.21 Set Vop

This instruction is used to adjust the optimum LCD supply voltage Vop.

The calculation of Vop is as shown blow: V0=3.6+(Vop[8:0]+VopIncStep-VopDecStep)x0.04

VopIncStep = Total Vop Increase Steps

VopDecStep = Total Vop Decrease Steps



A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	0	0	0	1	Set Vop
1	0	0	0	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
1	0	-	-	-	-	-	Vop8	Vop7	Vop6	

The suggestion of usable V0 voltage is shown below (assume VopIncStep/ VopDecStep=0):

Vop8	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	V0 (V)
0	0	1	0	1	0	1	0	1	7.00
0	0	1	0	1	0	1	1	0	7.04
0	0	1	0	1	0	1	1	1	7.08
:	:	:	:	:	:	:	:	:	:
1	0	1	1	0	0	1	0	0	15.92
1	0	1	1	0	0	1	0	1	15.96
1	0	1	1	0	0	1	1	0	16.00

9.2.22 Vop Control

This command is used to increase/decrease Vop step by one. Each step is 0.04V.

VOL=0; Vop increase one step

VOL=1; Vop decrease one step

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	VOL	Adjust Vop step by one

9.2.23 Read Register Mode

Execute the Read Register Mode and Read Status commands in succession to read the value of specified register.

REG=0 ; read the VPR[5:0] value of Vop set

REG=1 ; read the VPR[8:6] value of Vop set

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	1	1	1	0	REG	Set read register mode

Execute the “Read Status” command immediately after this command and execute the “NOP” command after the “Read Status” command.

9.2.24 NOP

This command does not affect the operation but has the function of canceling the IC test mode. Thus, it is recommended to enter it periodically to prevent malfunctioning due to noise and so on.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	1	0	1	No operation

9.2.25 Read Status

The command is to read the internal condition of the IC. One status can be displayed depending on the setting status after reset or after NOP operation

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	Status Data								Read status byte

Data Bus	Flag	Description
D7	Scroll Area Mode	Refer to SCM1
D6	Scroll Area Mode	Refer to SCM0
D5	RWM ON/OFF	0 : Out ; 1: In
D4	Data Scan Direction	0 : Column ; 1: Page
D3	Display ON/OFF	0 : OFF; 1: ON
D2	OTP Access	0 : OutAccess; 1: InAccess
D1	Inverse Display	0 : Inverse; 1: Normal
D0	Partial Display	0 : OFF; 1: ON

9.2.26 Data Format Select

Top/bottom mode sets data order.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	0	1	DO	0	0	Select LSB position

Flag	Description
DO	DO=0: LSB is on bottom ; D7→D0 (Default) DO=1: LSB is on top; D0→D7

9.2.27 Display Mode

This instruction defines the display mode is gray scale mode or monochrome mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	0	0	0	Set display mode DM=0 :Mono(Default) DM=1 :4Gray Scale Mode
1	0	0	0	0	1	0	0	0	DM	

9.2.28 ICON Control

This instruction is used to enable/disable ICON.

ICON=0 ; Disable

ICON=1 ; Enable

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	1	0	1	1	ICON	Enable/Disable ICON

Ensure to write B/W data to DDRAM in 4 gray scale mode.

"Extension Command 2"

9.2.29 Analog Circuit Set

This instruction is used to set booster efficiency and bias ratio.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	0	1	0	Analog setting
1	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	BE1	BE0	
1	0	0	0	0	0	0	BS2	BS1	BS0	

Booster Efficiency set

BE1	BE0	Frequency on booster capacitors (Hz)
0	0	3K
0	1	6K (Default)
1	0	12K
1	1	24K

Select LCD bias ratio of the voltage required for driving the LCD

BS2	BS1	BS0	LCD bias
0	0	0	1/14 (Default)
0	0	1	1/13
0	1	0	1/12
0	1	1	1/11
1	0	0	1/10
1	0	1	1/9

9.2.30 Booster Level

This instruction is used to control the built-in booster circuit to provide the power source of the built-in regulator.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	0	0	1	Analog setting
1	0	1	1	1	1	1	0	BST1	BST0	

BST1	BST0	Booster Level
0	1	X6
1	0	X8
1	1	X10 (Default)

9.2.31 Driving Select

This instruction is used to decide power source mode.

DS=0 ; Internal (default)

DS=1 ; External

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	0	0	DS	Power source select

9.2.32 High Power Mode

This instruction sets high power mode to enhance power efficiency.

HPM=0 ; Normal Mode

HPM=1 ; High Power Mode

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	0	0	HPM	Set High Power Mode

9.2.33 Auto Read Control

This instruction is used to set status of OTP auto read to enable or disable.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	1	XARD=0: Enable auto read
1	0	1	0	0	XARD	1	1	1	1	XARD=1: Disable auto read

9.2.34 OTP WR/RD Control

This instruction is used to set status of OTP that write to OTP or read from OTP.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	0	WR/RD=0: Enable OTP read WR/RD=1: Enable OTP write
1	0	0	0	WR /RD	0	0	0	0	0	

9.2.35 OTP Control Out

This instruction is used to cancel the OTP control.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	1	OTP control out

9.2.36 OTP Write

This instruction is used to trigger OTP programming procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	1	0	OTP programming procedure

9.2.37 OTP Read

This instruction is used to trigger OTP programming procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	1	0	OTP programming procedure

9.2.38 OTP Selection Control

This instruction is used to define OTP selection control.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	0	0	Ctrl=1: Disable OTP
1	0	1	Ctrl	0	1	1	0	0	1	Ctrl=0: Enable OTP

9.2.39 OTP Programming Setting

This instruction is used to set OTP write timing.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	0	1	OTP programming setting
1	0	0	0	0	0	1	1	1	1	

9.2.40 Frame Rate

The instruction is used to define frequency of frame rate in different temperature range as shown in **Figure 31**

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	0	0	0	FRA: FR in temp. -30℃ to TA FRB: FR in temp TA to TB FRC: FR in temp. TB to TC FRD: FR in temp TC to 90℃
1	0	-	-	-	FRA4	FRA3	FRA2	FRA1	FRA0	
1	0	-	-	-	FRB4	FRB3	FRB2	FRB1	FRB0	
1	0	-	-	-	FRC4	FRC3	FRC2	FRC1	FRC0	
1	0	-	-	-	FRD4	FRD3	FRD2	FRD1	FRD0	

FRx4	FRx3	FRx2	FRx1	FRx0	Frame Rate (Hz)
0	0	0	0	0	38.5
0	0	0	0	1	38.5
0	0	0	1	0	38.5
0	0	0	1	1	40.0
0	0	1	0	0	41.5
0	0	1	0	1	46.0
0	0	1	1	0	46.0
0	0	1	1	1	49.0
0	1	0	0	0	51.0
0	1	0	0	1	53.0
0	1	0	1	0	55.0
0	1	0	1	1	55.0
0	1	1	0	0	69.0
0	1	1	0	1	73.0
0	1	1	1	0	76.5
0	1	1	1	1	76.5

FRx4	FRx3	FRx2	FRx1	FRx0	Frame Rate (Hz)
1	0	0	0	0	77.0
1	0	0	0	1	77.0
1	0	0	1	0	77.0
1	0	0	1	1	80.0
1	0	1	0	0	83.0
1	0	1	0	1	92.0
1	0	1	1	0	92.0
1	0	1	1	1	98.0
1	1	0	0	0	102.0
1	1	0	0	1	106.0
1	1	0	1	0	110.0
1	1	0	1	1	110.0
1	1	1	0	0	138.0
1	1	1	0	1	146.0
1	1	1	1	0	153.0
1	1	1	1	1	153.0

The frame rate table is used for 162 duty. If the number of duty is changed, the frame rate will be different also.

9.2.41 Temperature Range

This instruction is used to define the temperature range for automatic frame rate adjustment according to current temperature as shown in **Figure 30**.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	0	1	0	TA[6 :0]=TA Temp.(℃)+40 TB[6:0]=TB Temp.(℃)+40 TC[6 :0]=TC Temp.(℃)+40
1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	

Temp. Range Value	Temp. Rising State (℃)	Temp. Falling State (℃)
Freq. changing point A	(TA[6:0]-40)+5	TA[6:0]-40
Freq. changing point B	(TB[6:0]-40)+5	TB[6:0]-40
Freq. changing point C	(TC[6:0]-40)+5	TC[6:0]-40

9.2.42 Temperature Gradient Compensation

This instruction is used to define the temperature gradient compensation coefficient. The temperature gradient compensation coefficient setting is shown as below table.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	1	0	0	Set temperature gradient compensation coefficient
1	0	MT13	MT12	MT11	MT10	MT03	MT02	MT01	MT00	
1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	
1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	
1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	
1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	
1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	
1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	
1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	

MTx3	MTx2	MTx1	MTx0	Mx (mV/℃)
0	0	0	0	0
0	0	0	1	-5
0	0	1	0	-10
:	:	:	:	:
1	1	0	1	-65
1	1	1	0	-70
1	1	1	1	-75

"Extension Command 3"

9.2.43 Set ID

This instruction is used to define the ID.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	0	1	Set ID
1	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	

9.2.44 Read ID

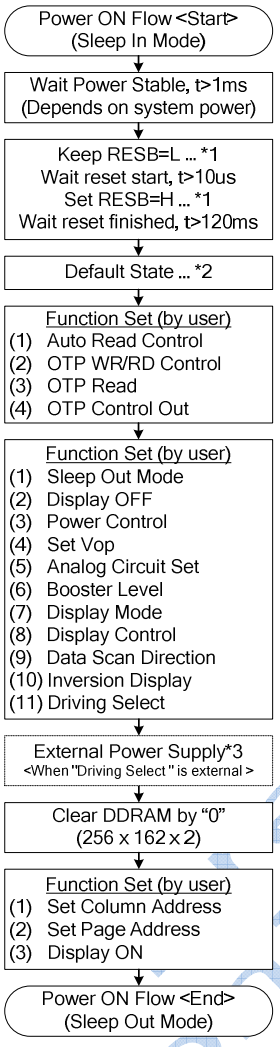
This instruction is used to read the ID.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	1	1	1	1	RID	Read ID
0	1	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RID=1 ; Enable RID=0 ; Disable

10 OPERATION FLOW

10.1 Power ON

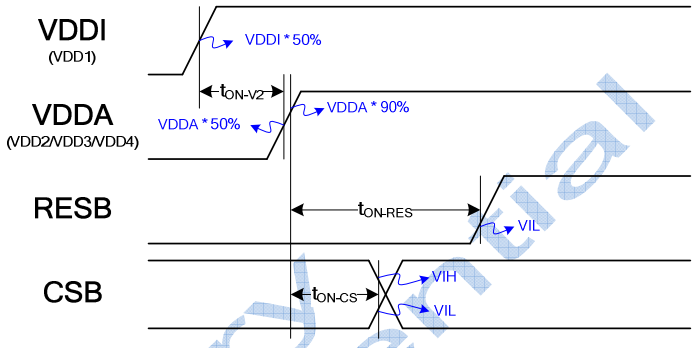
Referential Operation Flow	Operation Sequence



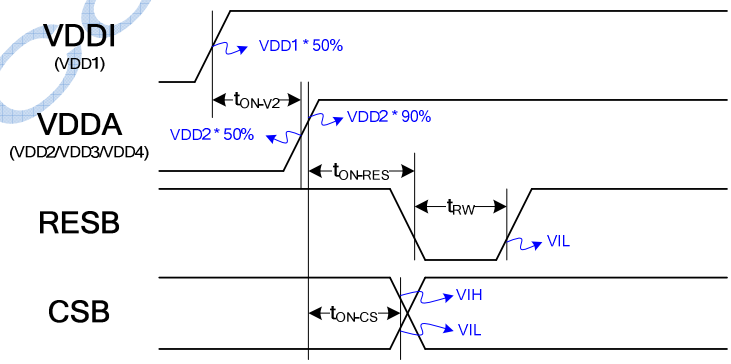
Note

1. Please refer to the specification of tRW and tR.
2. Refer to the section of Reset circuit.
3. The detail instruction functionality is described in section of INSTRUCTION DESCRIPTION.
4. The power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.
5. VDDA include VDD2, VDD3, VDD4

Case-1: RSTB=L while Power ON



Case-2: RSTB=H while Power ON



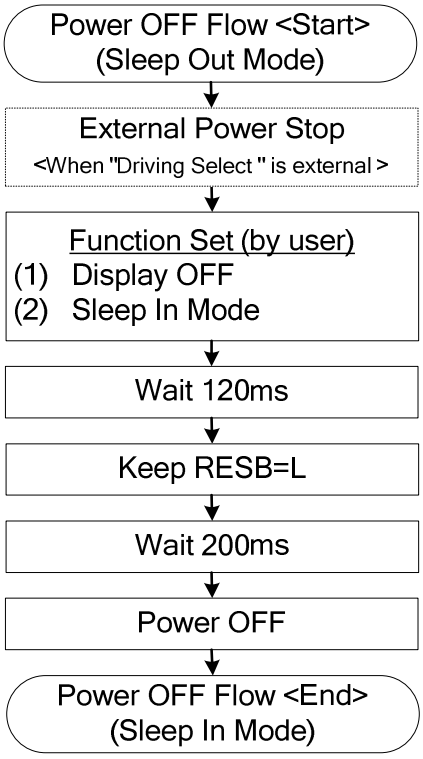
Item	Symbol	Requirement	Description
VDD2 power ON delay	t_{ON-V2}	No Limitation	● VDDI and VDDA can be applied in any order. IC will NOT be damaged when one of VDD1 and VDD2 is ON but another is OFF. ● Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage. ● Recommend Setting: -50ms ≤ t_{ON-V2} ≤ No Limitation.
RESB input time	t_{ON-RES}	Case-1 $t_{RW} \leq t_{ON-RES}$ Case-2 No Limitation	● RESB=L can be input at any time after power is stable. ● t_{RW} & t_R should match the timing specification of RESB. ● RESB has priority over CSB. ● Recommend Setting: 0 ≤ t_{ON-RES} ≤ 50 ms.
CSB input time	t_{ON-CS}	No Limitation	● CSB can be input at any time after power is stable.

Note:

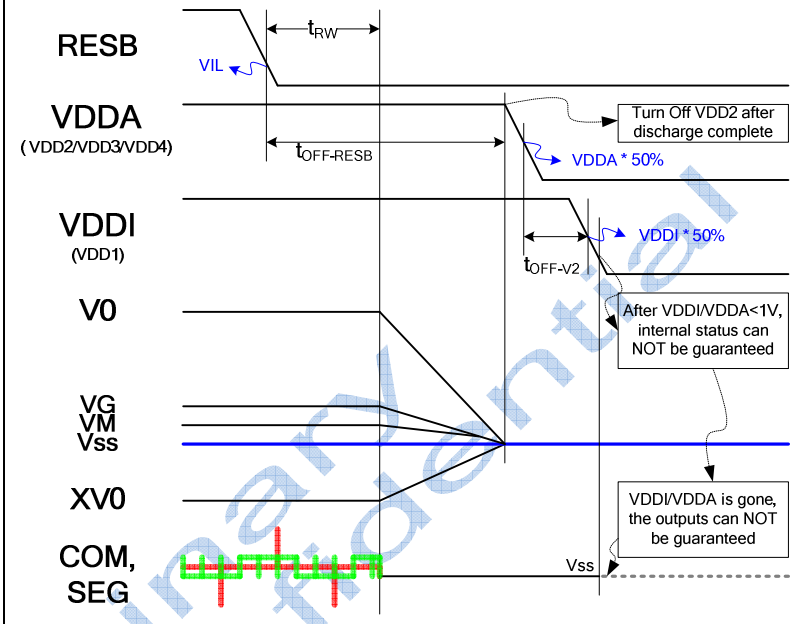
1. If the contents of internal registers are the same as default, the related commands can be ignored.
2. If RESB is held high or unstable during power ON, a successful hardware reset by RSTB is required after VDDI and VDDA are both stable (as illustrated in Case-2). Otherwise, correct functionality can NOT be guaranteed.

10.2 Power OFF

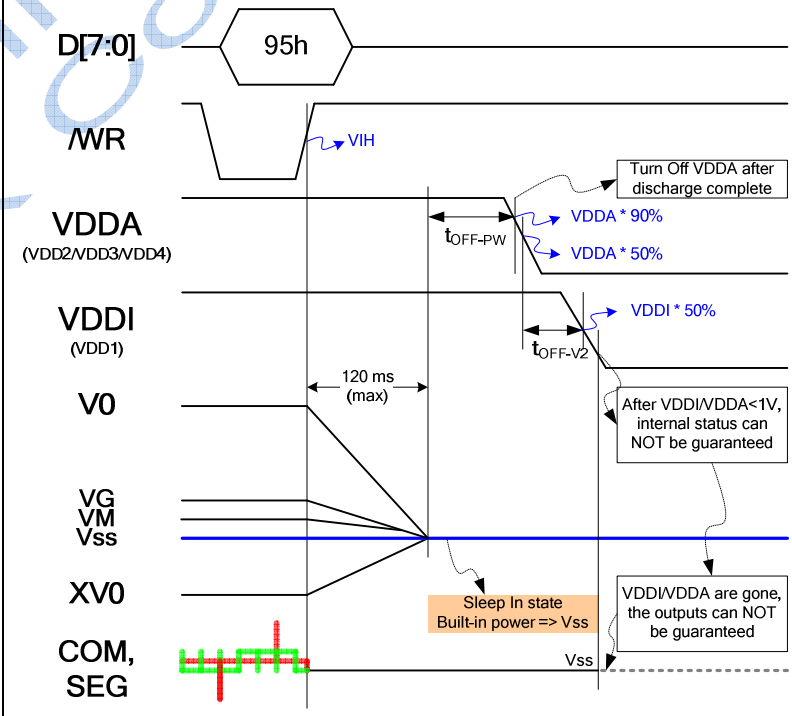
Referential Operation Flow	Operation Sequence



Case-1: Use RSTB



Case-2: Power OFF at Sleep State

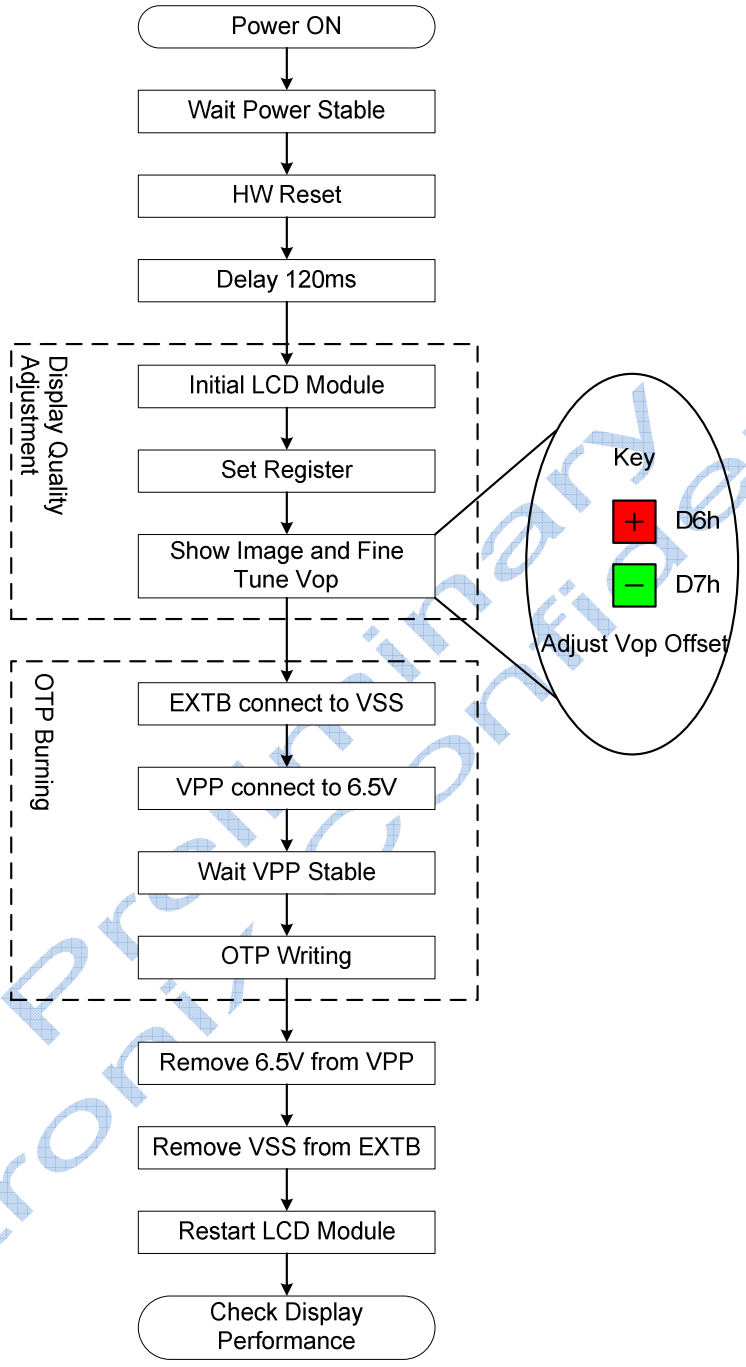


Item		Symbol	Requirement	Description
Power OFF Time	Case-1	$t_{OFF-RESB}$	200ms ≤$t_{OFF-RESB}$	● Power can be turned OFF after built-in power becomes VSS.
	Case-2	t_{OFF-PW}	0 ≤ t_{OFF-PW}	
VDD2 power ON delay		t_{OFF-V2}	No Limitation	● VDD1 and VDD2 can be powered down in any order. IC will NOT be damaged when one of VDD1 and VDD2 is ON but another is OFF. ● Recommend Setting: -50ms ≤ t_{OFF-V2} ≤ No Limitation.

Note: In Case-2, RSTB can fall to VSS at the same time as VDDI.

10.3 OTP Operation

10.3.1 Referential OTP Burning Flow



Note:

- In this section “+” and “-” key button, please execute command D6h to increase one step at Vop and execute command D7h to decrease one step at Vop.

10.3.2 Referential OTP Operation Code

```
void Initialization_ST75256(void)
{
        Reset_ms(10);
        Write(Command, 0x31);                  // Extension Command 2
        Write(Command, 0xD7);                  // Disable Auto Read
        Write(Data, 0x9F);
        Write(Command, 0xE0);                  // Enable OTP Read
        Write(Data, 0x00);
        Delay_ms(10);
        Write(Command, 0xE3);                  // OTP Up-Load
        Delay_ms(20);
        Write(Command, 0xE1);                  // OTP Control Out
        Write(Command, 0x30);                  // Extension Command 1
        Write(Command, 0x94);                  // Sleep Out
        Write(Command, 0xAE);                  // Display OFF
        Delay_ms(50);
        Write(Command, 0x20);                  // Power Control
        Write(Data, 0x0B);                     // VB, VR, VF All ON
        Write(Command, 0x81);                  // Set Vop = 14V
        Write(Data, 0x04);
        Write(Data, 0x04);
        Write(Command, 0x31);                  // Extension Command 2
        Write(Command, 0x32);                  // Analog Circuit Set
        Write(Data, 0x00);
        Write(Data 0x01);                      // Booster Efficiency =6KHz
        Write(Data, 0x00);                     //Bias=1/14
        Write(Command, 0x51);                  // Booster Level x10
        Write(Data, 0xFB);
        Write(Command, 0x30);                  // Extension Command 1
        Write(Command, 0XF0);                  // Display Mode
        Write(Data, 0x00);                     // Monochrome Mode
        Write(Command, 0xCA);                  // Display Control
        Write(Data, 0x00);                     // CL Dividing Ratio → Not Divide
        Write(Data, 0XA1);                     //Duty Set →162 Duty
        Write(Data, 0x00);                     //Frame Inversion
```

```
        Write(Command, 0xBC);          // Data Scan Direction
        Write(Data, 0x00);
        Write(Command, 0xA6);
        Write(Command, 0x31);          // Extension Command 2
        Write(Command, 0x40);          // Internal Power Supply

        Write(Command, 0x30);          // Extension Command 1
        Write(Command, 0x15);          // Column Address Setting
        Write(Data, 0x00);             // SEG0 -> SEG255
        Write(Data, 0xFF);

        Write(Command, 0x75);          // Page Address Setting
        Write(Data, 0x00);             // COM0 -> COM161
        Write(Data, 0x14);

        Clear_DDRAM();                 // Clear Whole DDRAM by "0"

        Write(Command, 0x30);          // Extension Command 1
        Write(Command, 0x15);          // Column Address Setting
        Write(Data, 0x00);             // SEG0 -> SEG255
        Write(Data, 0xFF);
        Write(Command, 0x75);          // Page Address Setting
        Write(Data, 0x00);             // COM0 -> COM161
        Write(Data, 0x14);

        Disp_Image();                  // Fill the DDRAM Data by Panel
                                       Resolution
        Write(Command, 0xAF);          // Display ON


void Set_OTP_Register(void)
{
        Write(Command, 0x38);          // Extension Command 3
        Write(Command, 0XD5);          // Set ID=1
        Write(Data, 0x01);
}
```

```
void Vop_Fine_Tune(void)
{
        Disp_Image();                   // Display the image

        Write(Command, 0x30);           // Extension Command 1
        Write(Command, 0xAF);           // Display ON
        Write(Command, 0XD6);           // Fine tuning Vop to adjust display
        or                              quality
        Write(Command, 0XD7);
}

void OTP_Write(void)
{
        Write(Command, 0x30);           // Extension Command 1
        Write(Command, 0xAE);           // Display OFF
        Delay_ms(50);                   // Delay 50ms

        Write(Command, 0x39);           //Enable OTP
        Write(Command, 0XD6);
        Write(Data, 0x10);

        Write(Command, 0x31);           // Extension Command 2
        Write(Command, 0XF0);           // Frame Rate = 77Hz
        Write(Data, 0x12);
        Write(Data, 0x12);
        Write(Data, 0x12);
        Write(Data, 0x12);

        Write(Command, 0xE4);           // OTP Selection Control
        Write(Data, 0x99);
        Write(Command, 0xE5);           // OTP Programming Setting
        Write(Data, 0x0F);
        Write(Command, 0xE0);           // OTP WR/RD Control
        Write(Data, 0x20);
        Delay_ms(100);                  // Delay 100ms
        Write(Command, 0xE2);           // OTP Write
        Delay_ms(100);                  // Delay 100ms
```

```
        Write(Command, 0xE1);          // OTP Control Out
        Write(Command, 0x30);          // Extension Command 1
    }
```

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

12 ABSOLUTE MAXIMUM RATINGS

VSS=0V

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1)	–0.3 ~ 4.0	V
Analog Power supply voltage	VDDA (VDD2~VDD4)	–0.3 ~ 4.0	V
LCD Power supply voltage	V0-XV0	–0.3 ~ 18	V
LCD Power supply voltage	VG	–0.3 ~ VDDA+0.3	V
LCD Power supply voltage	VM	–0.3 ~ VDDA+0.3	V
MPU Interface Input Voltage	Vin	–0.3 ~ VDDI+0.3	V
Operating temperature	TOPR	–30 to +85	℃
Storage temperature	TSTR	–55 to +125	℃

Note:

1. All voltages are respect to VSS unless otherwise noted (VSS1=VSS2=VSS3=VSS4=VSS5).
2. Insure the voltage levels of V0, VG, VM, VSS and XV0 always match the correct relation while operating: V0 ≥ VG > VM > VSS ≥ XV0
3. Stresses exceed the ranges listed above may cause permanent damage to IC. These values are stresses only. IC should be operated under DC/AC Characteristics condition for normal operation. If this condition is not met, IC operation may be error and the reliability may be deteriorated.
4. Parameters are valid in operating temperature range unless otherwise specified.
5. Interface input voltage range cannot exceed the maximum limitation of digital power supply voltage. Vin≦ 3.6V.

13 DC CHARACTERISTICS

VSS1=VSS2=VSS3=VSS4=VSS5=0V and Ta = –30 ~ 85 ℃, u nless otherwise specified.

Item	Symbol	Condition	Related Pin	Rating			Unit
				Min.	Typ.	Max.	
Digital Operating Voltage	VDDI		VDD1	1.7	–	3.6	V
Analog Operating Voltage	VDDA		VDD2~5	2.6	–	3.6	V
Input High-level Voltage	V_{IH}		MPU Interface	0.7*VDD1	–	VDD1	V
Input Low-level Voltage	V_{IL}		MPU Interface	VSS1	–	0.3*VDD1	V
Output High-level Voltage	V_{OH}		D[7:0]	0.8*VDD1	–	VDD1	V
Output Low-level Voltage	V_{OL}		D[7:0]	VSS1	–	0.2*VDD1	V
Input Leakage Current	I_{IL}	Vin = VDD1 or VSS1	MPU Interface	–1.0	–	1.0	μA
ON Resistance of LCD Drivers	R_{ON}	Ta=25℃ Bias=1/14 Vop=16V ΔV=10%	COM Drivers	–	1	–	KΩ
		Ta=25℃ Bias=1/14 VG=3V, ΔV=10%	SEG Drivers	–	1	–	KΩ
Frame Frequency	f_{FR}	VDDI=VDDA=3.3V, N-Line OFF, FR= 0x12 Duty=1/162, Ta = 25℃	–	72	77	82	Hz
Vop Voltage Output	Vop		V0-XV0[*1,2]	7		16	V
VG Voltage Output	VG		VG[*1,2]	1.8	–	VDD2-0.2	V
VM Voltage Output	VM		VM[*2]	0.9	VG/2	VDD2-0.2	V

Note:

1. V0, XV0 and VG include: V0I, V0O, V0S, XV0I, XV0O, XV0S, VGI, VGO & VGS.
2. V0, XV0, VG and VM do NOT support external power supply.

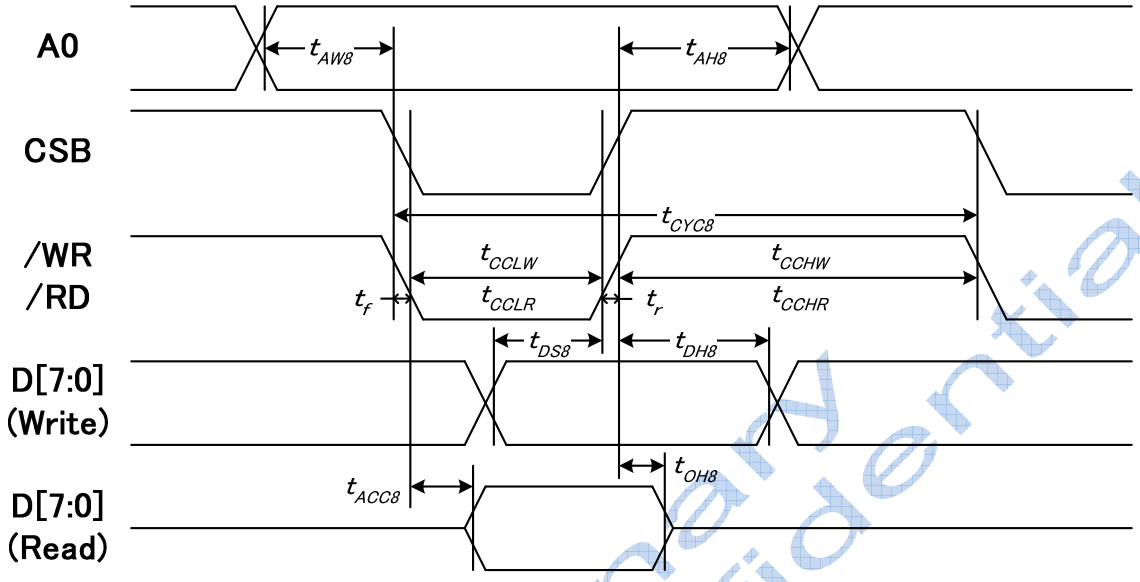
The current consumed by whole IC (bare die) with internal power system:

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Display ON Pattern: SNOW (Static)	ISS	VDDI=VDDA=3.3V, 10x Booster, Vop = 14.0V, Bias=1/14 N-Line OFF, f_{FR}=77Hz, Ta=25°C	–	800	1000	μA
Sleep In	ISS	VDDI=VDDA=3.3V, Ta=25°C	–	10	20	μA

Note: The current is DC characteristic of a “Bare Chip”

14 AC CHARATERISTIC

14.1 System Bus Timing for 8080 MCU Interface



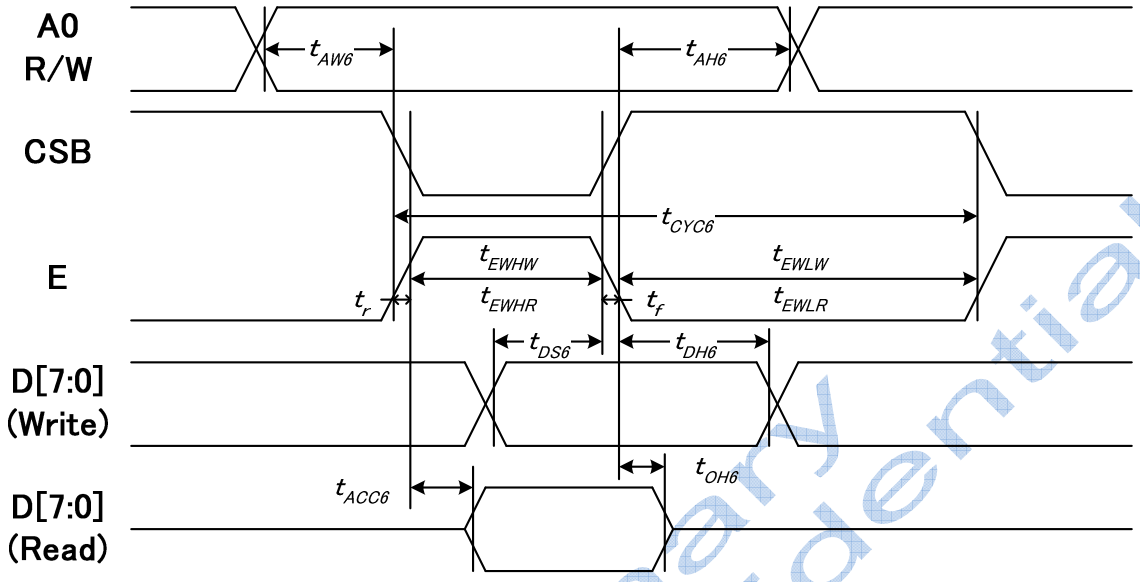
VDD1 = 1.8~3.3V, Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		20	—	ns
Address hold time		tAH8		0	—	
System cycle time (WRITE)	/WR	tCYC8		160	—	
/WR L pulse width (WRITE)		tCCLW		70	—	
/WR H pulse width (WRITE)		tCCHW		70	—	
System cycle time (READ)	RD	tCYC8		400	—	
/RD L pulse width (READ)		tCCLR		180		
/RD H pulse width (READ)		tCCHR		180		
WRITE Data setup time	D[7:0]	tDS8		15	—	
WRITE Data hold time		tDH8		15	—	
READ access time		tACC8	CL = 30 pF	—	100	
READ Output disable time		tOH8	CL = 30 pF	10	110	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

14.2 System Bus Timing for 6800 MCU Interface



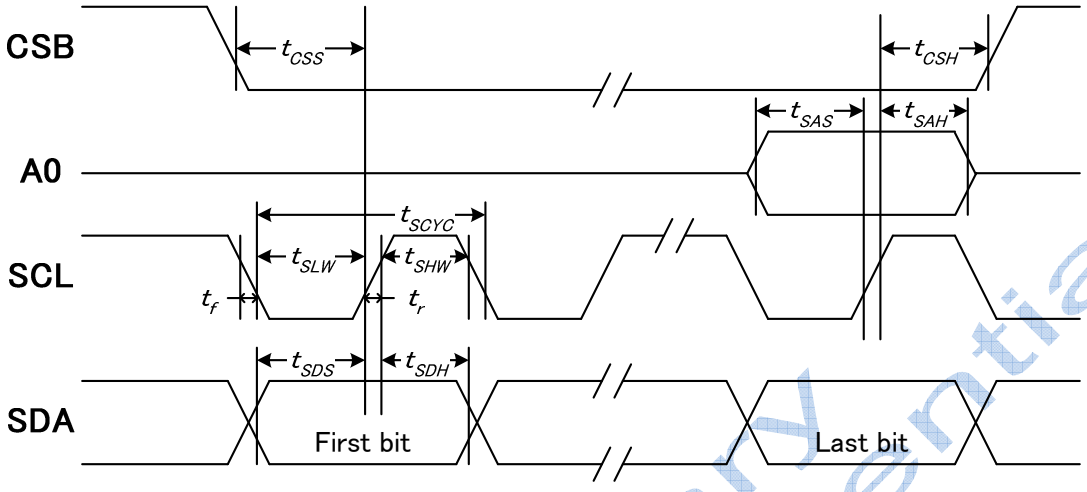
VDD1 = 1.8~3.3V, Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		20	—	ns
Address hold time		tAH6		0	—	
System cycle time (WRITE)	E	tCYC6		160	—	
Enable L pulse width (WRITE)		tEWLW		70	—	
Enable H pulse width (WRITE)		tEWHW		70	—	
System cycle time (READ)		tCYC6		400		
Enable L pulse width (READ)		tEWLR		180	—	
Enable H pulse width (READ)		tEWHR		180		
Write data setup time	D[7:0]	tDS6		15	—	
Write data hold time		tDH6		15	—	
Read data access time		tACC6	CL = 30 pF	—	100	
Read data output disable time		tOH6	CL = 30 pF	10	110	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

14.3 System Bus Timing for 4-Line SPI MCU Interface



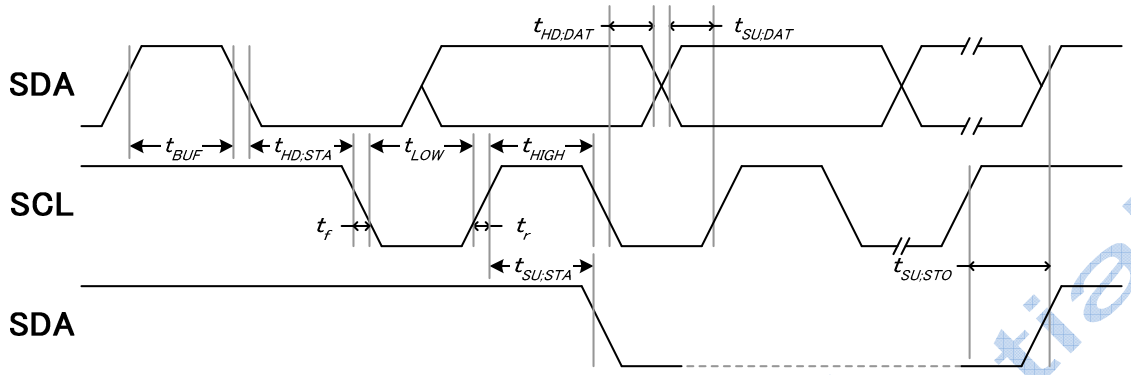
VDD1 = 1.8~3.3V, Ta = 25°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		60	—	ns
SCLK “H” pulse width		tSHW		30	—	
SCLK “L” pulse width		tSLW		30	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		20	—	
CSB-SCLK time	CSB	tCSS		20	—	
CSB-SCLK time		tCSH		20	—	
CS “H” pulse width		tCHW		0	-	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

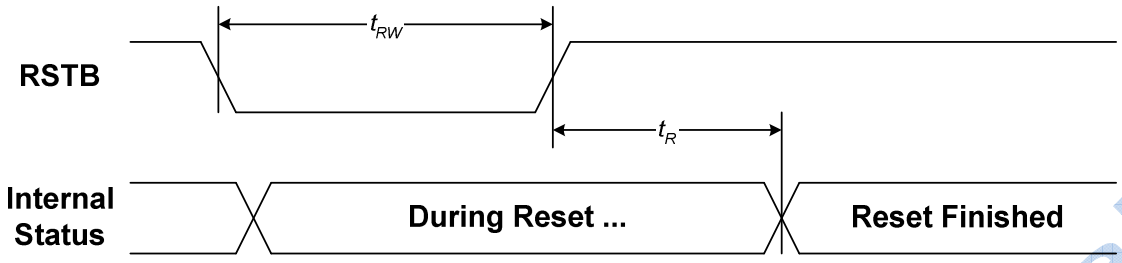
14.4 SERIAL INTERFACE (I²C Interface)



VDD1 = 1.8~3.3V, Ta =25°C

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
SCL clock frequency	SCL	fSCL		-	400	KHZ
SCL clock low period		tLOW		1.3	-	us
SCL clock high period		tHIGH		0.6	-	
Data set-up time	SDA	tSU;Data		0.1	-	
Data hold time		tHD;Data		0	0.9	
Setup time for a repeated START condition		tSU;STA		0.6	-	
Start condition hold time		tHD;STA		0.6	-	
Setup time for STOP condition		tSU;STO		0.6	-	
Bus free time between a STOP and START		tBUF		0.1	-	
Signal rise time	SCL SDA	tr		20+0.1Cb	300	ns
Signal fall time		tf		20+0.1Cb	300	
Capacitive load represented by each bus line		Cb			400	pF
Tolerable spike width on bus		tSW			50	ns

14.5 Reset Timing



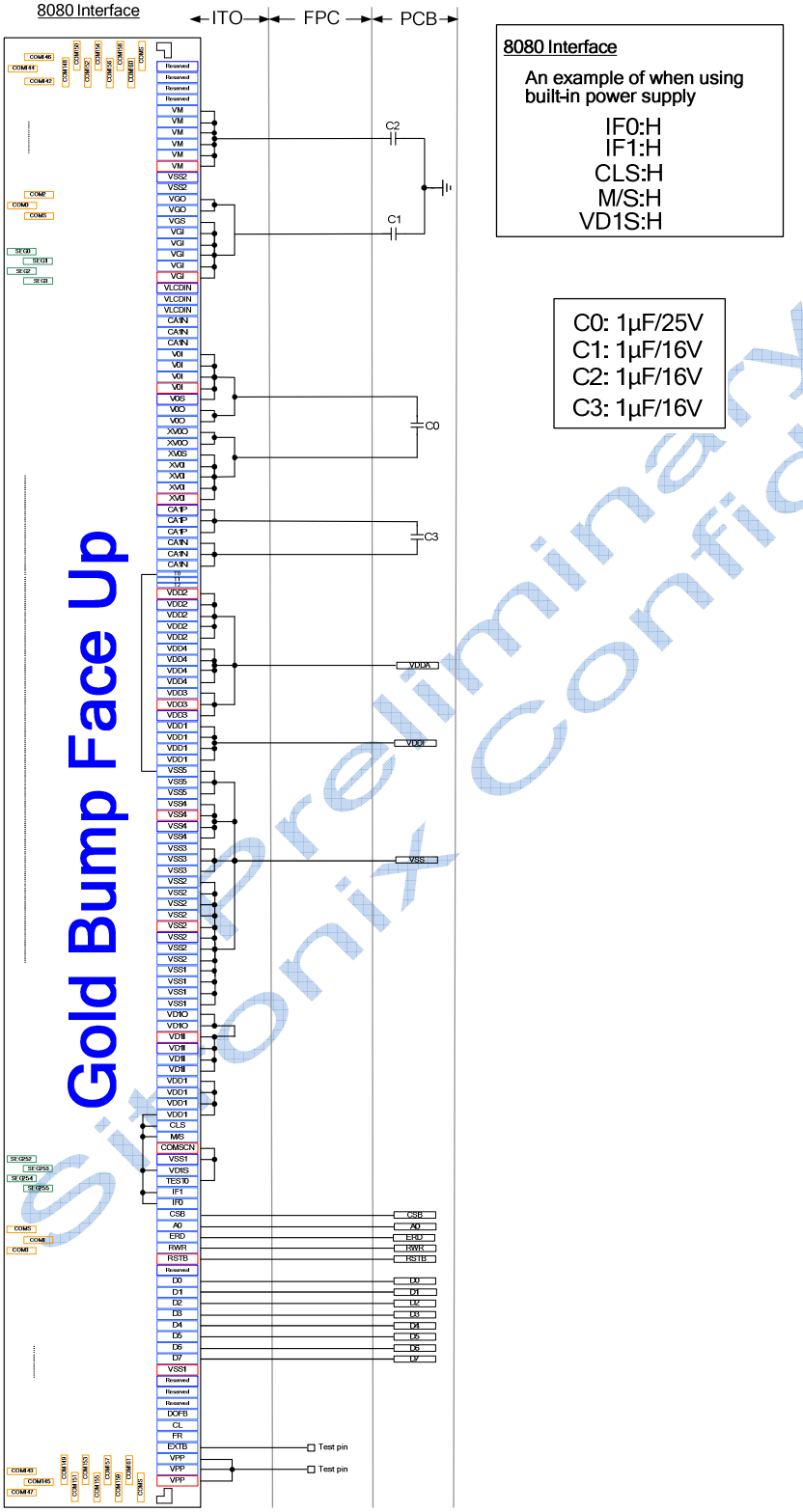
VDD1 = 1.8~3.3V, Ta = 25°C

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1	ms
Reset “L” pulse width	tRW		1	—	ms

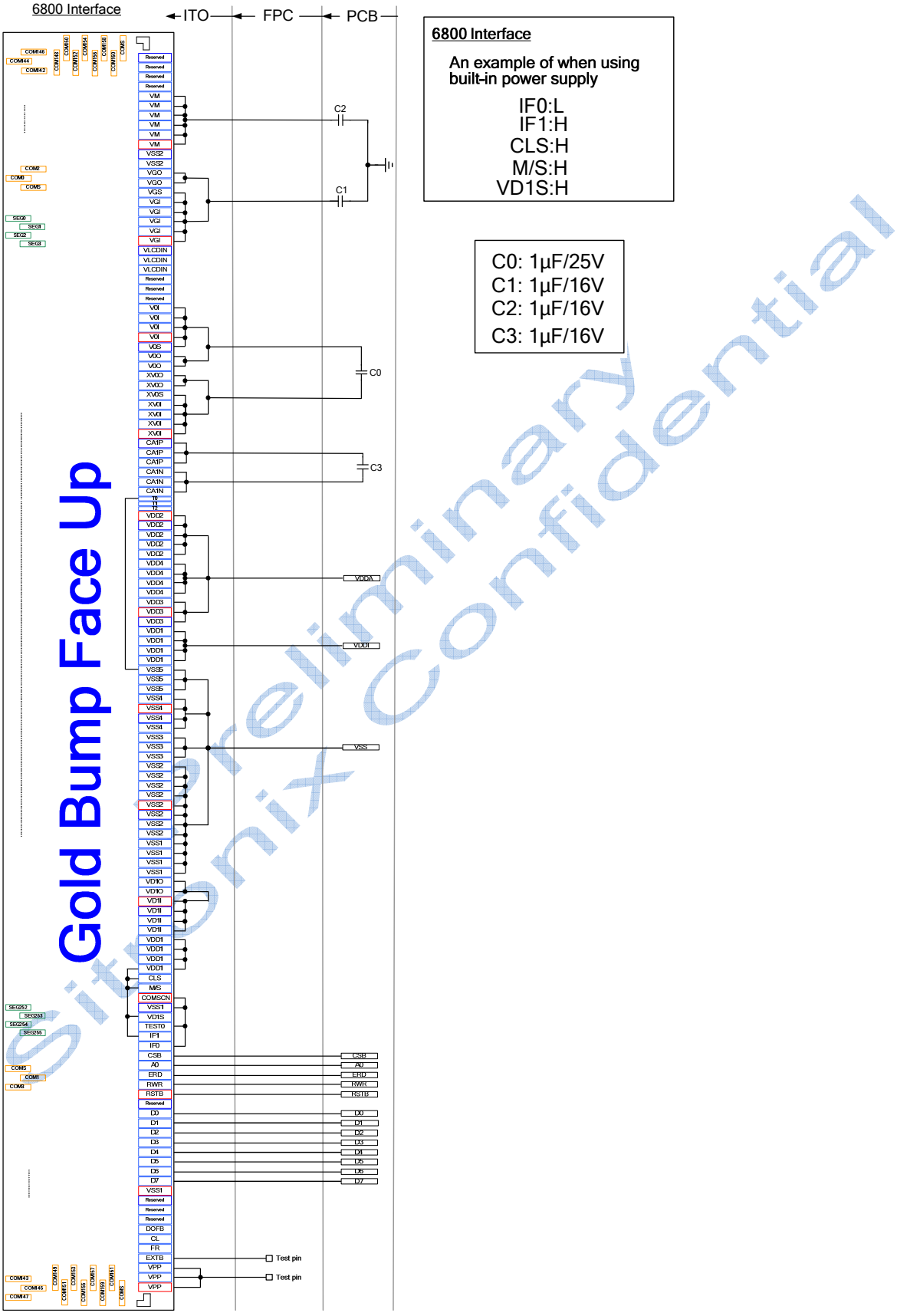
15 APPLICATION NOTE

15.1 Application Circuit

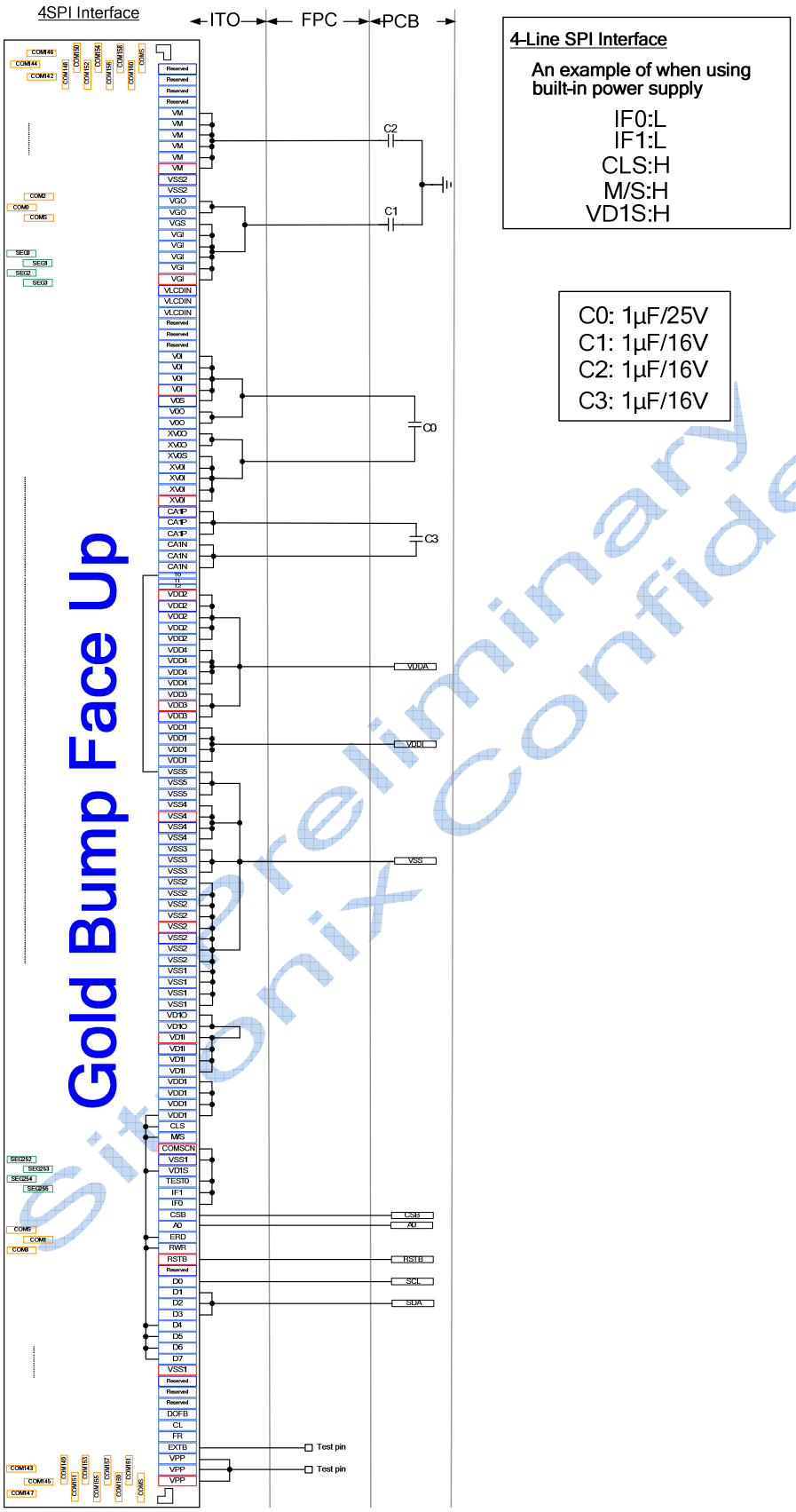
15.1.1 Parallel 8080 Interface



15.1.2 Parallel 6800 Interface



15.1.3 4-Line SPI Interface



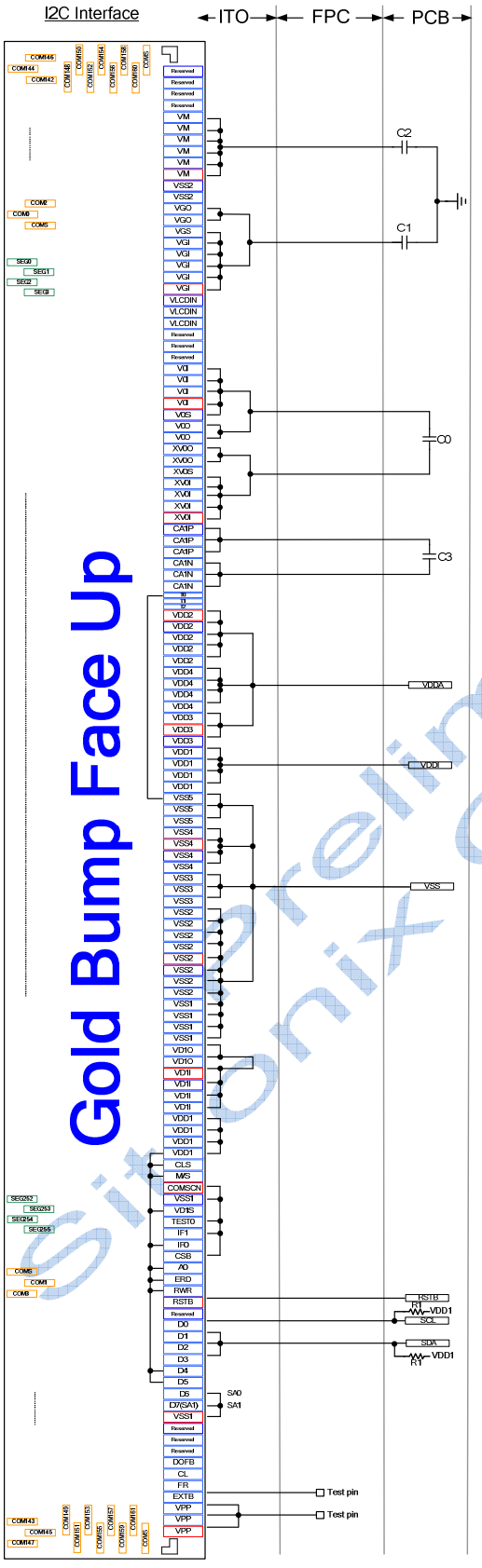
4-Line SPI Interface

An example of when using built-in power supply

IF0:L
IF1:L
CLS:H
M/S:H
VD1S:H

C0: 1µF/25V
C1: 1µF/16V
C2: 1µF/16V
C3: 1µF/16V

15.1.4 I²C Interface



I2C Interface

An example of when using built-in power supply

IF0:L
IF1:H
CLS:H
M/S:H
VD1S:H

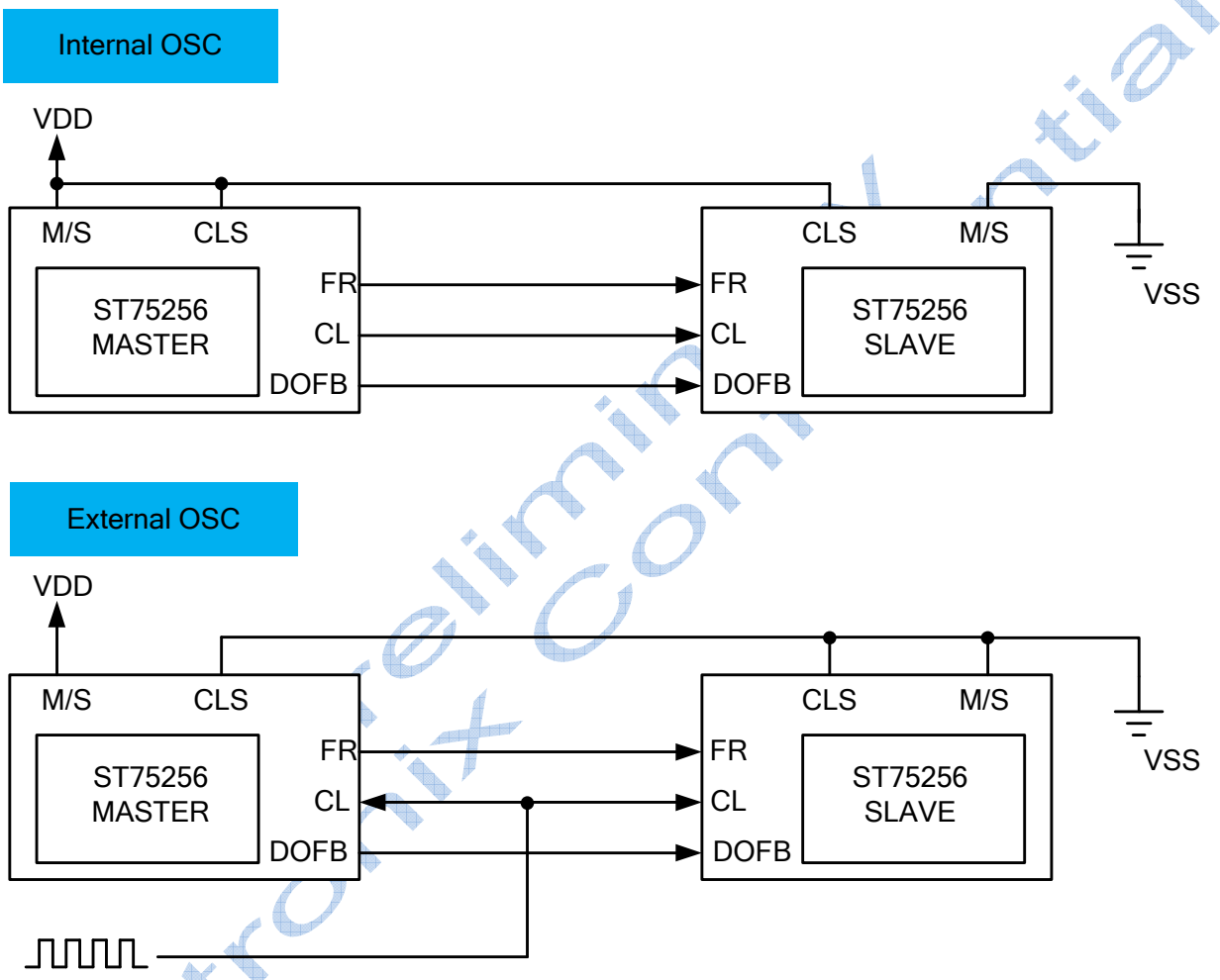
C0: 1µF/25V
C1: 1µF/16V
C2: 1µF/16V
C3: 1µF/16V
R1: 3~5 KΩ

16 MASTER/SLAVE MODE

Connections between LCD Drivers (Reference Example)

The display area of LCD panel can be extended horizontally by using two ST75256 chips. Use a same equipment type.

(1) ST75256 (master) → ST75256 (slave)



17 REVISION HISTORY

Version	Date	Description
V0.1	2013/02/05	● Preliminary.
V0.2	2013/03/13	● Modify I^2C interface protocol.
V0.3	2013/05/20	● Replace cover. ● Modify alignment mark coordinate. ● Add “PAD CENTER COORDINATES”. ● Modify PIN DESCRIPTION. ● Modify Block Diagram. ● Add V0 Restriction. ● Add Referential OTP Operation Code ● Add Application Note. ● Add MASTER/SLAVE MODE.
V0.3a	2013/06/28	● Add I/O pin name of PAD ARRANGEMENT ● Modify Block Diagram ● Modify ITO Layout Guide ● Modify DDRAM Mapping Figure ● Modify Command Sequence for Read/Modify/Write ● Modify OTP Operation Code ● Modify Application Circuit
V0.3b	2013/08/29	● Modify PAD ARRANGEMENT ● Modify PIN DESCRIPTION
V0.4	2013/09/23	● Add DC/Timing TBD Data ● Modify OTP Operation ● Remove 1/5 and 1/7 bias ratio