Ismael Diaz

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Education

Duke University — Durham, NC
B.S.E in Electrical and Computer Engineering and Computer Science — *Aug. 2023 – May 2027*

Experience

Undergraduate Teaching Assistant — Duke University
ECE 250 - Computer Architecture — *Aug. 2024 – Present*
- Led weekly recitations and office hours; graded exams, produced review content, and evaluated TA candidates

ECE 350 - Digital Systems Lab — *Jan. 2025 – Present*
- Leading a weekly lab section

Cyber-Physical Systems Research Assistant — Durham, NC
Duke University — *Aug. 2025 – Present*
- Collecting datasets for a new AR hand-sensing technique
- Comprehensive embedded software development for mmWave radar integration on UAVs

Duke Electric Vehicles (DEV) — Durham, NC
Member — *Aug. 2025 – Present*
- Developed CAN-based C++ telemetry modules for vehicle subsystems
- Designed a 12 to 5V two-layer regulator PCB with EMI and capacitors for noise filtering

Iglesia Bautista Libertad — Houston, TX
Technology Assistant — *May 2023 – Present*
- Maintaining church website, implementing UniFi network with working VLANs, admin for Google and Microsoft workspaces, and project coordinator for the interactive missions display boards

Amazon — Bellevue, WA
Software Development Engineering Intern - Hub Delivery Team — *May 2025 – Aug. 2025*
- Modified backend Java APIs powering internal search tools for store operators
- Designed chaos-testing strategy for a tier-1 service, raising Prime Day readiness score above 70%
- Increased unit test coverage and authored technical documentation

Software Development Engineering Intern - Connected Vehicle Team — *May 2024 – Aug.2024*
- Built four vehicle-centric React dashboards for Amazon's Fleet Edge IoT platform
- Enabled VIN-based views of vehicle location, device health, and time-windowed telemetry
- Integrated telemetry APIs backed by custom AWS infrastructure

Projects

RISC-V Floating-Point Single-Precision Addition Approximation ISA Extension — Oct. 2025 – Dec. 2025
- Designed a custom Verilog IEEE-754–style approximate FP adder
- Evaluated accuracy–performance tradeoffs via gem5 simulations and microbenchmarks

FPGA Vending Machine — Jan. 2025 – May 2025
- Designed a 5-stage pipelined MIPS-like CPU with bypassing, mult/div, and memory-mapped I/O
- Deployed on Nexys A7 FPGA using Verilog, Vivado, and custom assembly programs

Technical Skills

Certifications: Oracle Java SE 8 Certified Associate, Autodesk Fusion 360
Languages: Java, Verilog, C/C++, Python, MIPS Assembly, TypeScript, HTML/CSS, R
Frameworks: ROS2, gem5, React, Node.js, JUnit, WordPress, Joomla!
Developer Tools: Git, Docker, AWS, Vivado, CI/CD, IntelliJ, RStudio, Altium