

Chapter-1

Introduction

■ Traditional VLSI design cycle:

7 steps

- System specification
- Functional architecture design
- Logic design synthesis
- Circuit design
- Physical layout design synthesis
- Fabrication
- Packaging & testing

System specification:

- it is high level representation of the system
- Consider following are considered,
 - performance
 - functionality

- Physical dimensions (size of the die (chip))
- fabrication technology
- design techniques

→ compromise between
 → market requirements
 → technology

= System design

of

- takes system specification
- translates it into a block diagram of the architecture
 - system functional blocks
 - cache memory
 - register
 - arithmetic block
 - logic block.
 - interconnecting data path.

- ability to be able to test it.
- architecture is checked against system specification to ensure all required h/w features & data paths have been included.

Logic design:

→ architectural blocks are expanded

into logic diagrams

→ logic simulation used to

verify that the logic

* logic functions

* perform the task required by the system specification.

Circuit design:

→ logic is translated into circuits

with dimensions assigned to the transistors.

→ → often drawn as stick diagram.

Stick diagram:

pictorial representation of the circuit in terms of the lines

→ connections rewired at each layer of the silicon.

→ circuit simulation

→ verify the design at this level.

→ provide an indication of the power dissipation
★ speed

Geometric layout / Physical layout design:

→ circuits are allocated to positions on the silicon

→ geometric shapes are generated.

for each silicon layer.

Fabrication

→ Layout data is converted into

photo-lithographic marks

for each layer.

* identify the shapes on the wafer

→ Silicon crystals are grown &

(20cm in diameter)

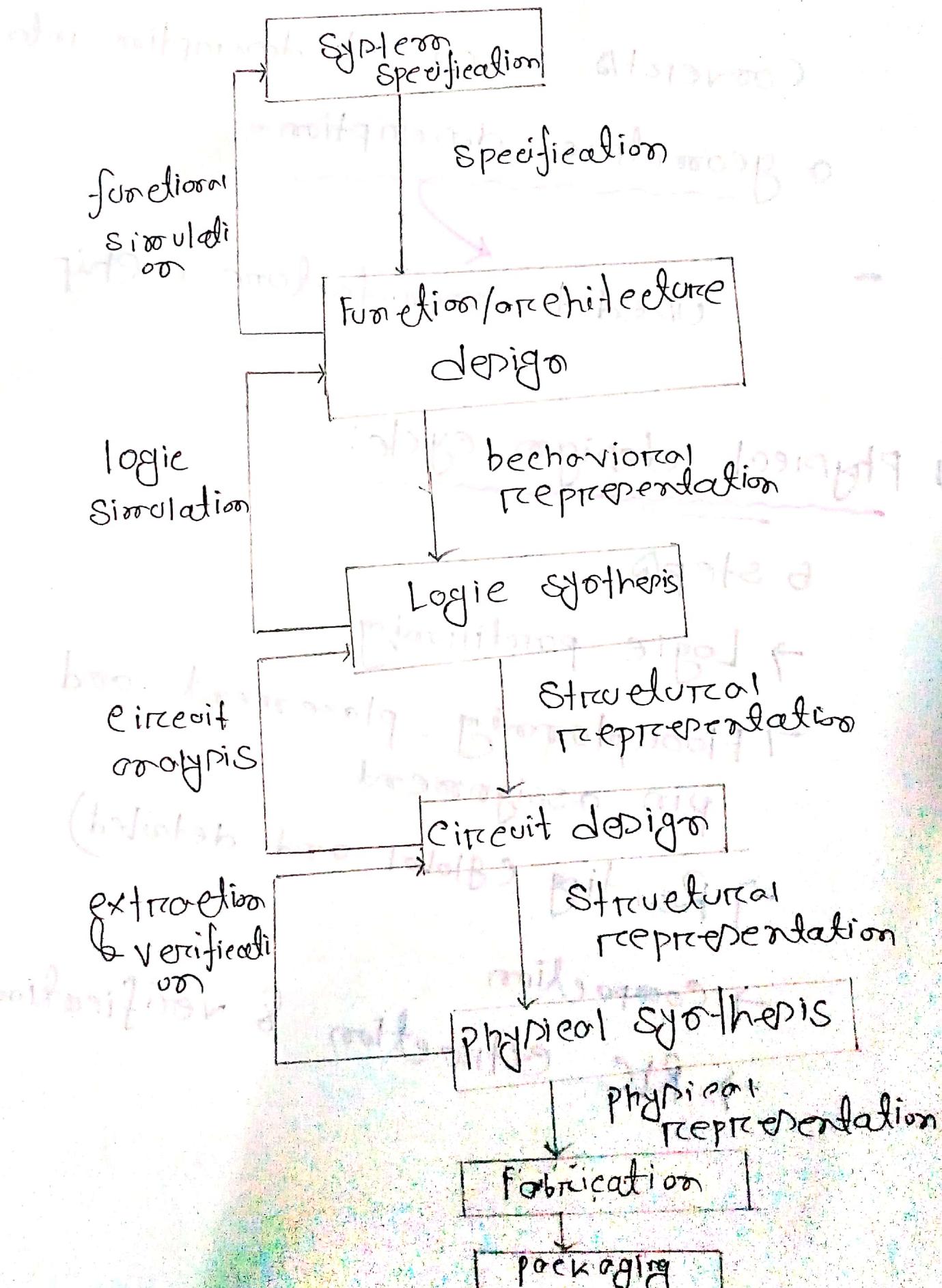
sliced

→ to produce wafers.

→ wafers are used to produce 100 chips.

- Packaging:
- chip used in printed circuit boards (PCB)
 - " " " multi-chip-modules (MCM)
 - Dual in line package
 - Dual Grid Array
 - Ball " "
 - Quad flat package

Traditional VLSI Design Flow



Physical Design:

- Converts a circuit description into a geometric description
- Used to manufacture a chip

Physical design cycle:

5 steps

→ Logic partitioning

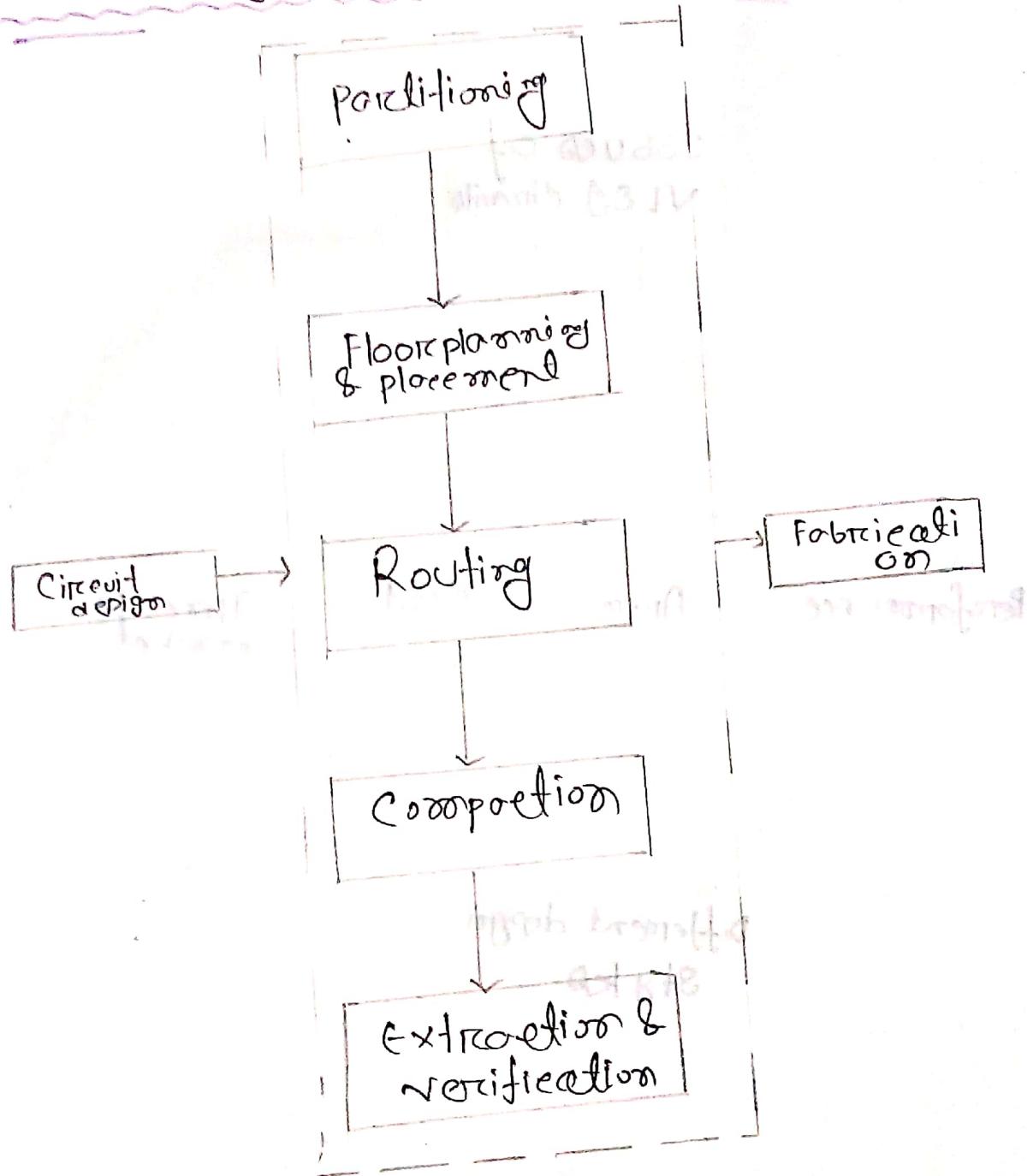
→ Floorplanning - placement and pin assignment

→ Routing (global and detailed)

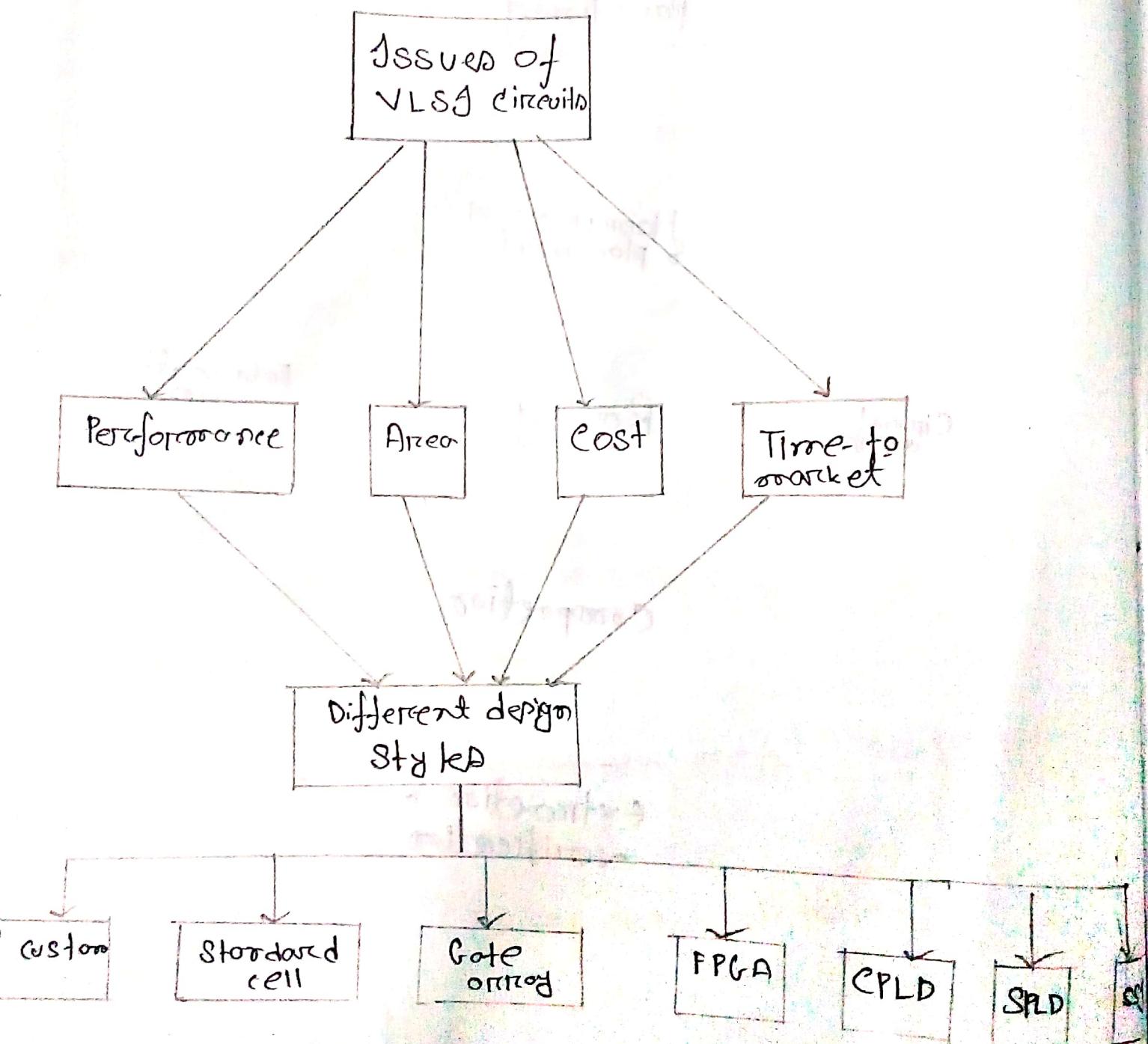
→ Compression

→ RLC extraction & verification.

Physical Design Flow:



Issues of VLSI circuit design:



performance, Area efficiency, Cost,
Flexibility

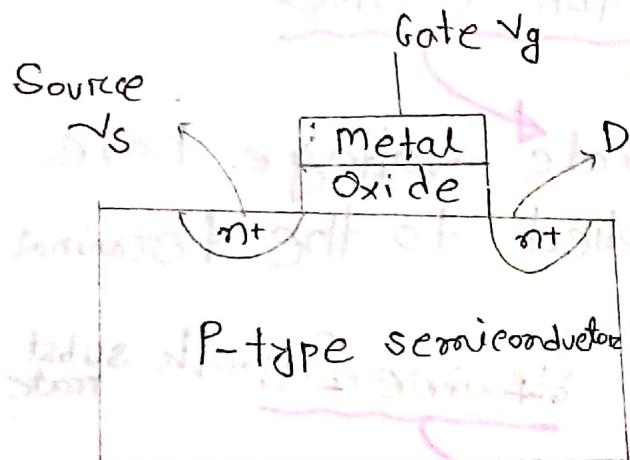
Chapter-2

MOS Devices and Basic Circuits

Structure of NMOS:

→ basis of the transistor is metal-oxide - semiconductor, hence MOS

→ device input: gate



→ this was a metal plate.

→ oxide is very pure silicon dioxide

separates the gate

Semiconductor material consists of get as an insulator

→ lightly doped p-type substrate

→ heavily " n-type regions "

→ device output: drain

→ terminal that is common to both the input and output circuit.
→ source

→ input voltage $v_{gs} = v_g - v_s$

→ output $v_{ds} = v_d - v_s$

■ Conduction of NMOS

→ to make the transistor conduct

appropriate voltage have to be applied to the terminal

→ v_g is applied to source & bulk

→ positive bias to the gate and drain

Although the conductivity of semiconductor is less than that of the metal, it can be considered to be a conducting material.

So oxide acts as an insulator between two conductors.

There is now a continuous electron channel from the drain to source

and the current flows

if there is a bias between them.

Current flows from drain to the

source

as the drain potential is higher than that of the source.

A region depleted of free charge

carriers

→ separates all p-type region from n-type

→ prevents conduction of reverse-biased on transition

Threshold voltage:

The input potential V_{GS} at which the surface just becomes inverted called threshold voltage (V_t)

$\rightarrow < V_t$ (NMOS is off)

$\rightarrow > V_t$ (inversion channel is established, device conducts)

Body effect:

Threshold one rooted for transistors assuming source-substrate voltage of 0V.

Changing the substrate voltage causes the threshold voltage to change.

Known as body effect.

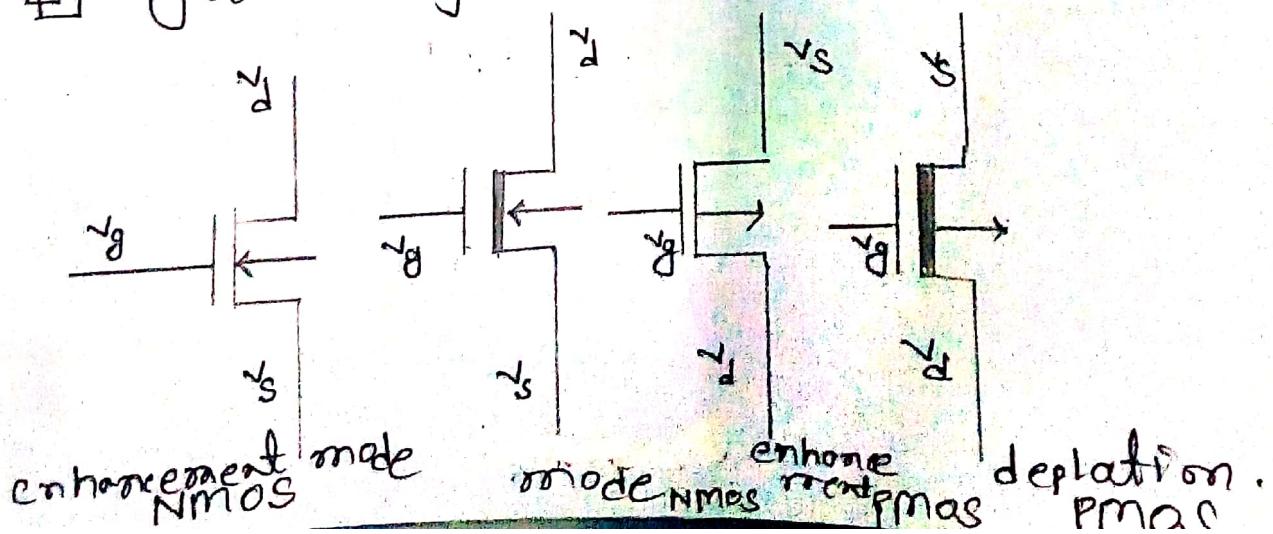
$$V_t = V_{t0} + \gamma (V_{SB})^{1/2}$$

→ constant
→ 0.3-0.7
→ generally 0.5

→ threshold voltage when $V_{SB}=0$

modified threshold voltage

Symbol of MOS transistors:



Mode of Transistor

→ NM → enhancement mode

→ depletion "

State of NMOS device

2 state

→ $V_{GS} < V_T$ { Transistor is off
no current flow

→ $V_{GS} > V_T$ { Transistor is on

{ drain to

source for off

Characteristic equation of NMOS

OTC For a constant V_{GS} , I_{DS} increases with an increase in V_{DS} :

There are an infinite number

of capacitances \rightarrow between drain & source.

Total charge induced in the channel
is the sum of the charge"

\rightarrow on each of
the capacitance

Now, $d\lambda$ = length of one of these capacitance

w = channel width

L = " length.

D = thickness of the oxide

\therefore capacitance, $C = \frac{w \epsilon d \lambda}{D}$

ϵ = permittivity of the insulator

The voltage v in excess of v_t

$$v = (v_{gd} + \frac{\kappa}{L} v_{ds} - v_t)$$

$$= (v_{gs} - v_{ds} + \frac{\kappa}{L} v_{ds} - v_t)$$

$$v_{ds} = v_d - v_s$$

$$= v_{dg} + v_{gs}$$

$$= v_{ds} - v_{gd}$$

$$\therefore v_{gd} = v_{gs} - v_{ds}$$

\therefore Charge q induced on
this capacitor

$$q = C v \\ = \frac{\omega \epsilon d k}{D} (v_{gs} - v_{ds} + \frac{\kappa}{L} v_{ds} - v_t)$$

\therefore Total charge Q induced in the channel,

$$Q = \int_0^L \frac{\epsilon \omega}{D} (v_{gs} - v_{ds} + \frac{\kappa}{L} v_{ds} - v_t) dk \\ = \left[\frac{\epsilon \omega L}{D} \left((v_{gs} - v_t) - \frac{v_{ds}}{2} \right) \right]$$

$$\text{Now } Q = t \int ds$$

$$t = \frac{\text{channel length } L}{\text{electron velocity}}$$

$$\text{electric velocity} = \frac{N_n v_{ds}}{\text{electron mobility}}$$

where, N_n = electron velocity per unit electric field. (metre²/volt-second)

$$J_{ds} = \frac{Q}{A}$$

$$= \frac{e \omega L}{D} \left[(v_{gs} - v_t) - \frac{v_{ds}}{2} \right]$$

$$\left(\frac{L}{\frac{N_n v_{ds}}{L}} \right)$$

$$= \frac{e \omega L}{D} \frac{N_n v_{ds}}{L^2} \left[(v_{gs} - v_t) - \frac{v_{ds}}{2} \right]$$

$$J_{ds} = \frac{e \omega N_n}{DL} \left[(v_{gs} - v_t) v_{ds} - \frac{v_{ds}^2}{2} \right]$$

Again, $v_{ds} \ll v_{gs} - v_t$

$$\therefore J_{ds} = \frac{e \omega N_n}{DL} [(v_{gs} - v_t) v_{ds}]$$

Characteristic I_D (NMOS)

Resistive region.

$$I_{DS} = \frac{CWL_n}{DL} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Saturation region.

$$V_{DS} \approx V_{GS} - V_t$$

At pinch-off point,

$$V_{DS} = V_{GS} - V_t$$

Above Above pinch-off voltage between source & end of the inversion channel is constant

at $V_{GS} - V_t$

$$I_{DS} = \frac{CWL_n}{2DL} (V_{GS} - V_t)^2$$

Characteristic equation (PMOS)

Resistive region:

In the resistive region $V_{SD} < V_{SG} - V_t$

$$I_{SD} = \frac{E \mu_p w}{DL} [(V_{SG} - V_t) V_{SD} - \frac{V_{SD}^2}{2}]$$

Saturated region

Pinch-off occurs $V_{SD} = V_{SG} - V_t$

and for $V_{SD} > V_{SG} - V_t$ the device is saturated

$$I_{SD} = \frac{E \mu_p w}{2DL} (V_{SG} - V_t)^2$$

Hole mobility: p_h, hole velocity per unit

electric field.

μ_h is two to three times less than μ_n

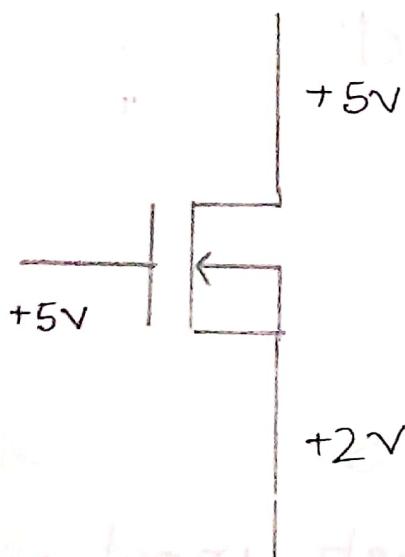
NB: Nmos transistors will conduct more current than a Pmos device of smaller size.

→ current flow is proportional to the carrier mobility.

Principles of Inverters

- It has a digital switch
- Switch is closed if a high input voltage is applied
- Switch is opened if a low voltage is applied
- Switch output is connected via a load
 - to the power rail
- n-channel enhancement transistor used as the digital switch

→ load can be implemented by the use of an mos device



Given that,

$$\frac{eN_A}{D} = 30 \text{ NA/V}^2$$

$$w:L = 1:1$$

$$V_{to} = 1 \text{ V}$$

$$\gamma = 0.5$$

$$V_t = V_{to} + \gamma \cdot \theta (V_{sb})^{1/2}$$

$$= 1 + 0.5(0)^{1/2}$$

$$= 1$$

$$\therefore V_{gs} = (5-2) \text{ V}$$

$$V_{gs} > V_t$$

∴ Transistor is on.

$$V_g = +5 \text{ V}$$

$$V_d = +5 \text{ V}$$

$$V_s = +2 \text{ V}$$

$$V_{ds} = -3(5-2) \text{ V}$$

$$= 3 \text{ V}$$

$$V_{gs} - V_t = 3 - 1 \text{ V}$$

$$= 2 \text{ V}$$

$$V_{ds} > V_{gs} - V_t$$

∴ Transistor is at saturated region.

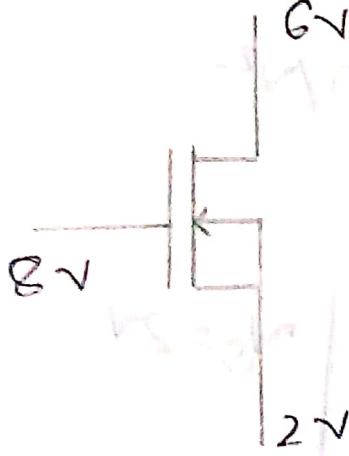
$$\therefore I_{DS} = \frac{e \mu_n \omega}{2DL} (v_{GS} - v_t)^2$$

$$= \frac{30}{2} (3-1)^2$$

$$= 15(2)^2$$

$$= 15 \times 4$$

$$= 60 \text{ mA}$$



Given that

$$\omega : L = 1 : 1$$

$$\frac{e \mu_n}{D} = 30 \text{ PA/V}^2$$

$$v_{th} = 1V$$

$$\therefore v_g = 8V \quad \therefore v_{GS} = v_g - v_s = (8-2)V = 6V$$

$$v_d = GV$$

$$v_s = 2V$$

$$v_{DS} = (G-2)V = 4V$$

$$v_{GS} > v_{th}$$

$v_{GS} - v_{th} = (6-1)V = 5V$

$$v_{DS} < v_{GS} - v_t$$

\therefore Transistor is in active region.

$$\therefore I_{DS} = \frac{e \mu_n \omega}{DL} [(v_{GS} - v_t) \cdot v_{DS} - \frac{v_{DS}^2}{2}]$$

$$= 30 \left[(C_6 - 1) \cdot 4 - \frac{4^2}{2} \right]$$

$$= 30 \left[35 \cdot 4 - 16/2 \right]$$

$$= 30 (100 - 8)$$

$$= 30 \times 92$$

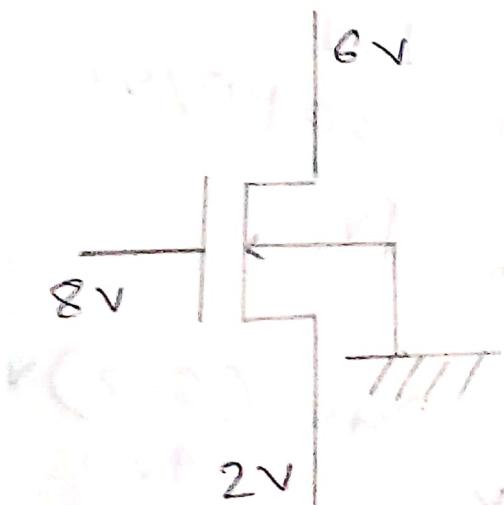
$$= 30 \times 12$$

$$= 360 \text{ PA}$$

Ans



Given that,



$$\frac{eN\alpha}{D} = 30 \mu\text{A}/\text{V}^2$$

$$\omega : L = 1$$

$$V_{t0} = 1V \quad | \quad V_S = 2V$$

$$V_g = 8V$$

$$V_D = 6V$$

$$V_t = V_{t0} + \gamma (V_{Sb})^{1/2}$$

$$= 1 + 0.5(2)$$

$$= 1 + 0.707$$

$$= 1.71$$

$$V_{GS} = V_g - V_S$$

$$= (8 - 2)V$$

$$= 6V$$

$$V_{GS} > V_t$$

∴ Transistor is on.

$$V_{GS} - V_t = 6 - 1.7 \\ = 4.2 \text{ V}$$

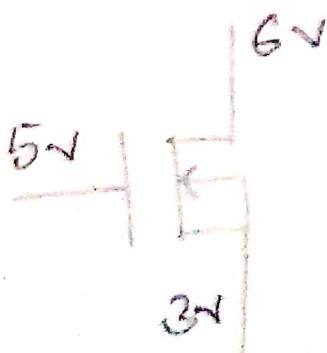
$$V_{DS} = V_D - V_S \\ = (6 - 2) \text{ V} \\ = 4 \text{ V}$$

$V_{DS} < V_{GS} - V_t$

\therefore Transistor is at resistive region.

$$\begin{aligned} I_{DS} &= \frac{EN_n w}{DL} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right] \\ &= 30 \left\{ (6 - 1.7) 4 - \frac{4^2}{2} \right\} \\ &= 30 (17.16 - 8) \\ &= 274.8 \text{ mA} \end{aligned}$$

Ans



Given that,

$$V_g = 6 \text{ V} \quad V_{th} = 3 \text{ V}$$

$$V_d = 6 \text{ V}$$

$$V_S = 3 \text{ V}$$

$$\frac{EN_n}{D} = 30 \text{ mA/V}^2$$

$$\omega : L = 1 : 1$$

$$\begin{aligned} V_{GS} &= V_g - V_S \\ &= (6 - 3) \text{ V} \\ &= 3 \text{ V} \end{aligned}$$

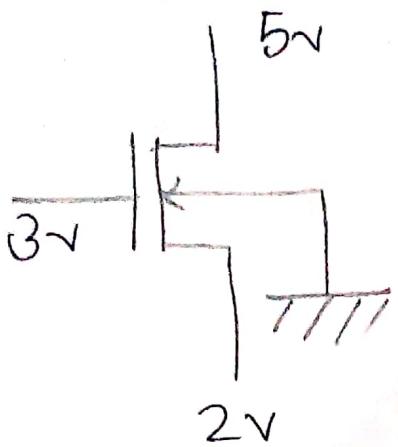
$$V_{GS} > V_{th}$$

$$\therefore I_{DS} = 0$$

Ans

\therefore Transistor is off.

Q



Given that,

$$\frac{EI_{DN}}{D} = 30 \text{ mA/V}^2$$

$$\omega : L = 1 : 1$$

$$V_{f0} = 1V$$

$$\gamma = 0.5$$

$$V_{GS} = (3 - 2)V$$

$$= 1V$$

$$V_{DS} = (5 - 2)V$$

$$= 3V$$

$$V_f = V_{f0} + \gamma (V_{DS})^{\frac{1}{2}}$$

$$= 1 + 0.5 (2)^{\frac{1}{2}}$$

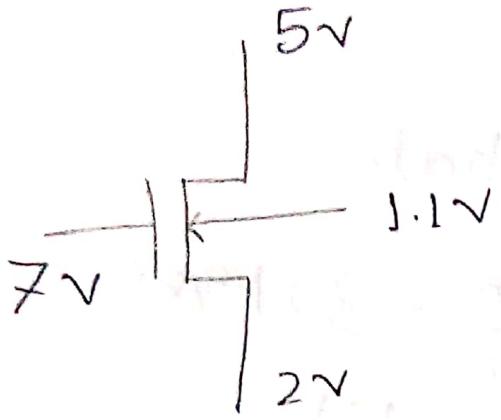
$$= 1 + 0.707$$

$$= 1.707$$

$$V_{GS} > V_f$$

∴ Transistor is off

$$\therefore I_{DS} = 0 \text{ Am}$$



Given that,

$$\frac{EN_A}{D} = 30 \text{ mA/V}^2$$

$$W:L = 1:1$$

$$V_0 = 1V$$

$$\gamma = 0.5$$

$$\begin{aligned} \therefore V_{GS} &= (V_g - V_s) \\ &= (7 - 2)V \\ &= 5V \end{aligned}$$

$$\begin{aligned} V_{DS} &= (5 - 2)V \\ &= 3V \end{aligned}$$

$$\begin{aligned} V_f &= V_0 + \gamma (V_{SB})^{\frac{1}{2}} \\ &= 1 + 0.5(2 - 1)^{\frac{1}{2}} \\ &= 1 + 0.5(0.9)^{\frac{1}{2}} \\ &= 1 + 0.474 \\ &= 1.474 \end{aligned}$$

$$\therefore V_{GS} > V_f$$

$V_{GS} > V_f$
∴ Transistor is on.

$$V_{DS} = V_{GS} - V_f = (5 - 1.474)V$$

$$= 3.526V$$

$$V_{DS} < V_{GS} - V_f$$

∴ Transistor is at resistive region.

$$I_{DS} = \frac{EN_A W}{DL} \left[(V_{GS} - V_f) V_{DS} - \frac{V_{DS}}{2} \right]$$

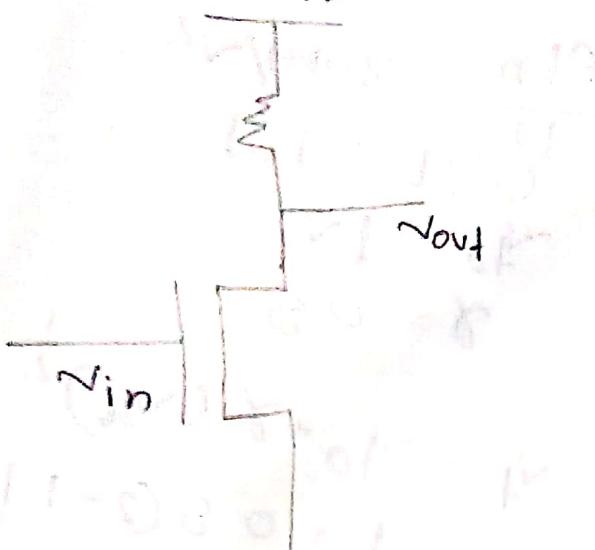
$$= 30 \left\{ (5 - 1.474) 3 - \frac{3^2}{2} \right\}$$

$$= 30 \left\{ 10.578 - 9/2 \right\}$$

$$= 162.34 \text{ PA} \quad \underline{\text{Ans}}$$

H

$$V_{DD} = +5V$$



Given that

$$\frac{EN_n}{D} = 30 \text{ NA/V}^2$$

$$W:L = 1:1$$

$$V_{th} = 1V$$

$$\begin{aligned} V_{out} &= 0.3V_{th} \\ &= (0.3 \times 1)V \\ &= 0.3V \end{aligned}$$

Now,

$$V_{GS} = V_{in} = 5V$$

$$V_{out} = V_{DS} = 0.3V$$

$\emptyset V_{GS} > V_{th}$

\therefore trcompistor is on.

$$\begin{aligned} V_{GS} - V_t &= (5 - 1)V \\ &= 4V \end{aligned}$$

$$V_{DS} = 0.3V$$

$V_{DS} < V_{GS} - V_t$

\therefore trcompistor is at resistive region.

$$I_{DS} = \frac{EN_n \omega}{DL} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$= 30 \left\{ (5-1) 0.3 - \frac{0.3^2}{2} \right\}$$

$$= 30(1.2 - 0.095)$$

$$= 30 \times 1.155$$

$$= 34.65 \text{ A}$$

Am

$$R = \frac{V_{DD} - V_{out}}{I_{ds}}$$

$$= \frac{5 - 0.3}{34.65 \times 10^{-6}}$$

$$= \frac{4.7}{34.65 \times 10^{-6}}$$

$$= 1.357 \times 10^5 \text{ } \Omega \text{ } \text{sr}$$

$$= 1.357 \times 10^2 \times 10^3 \text{ } \Omega \text{ } \text{sr}$$

$$= 135.7 \times 10^3 \text{ } \Omega \text{ } \text{sr}$$

$$= 135.7 \text{ K } \text{sr}$$

Ans

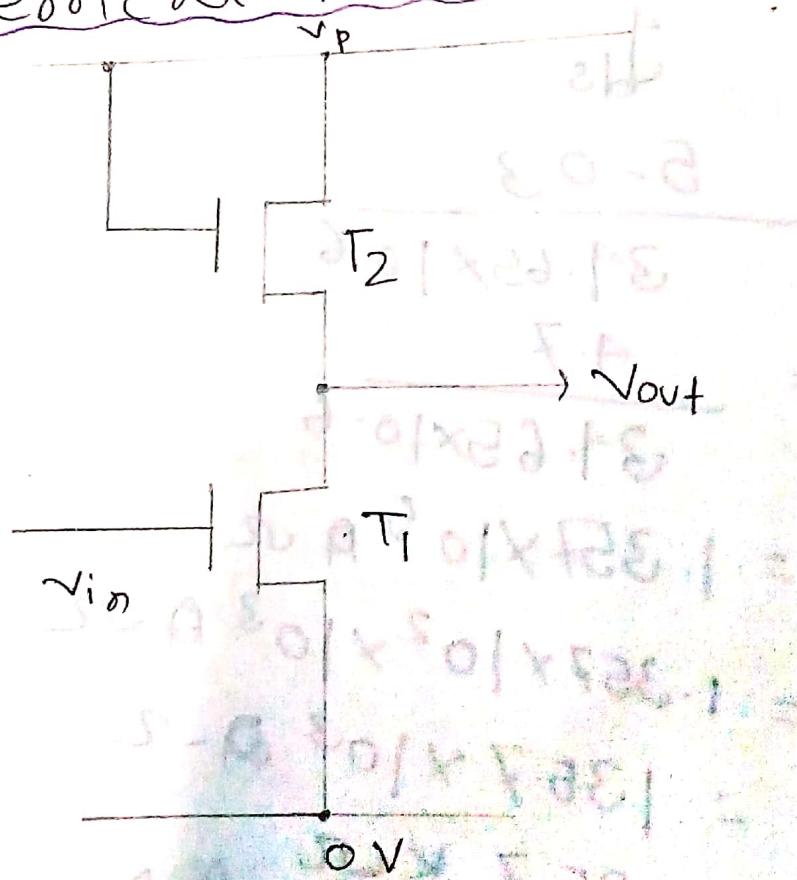
■ A speed ratio:

width to length ratio

of the transistor.

$$\text{Aspect ratio} = W/L$$

■ NMOS Inverter with on Nmos
Enhancement Transistor Load:



→ T_1 act as a switch / driver

→ T_2 " " a load

→ T_2 gate is connected to V_P
to maximize its V_{GS}

→ When V_{in} is low T_1 is off

$$\rightarrow V_{in} = V_{BS} < V_{te}$$

→ some very small leakage current flows

→ through T_1 supplied by T_2

$$V_{out} = V_p - V_{te}$$

Given that, $V_p = 5V$

$$V_p = 5V$$

$$V_{le} = 1V$$

$$V_{out} = V_p - V_{le}$$

$$V_{out} = 5 - 1 = 4V \quad \text{if body effect is neglected.}$$

$$V_{out} = V_p - V_{le}$$

$$= V_p - [V_{le0} + \beta(V_{SB})^{\frac{1}{2}}]$$

$$= 5 - [1 + 0.5(V_{out})^{\frac{1}{2}}]$$

$$= 5 - 1 - 0.5(V_{out})^{\frac{1}{2}}$$

$$\Rightarrow n = 4 - 0.5n^{\frac{1}{2}} \quad [\text{Let } V_{out} = n]$$

$$\Rightarrow (0.5n^{\frac{1}{2}})^2 = (4-n)^2$$

$$\Rightarrow 0.25n = 16 - 8n + n^2$$

$$\Rightarrow 0.25n - n^2 = 16$$

$$\Rightarrow 0.25n - 8.25 + 16 = 0$$

$$n = 3.12$$

$$\therefore V_{out} = 3.12$$

$$\text{For T}_1, \quad V_{in} = V_{GS} = 3.12V$$

$$V_{out} = 0.3V = V_{DS}$$

$$V_{GS} - V_{TE} = (3.12 - 1)V$$

$$= 2.12V$$

$$V_{GS} > V_{TE}$$

$$V_{DS} < V_{GS} - V_{TE}$$

\therefore transistor is in triode region

\therefore transistor T_1 is in resistive region.

$$\begin{aligned} I_{DS} &= \frac{eN_n w}{2DL} \left[(V_{GS} - V_{TE}) V_{DS} - \frac{V_{DS}^2}{2} \right] \\ &= 30 \left[(3.12 - 1) 0.3 - \frac{0.3^2}{2} \right] \frac{w_1}{L_1} \\ &= 30 \left[(2.12)(0.3) - 0.045 \right] \frac{w_1}{L_1} \\ &= 17.73 \frac{w_1}{L_1} \text{ NA} \end{aligned}$$

T_2 is on and $V_{DS} = V_{GS}$

$$V_{DS} > V_{GS} - V_{TE}$$

$\therefore T_2$ is in saturated region.

$$\therefore I_{DS} = \frac{eN_n w_2}{2DL_2} (V_{GS} - V_{TE})^2$$

$$= \frac{30}{2} (4.7 - 1)^2 \frac{w_2}{L_2}$$

$$= 205.35 \frac{w_2}{L_2} \text{ NA}$$

inverted ratio, $k = \frac{\omega_1/L_1}{\omega_2/L_2}$

$$k = \frac{\frac{1}{17.73}}{\frac{1}{205.35}}$$

$$= \frac{1}{17.73} \times 205.35$$

$$= 11.6$$

Ans

For convenience $k = 11.6 \approx 12$

$$\therefore k = \frac{\omega_1/L_1}{\omega_2/L_2} = \frac{3/1}{1/4}$$

$$= \frac{3}{1}$$

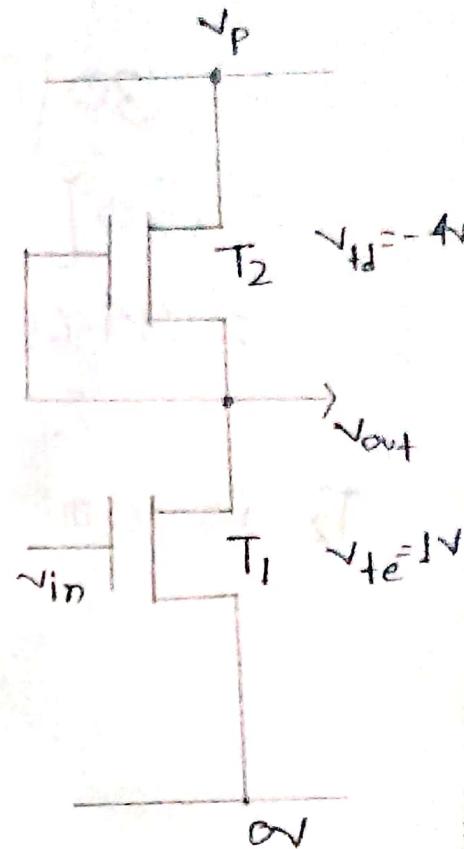
Q. $\therefore \omega_1/L_1 = 3/1$

$$\omega_2/L_2 = 1/4$$

Ans

■ NMOS Inverter with an NMOS Depletion Tristor Load.

- V_{td} of T_2 is negative
- V_{gs} of T_2 is 0
- T_2 is already on



when V_{in} is low

$$V_{gs} = V_{in} < V_{te}$$

$\therefore T_1$ is off.

T_2 is on, so and supplies the very small leakage current of T_1 .
High level input voltage to a gate is therefore V_p .

$$\text{Now, } \frac{E_N}{D} = 30 \text{ NA/V}^2$$

$$V_{ds} = 0.3 \times 1 = 0.3V$$

$$V_{gs} = 5V$$

$$V_{gs} - V_{te} = 4V$$

$$V_{out} = 0.3 V_{te} = 0 V_{ds} \quad \therefore V_{ds} < V_{gs} - V_{te}$$

$$V_{te} = 1V$$

∴ Transistor is on

$$V_{gs} > V_{te}$$

Transistor is on

Resistive
Region.

$$\begin{aligned}
 J_{ds} &= \frac{EN_n C_0}{PL_1} \left[(V_{gs} - V_{le}) V_{ds} - \frac{V_{ds}}{2} \right] \\
 &= 30 \left[(5 - 1) \cdot 0.3 - \frac{0.32}{2} \right] \frac{\omega_1}{L_1} \\
 &= 30 \left[(4 \times 0.3) - 0.095 \right] \frac{\omega_1}{L_1} \\
 &= 34.65 \left(\frac{\omega_1}{L_1} \right) \mu A
 \end{aligned}$$

T_2 is on with $V_{gs} = 0V$

$$\begin{aligned}
 V_{ds} &= V_p - V_{out} \\
 &= (5 - 0.3) \\
 &= 4.7V
 \end{aligned}$$

$$V_{ds} > V_{gs} - V_{td}$$

\therefore Transistor is on saturated region.

$$J_{ds} = \frac{EN_n C_0}{2PL_2} (V_{gs} - V_{td})^2$$

$$= \frac{25}{2} \cdot (0 - (-4))^2 \frac{\omega_2}{L_2}$$

$$= 25/2 \times 16 \frac{\omega_2}{L_2} \mu A$$

$$= 200 \frac{\omega_2}{L_2} \mu A$$

$$\begin{aligned}
 \text{Invertor ratio, } K &= \frac{\left(\frac{\omega_1}{L_1} \right)}{\left(\frac{\omega_2}{L_2} \right)} \\
 &= \frac{34.65}{200} = 0.173
 \end{aligned}$$

□ Edge Times for NMOS Inverter with a Depletion Load:

maximum I_{ds} of T_1

$$= \frac{30}{2}$$

$$= \frac{\epsilon N_n \omega_1}{2 D L_1} (V_{gs} - V_{te})^2$$

$$= \frac{30}{2} \left(\frac{\omega_1}{L_1}\right) (5-1)^2$$

$$= 240 \frac{\omega_1}{L_1} \mu A$$

maximum I_{ds} of T_2 ,

$$= \frac{\epsilon N_n \omega_2}{2 D L_2} (V_{gs} - V_{te})^2$$

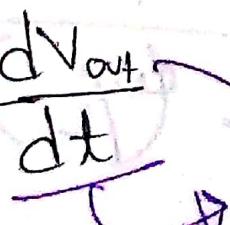
$$= \frac{25}{2} \left(\frac{\omega_2}{L_2}\right) (5-1)^2$$

$$= 200 \frac{\omega_2}{L_2} \mu A$$

$$\frac{\text{maximum } I_{ds} \text{ of } T_1}{\text{maximum } I_{ds} \text{ of } T_2} = \frac{240 \frac{\omega_1}{L_1}}{200 \frac{\omega_2}{L_2}}$$

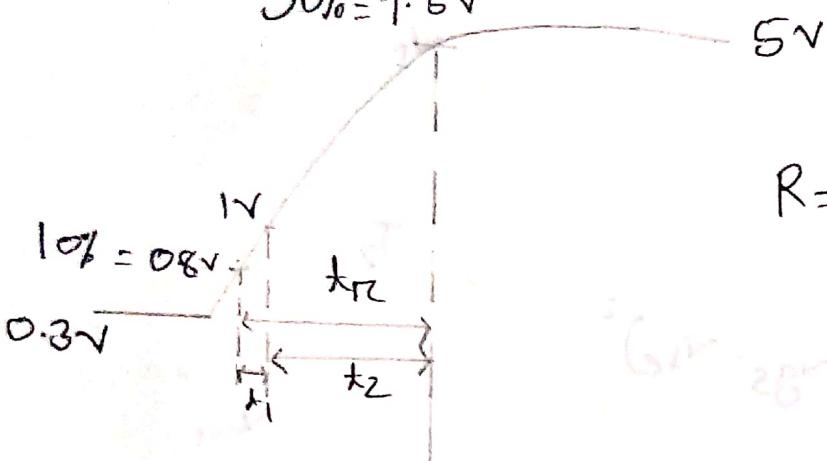
$$= \frac{6K}{5}$$

$$J_C = C_{out} \frac{dV_{out}}{dt}$$

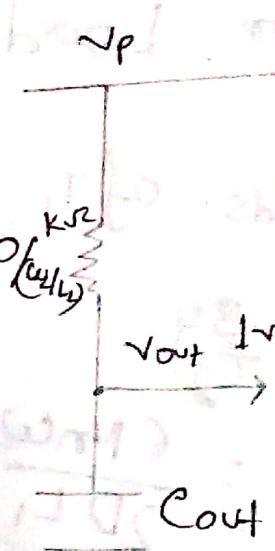


Change in voltage
Change in time

$$90\% = 9.5V$$



$$R = 20 \frac{K\Omega}{A_{OL}}$$



$t_R = t_1 + t_2 \rightarrow T_2$ is in saturated mode

t_1 = time for the output
to rise from $0.8V$ to $1V$

t_2 = time for the output to
rise from $1V$ to $9.5V$

$\rightarrow T_2$ is in resistive mode.

$$R = \frac{\text{Pinch off voltage}}{\text{Pinch-off current}}$$

$$= -\frac{E_{PN}}{2D} \left(\frac{V_{GS} - V_T}{L} \right) (V_{GS} - V_T)^2$$

$$= \frac{1}{\frac{25}{2} \left(\omega_2 / L_2 \right) (50 - (-1))}$$

$$= \frac{1}{50 \frac{\omega_2}{L_2}} \text{ mVR}$$

$$= \frac{1000 \times 10^3}{50 \frac{\omega_2}{L_2}} \times 10^3 \text{ VR}$$

$$= \frac{20}{\omega_2 / L_2} \times 10^3 \text{ VR} = \frac{20}{\omega_2 / L_2} \text{ kVR}$$

$$V_{out} = V_p - (V_p - V_i) e^{(-t_2 / RC_{out})}$$

$$4.5 = 5 - (5-1) e^{(-t_2 / RC_{out})}$$

$$= 7 e^{-t_2 / RC_{out}} = \frac{(5 - 4.5)}{(5-1)}$$

$$= 7 e^{-t_2 / RC_{out}} = \frac{0.5}{4} = 0.125$$

$$\Rightarrow -t_2 / RC_{out} = -2.079$$

$$\Rightarrow t_2 / RC_{out} = 2.079$$

$$t_2 = 2.079 RC_{out}$$

$$t_{R2} = t_2 = 2.08 R_{e04}$$

$$= 2.08 \frac{20}{\omega_2/L_2} R_{e04} C_{out}$$

$$\therefore t_{R2} = 92 C_{out} \frac{ns}{(\omega_2/L_2)}$$

$$t_{R2} = \frac{6K}{5} t_f$$

$$\Rightarrow t_f = t_{R2} \frac{5}{6K}$$

$$= \frac{(92)(C_{out})}{(\omega_2/L_2)(6)(\omega_1/L_1)} (5)$$

$$\therefore t_f = \frac{35 C_{out}}{\omega_1/L_1} ns$$

Expression for the rise time is
not so accurate

→ as the body effect is significant
for T_2 .

$$\therefore t_{R2} = \frac{60 C_{out}}{\omega_2/L_2} ns$$

Ratioed design:

It is necessary to choose suitable gate geometry ratios for both the load and drive transistors in order to obtain desired output. This is called ratioed design.

Importance of (ω/L) ratio of transistors:

→ determines the circuit speed
→ "switching time"
edge time $\propto \frac{1}{\text{aspect ratio}}$
current flow $\propto \text{aspect ratio}$

Half-bridge

→ implemented by the inverter load

with digital switch:

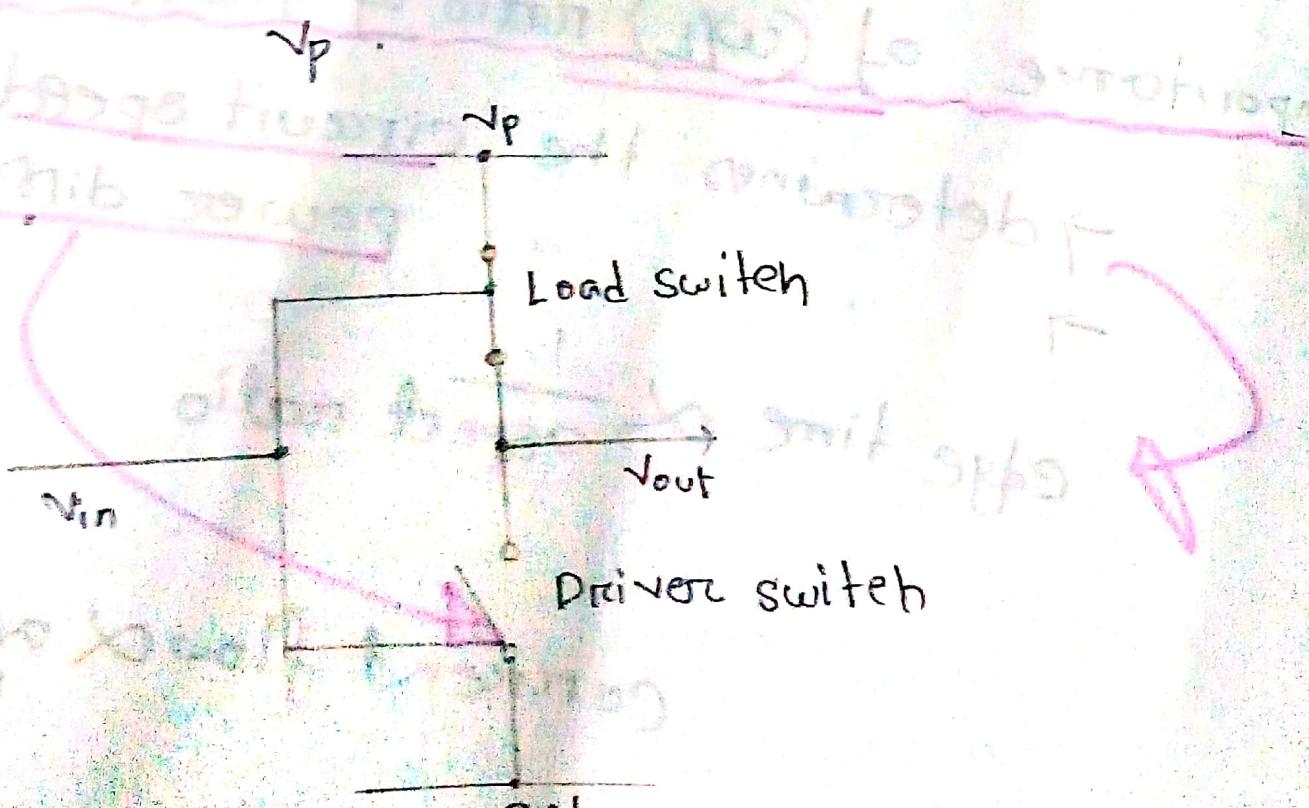
→ load switch & driver switch

one never simultaneously closed

→ load and driver switch

operate in antiphase

→ no current flow between load



→ at high input → driver switch closed
at low input → load switch closed

CMOS inverter:

driver switch (T1)

→ n-channel enhancement switch

→ substrate is connected to ON

→ threshold V_{te} = minimum gate-source voltage.

load switch (T2)

→ p-channel enhancement switch

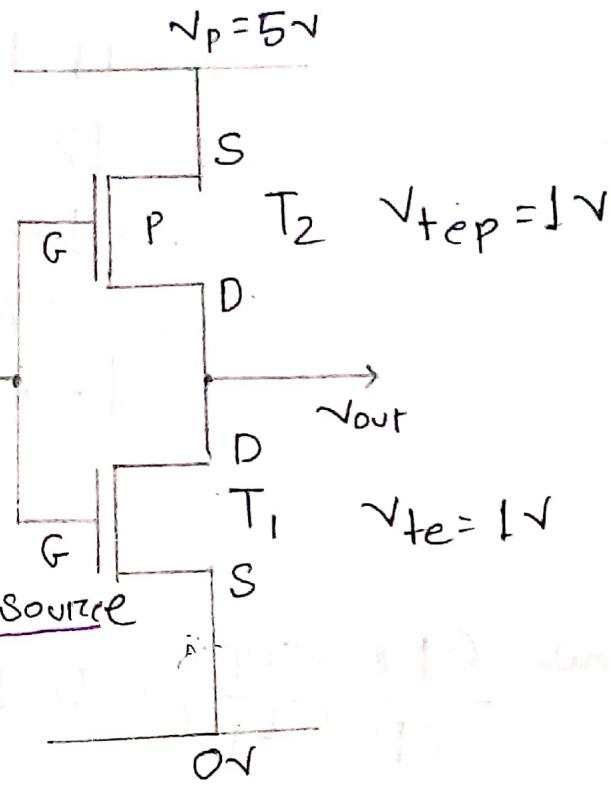
→ substrate is connected to N_p

→ threshold V_{tsp} = minimum source-gate voltage

→ V_{in} changes from low to high

→ T1 turns on
→ T2 turns off

→ load capacitor of the output discharges from $5V$ to $0V$.



→ Vin changes from high to low

→ T1 turns off

→ T2 turns on

→ load capacitor

on the output charges

from $0 \approx 105V$.

Now $\frac{\epsilon_{pn}}{2D} \left(\frac{\omega_1}{L_1}\right) (5-1)^2 = \frac{\epsilon_{pp}}{2D} \left(\frac{\omega_2}{L_2}\right) (5-1)^2$

$$\Rightarrow \frac{\omega_1/L_1}{\omega_2/L_2} = \frac{N_p/N_n}{2}$$

$$\Rightarrow \frac{\omega_1}{\omega_2} = \frac{\frac{1}{2} N_p}{N_n} = \frac{1}{2} [C \cdot N_p - \frac{1}{2} N_p^2]$$

$$\therefore \frac{\omega_2}{L_2} = 2 \left(\frac{\omega_1}{L_1} \right)$$

$$\therefore \frac{\omega_1}{L_1} = 1:1$$

$$\therefore \frac{\omega_2}{L_2} = 2:1$$

* edge time in CMOS approximated
of the falling edge time

for NMOS

lowered with a depletion load.

$$t_r = t_f = \frac{35 C_{out}}{(C_1(L_1))} \text{ ns}$$

where, C_{out} = output of load capacitance.

T₁ Transistor of CMOS

$$C_1/L_1 = 1/1$$

$$\epsilon_{Hn/D} = 30 \text{ nA/V}^2$$

$$V_{te} = 1 \text{ V}$$

$$\rightarrow \text{Saturation } I_{ds} = \epsilon_{Hn}/2D^2(C_{gs} - V_{te})^2 NA$$

$$= \frac{30}{2} (C_{gs} - 1)^2 \text{ nA}$$

$$= 15 (C_{gs} - 1)^2 \text{ nA}$$

\rightarrow pinch-off occurs when, $V_{ds} = V_{gs} - 1$

$$\therefore V_{in} = V_{gs}$$

$$V_{out} = V_{ds}$$

$$I = I_{ds}$$

T2 transistor of emos:

$$w_2/l_2 = 2/1$$

$$ENP/D = 15 \text{ nm/V}^2$$

$$V_{tp} = 1 \text{ V}$$

$$\rightarrow \text{saturation } I_{sd} = \frac{ENP}{2D} \frac{w_2}{l_2} (V_{sg} - V_{tp})^2 NA$$
$$= \frac{15}{2} \left(\frac{2}{1}\right) (V_{sg} - 1)^2 NA$$
$$= 15 (V_{sg} - 1)^2 NA$$

\rightarrow pinch-off occurs when

$$V_{sd} = V_{sg} - 1$$

$$V_{in} = 5 - V_{sg}$$

$$V_{out} = 5 - V_{sd}$$

$$I = I_{sd}$$

2018 - 3(b)

For trionistor L

i) pinch off occurs voltage $V_{ds} = V_{gs} = 1 \text{ V}$

$$V_{gs} = (2.1 - 1) \text{ V}$$

$$= (1.1) \text{ V}$$

ii) input voltage $V_{in} = V_{gs} = 2.1 \text{ V}$

$$= \underline{\text{Am}}$$

iii) Output voltage $V_{out} = V_{ds} = 1.1 \text{ V}$ I from

iv) Saturation currents $I = I_{ds} = \frac{eN_A}{2D} \left(\frac{V_D}{V_D - V_s} \right)^{1/2}$

Now, $\frac{eN_A}{D} = 3 \times 10^{-8} \text{ mA/V}^2$

$$= \frac{3 \times 10^{-8}}{10^{-6}} \text{ mA/V}^2$$

$$= 3 \times 10^{-2} \text{ mA/V}^2$$

$$= \frac{3 \times 10^{-2}}{10^3} \text{ mA/V}^2$$

$$= 3 \times 10^{-5} \text{ A/V}^2 = \frac{3 \times 10^{-5}}{10^{-6}} \text{ Nm/V}^2$$

$$\begin{aligned}
 \therefore I_{ds} &= \frac{3 \times 10^{-5}}{2} (1/1)(2 \cdot 1 - 1)^2 \\
 &= 1.5 \times 10^{-5} (1 \cdot 1)^2 \\
 &= 1.815 \times 10^{-5} A \\
 &= \underline{0.1815} \\
 &= 18.15 \times 10^{-6} \times 10^{-1} \\
 &= 18.15 \times 10^{-6} A \\
 &= 18.15 N_A
 \end{aligned}$$

For transistor T2

$$\begin{aligned}
 \text{i) pinchoff voltage } V_{ds} &= V_{sd} = V_{sg}^{-1} \\
 &= (2 \cdot 1 - 1) \\
 &= 1.1 V
 \end{aligned}$$

$$\begin{aligned}
 \text{ii) input voltage } V_{ir} &= 5 - V_{sg} \\
 &= (5 - 2 \cdot 1) \\
 &= 2.9 V
 \end{aligned}$$

$$\begin{aligned}
 \text{iii) Output voltage } V_{out} &= 5 - V_{sd} \\
 &= 5 - 1.1 \\
 &= 3.9 N_{A_n}
 \end{aligned}$$

$$i_v = \text{Saturation current, } J_s = J_{sd} S_d = \frac{e N_p}{2D} \frac{w_2}{L_2}$$

Let us assume that $(V_{sg} - V)$

$$\text{Now } \frac{e N_p}{2D} = 0.75 \times 10^{-11} \text{ A/V}^2$$

$$= \frac{0.75 \times 10^{-11}}{(10^{-3})^2} \text{ A/V}^2$$

$$= 0.75 \times 10^{-11} \times 10^6 \text{ A/V}^2$$

$$= 0.75 \times 10^{-5} \text{ A/V}^2$$

$$= 0.75 \times 10^{-5} \text{ A/V}^2$$

$$\therefore J_{sd} = 0.75 \times 10^{-5} \left(\frac{2}{1}\right) (2.1 - 1)^2$$

$$= 1.815 \times 10^{-5} \text{ A}$$

$$= 18.15 \times 10^{-6} \times 10^{-1}$$

$$= 18.15 \times 10^{-6} \text{ A}$$

$$= 18.15 \text{ nanoAmp}$$

~~AA~~

NMOS pass transistor / transmission gate

→ consists of a minimum geometry n-channel enhancement device

→ not to label the input and output terminals

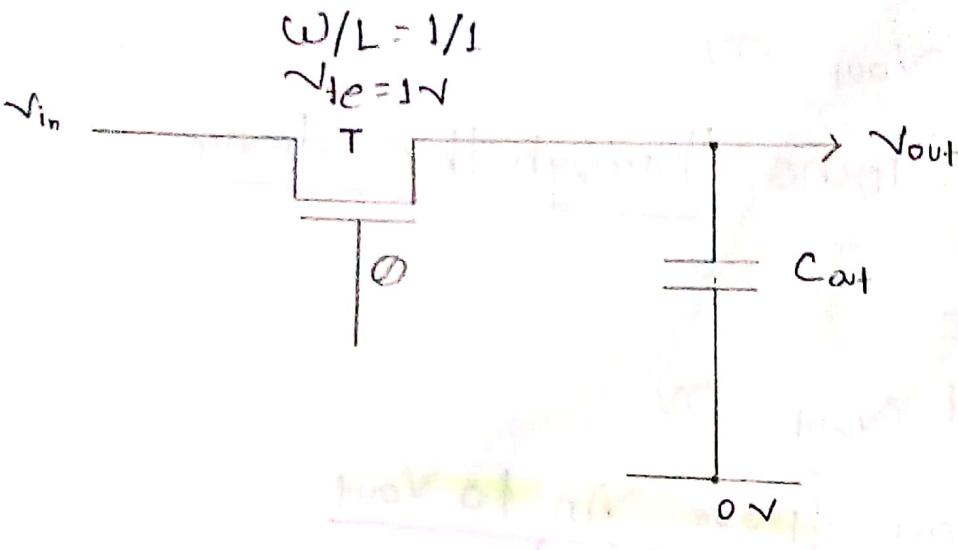
as both can act as the drain or source

depends on {
 → applied voltage
 → existing "

→ act as a voltage-controlled switch

→ devices input to be selectively

transmitted to its output.



- low logic level is 0V
- high " " V_p .
- State of the switch is controlled by the level of ϕ . Transistor T is off regardless of the logic levels existing at V_{in} or V_{out} .
- V_{out} remains at its existing voltage as there is no connection between V_{in} and V_{out} .
- if ϕ goes high to V_p , transistor T turns on. Action now depends on
 - value of V_{in}
 - initial value of V_{out}

There are four cases.

a) $V_{in} = 0V$, initial $V_{out} = 0V$

No current flows through the device

→ input drain

→ output source

b) $V_{in} = V_p$, initial $V_{out} = 0V$

→ Current flow from V_{in} to V_{out}

$V_{GS} - V_T$ causing V_{out} to rise
as C_{out} is charged

→ initially V_{GS} is V_p .

→ As the output rises, the V_{GS} drops.

→ triode at V_{out} is halted when

$$V_{GS} - V_T = 0V$$

→ for body effect V_{out} rises only

to 3.12V. if $V_p = 6V$.

c) $V_{in} = V_p$ initial $V_{out} = V_p - V_T$

→ no current flows as $V_{GS} - V_T = 0V$

→ V_{out} remains $V_p - V_T$

d) $V_{in} = 0V$, initial $V_{out} = V_p - V_t e^{-\frac{t}{\tau}}$

Current flows from V_{out} to V_{in}
 coupling V_{out} to discharge
 to Δ .

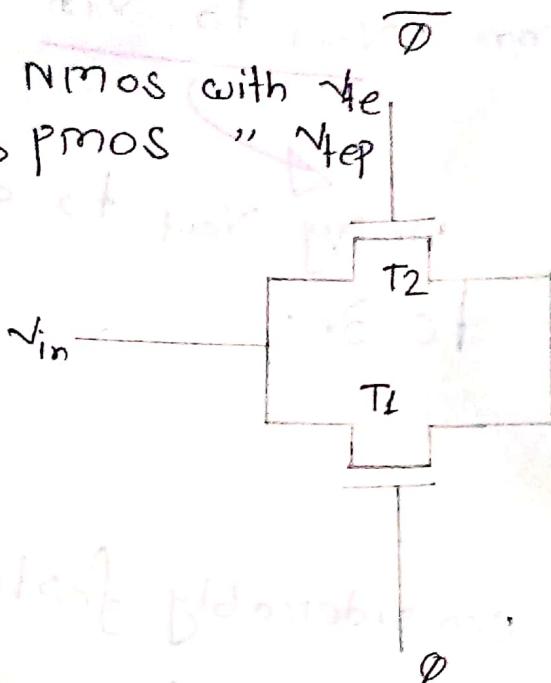
input source
 output drain

* Fall time of V_{out} is considerably faster
 than the rise time encountered in case (b)
because voltage drop across drain is small
as V_{ds} is constant at V_p .

- NB:
- pass transistor / transmission gate
 - passing an input value to the output under the control of the input ϕ
 - gates performance and function.
 - during the application of ϕ

CMOS Pass Gate:

T₁ is NMOS with $\text{V}_G = \text{V}_D$
 T₂ is PMOS " $\text{V}_G = \text{V}_S$



4 cases

- if ϕ is low both transistors are off
- if ϕ is taken high both devices turn on

1 case:

- a) $V_{in} = 0V$, initial $V_{out} = 0V$
 No current flows

Case	V_{in}	V_{out}
a	0V	0V
b	VP	VP

- No current flow
 → drain and source potentials of each device are C_{2V0}
 → No current flow

Case	V_{in}	V_{out}	
c.	V_p	$0V$	<ul style="list-style-type: none"> → Current flow from V_{in} to V_{out} → V_{in} acts as the drain of T_1 → source of T_2 → V_{out} to rise as C_{out} charged up. → V_{sg} of T_2 is V_p throughout this rise → V_{gs} of T_1 is initially <u>V_p</u>, decreased as → At $V_{out} = V_p - V_t$ V_{out} risen. Nmos turns off. → V_{out} continuous to rise to V_p via T_2
d.	$0V$	V_p	<ul style="list-style-type: none"> → Current flow from <u>V_{out}</u> to <u>V_{in}</u> → V_{in} act as the source of T_1 → drain of T_2 → V_{out} to fall as C_{out} discharged → V_{gs} of T_1 is <u>constant</u> during the fall → V_{sg} of T_2 is initially <u>V_p</u>, decreased as V_{out} falls

Chapter-3 (contd)

MOS and BiCMOS

Circuit design process

MOS layers:

→ MOS circuits are formed on bodie layers

→ 4 basic layers

→ n-diffusion
p-diffusion
polysilicon
metal

isolated from one another

by thick / thin
 SiO_2 insulating layer

→ thin oxide mask region includes

→ n-diffusion
→ p-diffusion
→ transistor channel

- ~~→ Polysilicon and thin oxide region intersecting regions form~~
- polysilicon and thin oxide region intersecting regions form to form transistor
- Some processes have
- metal layer
 - polysilicon layer
- layers are joined together
- where contacts are formed.

→ cartoon of a layout
Stick diagram:

It is a stick representation
for the layout.
→ represented by simple lines

Properties of stick diagram:

- * → a means of capturing topography and layer information
 - identifies different layers and their relationship
- conveys layer information through color code
- acts as an interface between a symbolic circuit and actual layout

→ Shows relative placement of component

→ helps plan the layout and routing

→ Shows all components

→ Exact placement of components

→ transistor size

→ wire length, wire width,

→ tub boundaries

→ any other low level details

parasitics

NB: possible to translate

Stick diagram →

layout with
correct
design rules

Stick digicam color codes:

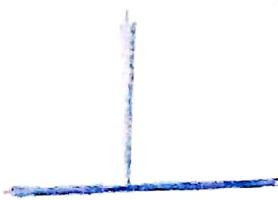
Color	Layers
yellow	P diffusion
green	N diffusion
red	polysilicon
Blue	Metal 1
Contacts	contact cut
yellow (nmos only)	implant
brown (nmos only)	buried contact
dark blue / purple	Metal 2
brown	Demarcation line
grey	overgloss

Rules of Stick diagram:

4 rules

Rule 1:

Sticks of the same type cross or touch each other, represents / belongs to



→ electrical contact
/some mode.

Rule 2: Sticks of the different type

cross or touch each other. represents



no electrical contact

→ to show the connection



→ electrical contact
is needed

Rule 3:

When p or poly crossed diffusion

it represents a bipolar transistor

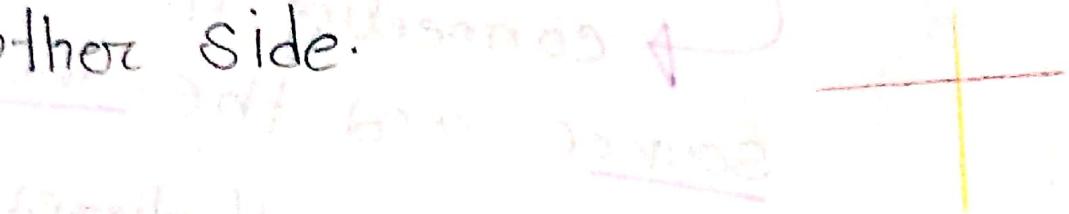
→ if a contact is shown, then it
is not a bipolar transistor

Rule 4:

In CMOS & a demarcation line

is drawn to avoid touching of
p-diff with n-diff.

All PMOS must lie on one side of the line
and all NMOS will have to be on the other side.



Graph the first width or third

marginally. ~~marginally~~

start from bottom of bottom of

NB: Only metal & poly silicon can cross the demarcation line.

Hdg

Fiber

big

#

- polysilicon is drawn on top of diffusion
- Diffusion must be drawn
 - connecting the source and the drain
- Gate is automatically self-aligned
 - during fabrication
- When a metal line needs to be connected to one of the other three coordinates
 - a contact cut (via) is required

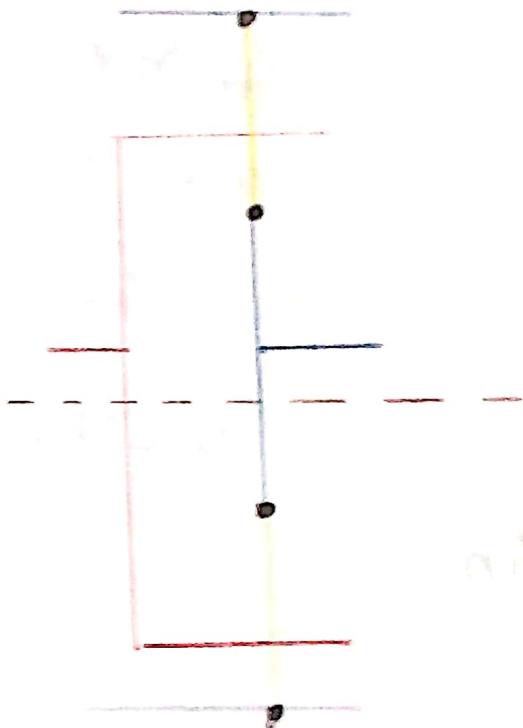


B) Schematic diagram of CMOS inverter:

Credit diego



Stick diagram

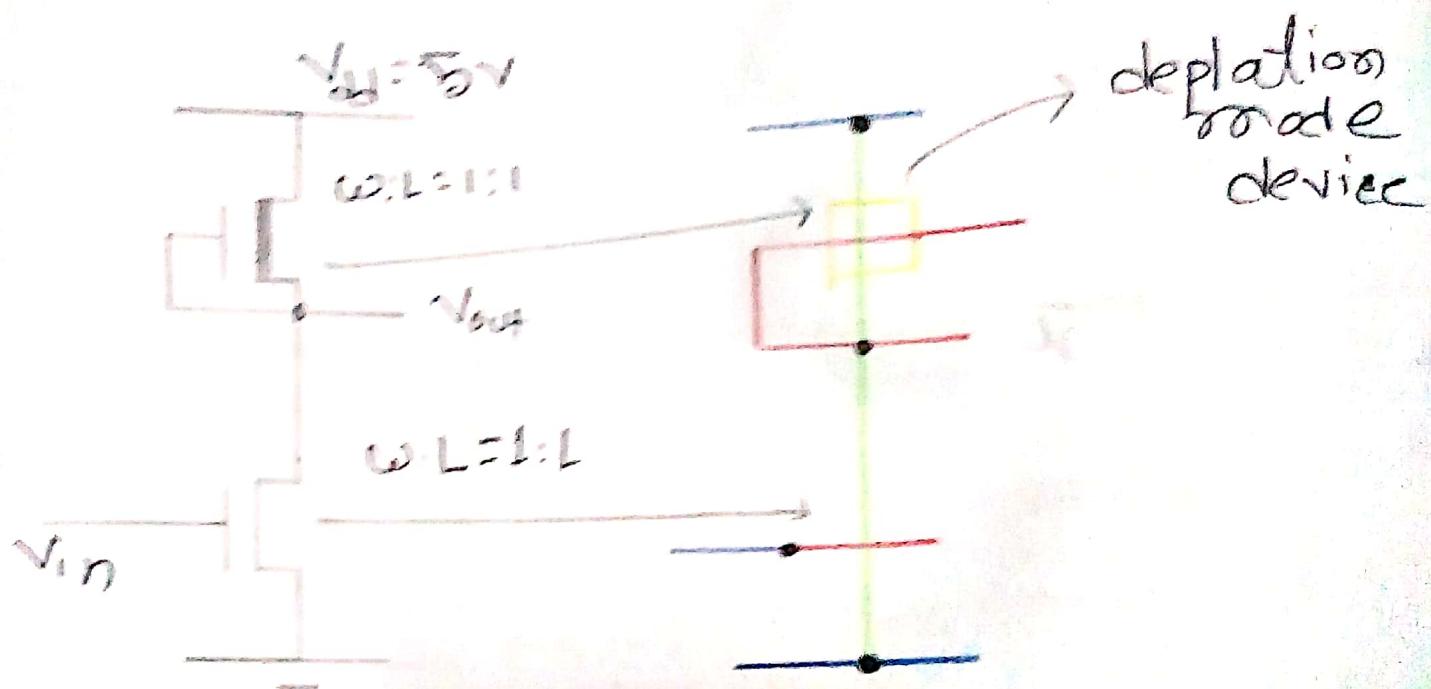


Stick diagram-1

Stick diagram - 2

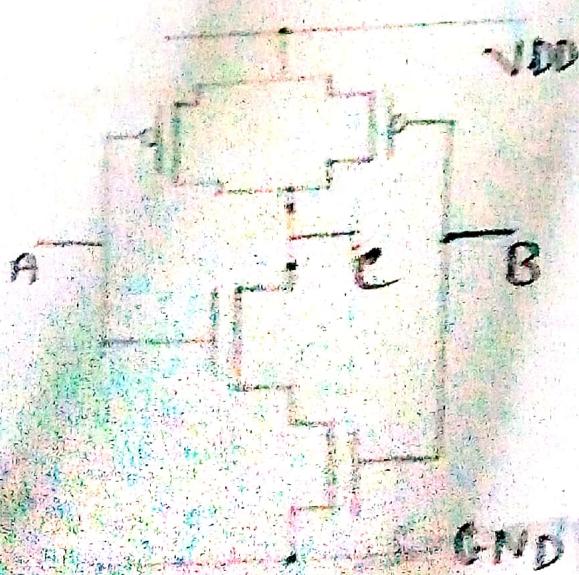
B Stick diagram of nmos inverter (depletion mode)

Circuit diagram:



B Stick diagram of cmos NAND gate:

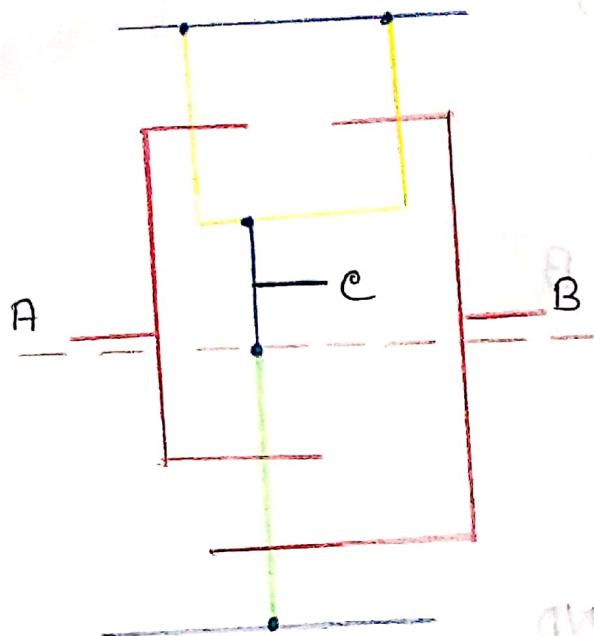
Circuit diagram:



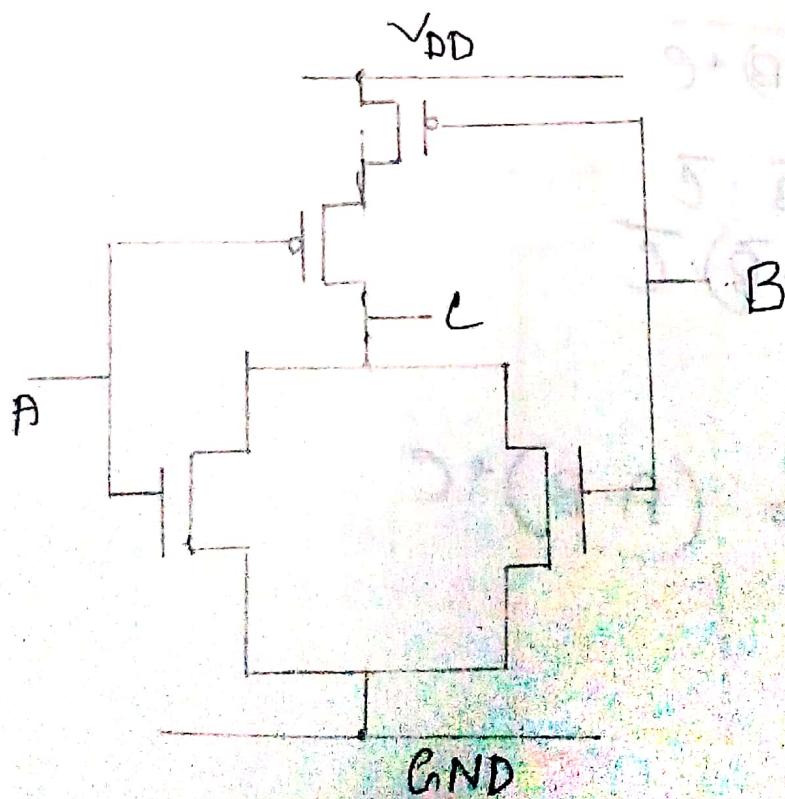
in1	in2	out
A	B	c
0	0	1
0	1	1
1	0	1
1	1	0

$$c = \overline{A \cdot B} \\ = \overline{A} + \overline{B}$$

Stick diagram

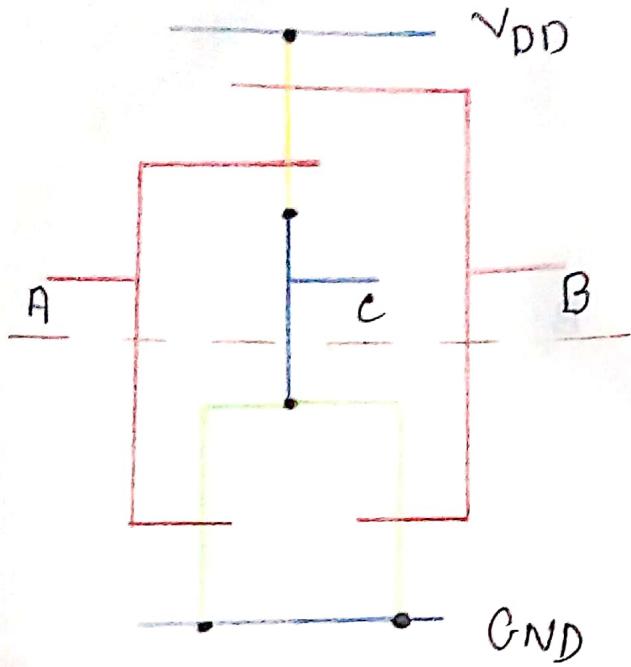


Stick diagram of CMOS NOR gate



A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

$$\begin{aligned}C &= \overline{\overline{A} + \overline{B}} \\ &= \overline{\overline{A}} \cdot \overline{\overline{B}}\end{aligned}$$



Stick diagram of $f = \overline{(A \cdot B)} + C$

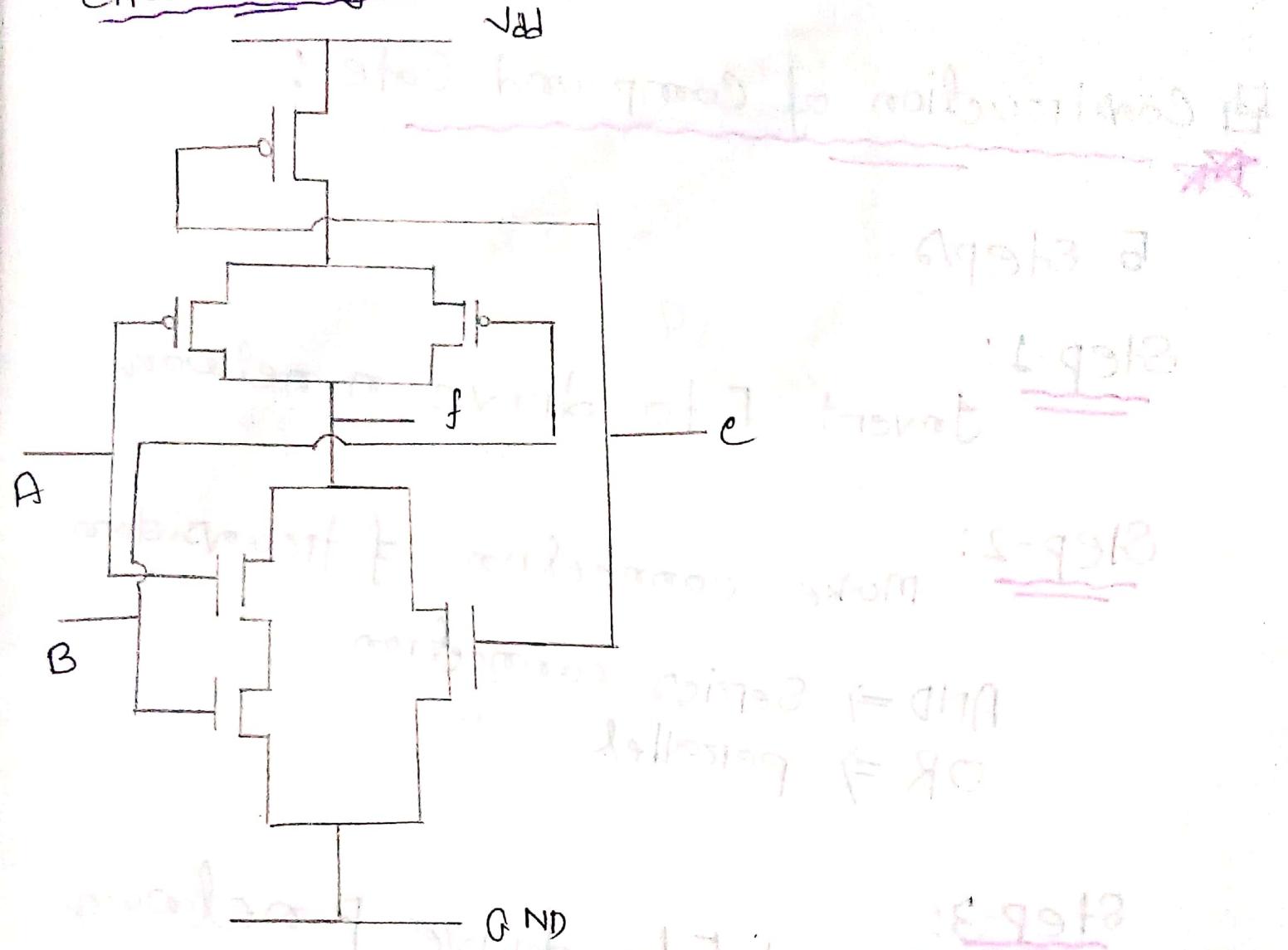
* Now, $f = \overline{(A \cdot B)} + C$

$$\begin{aligned}
 &= \overline{A \cdot B} \cdot \overline{C} \\
 &= (\overline{A} + \overline{B}) \cdot \overline{C}
 \end{aligned}$$

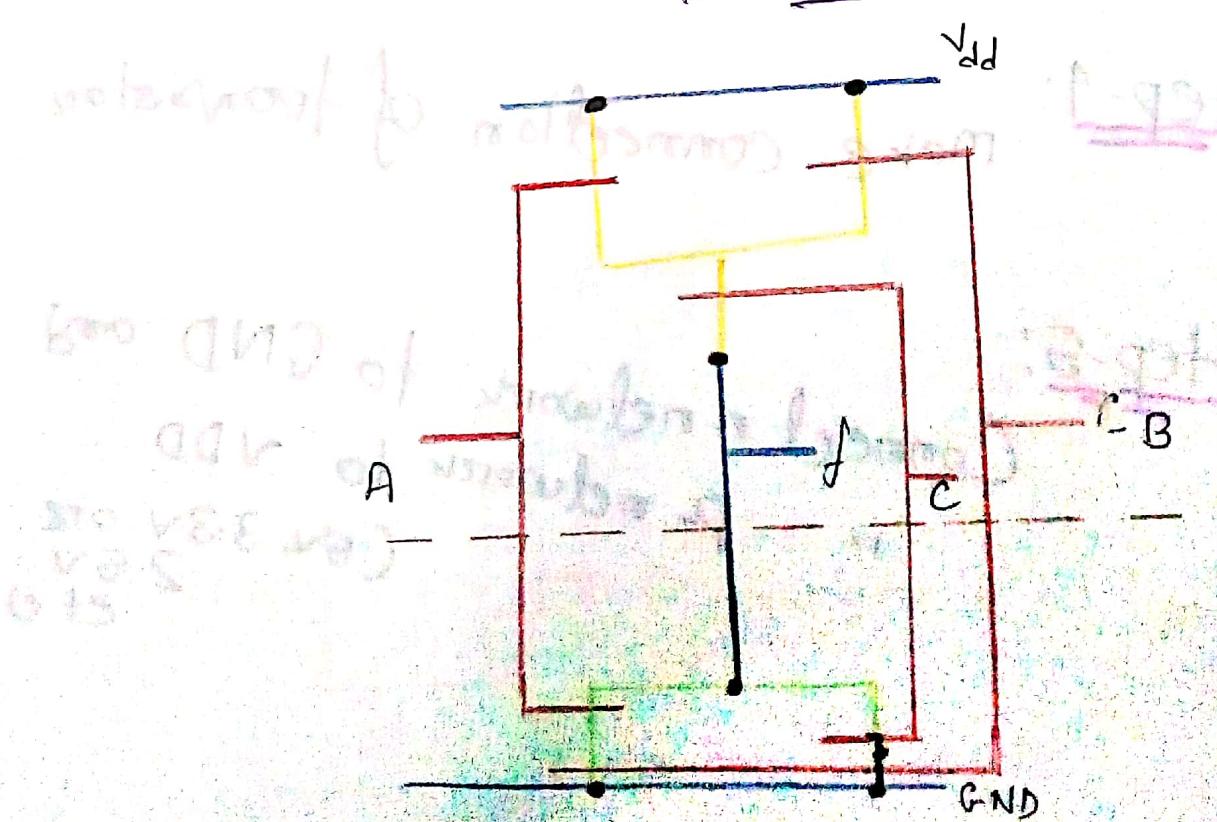
po pull down $f' = (A \cdot B) + C$

GND

Circuit diagram



Stick diagram



Construction of Compound Gate:

5 steps

Step-1:

Invert F to derive n-network

Step-2:

Make connection of transistors

AND \Rightarrow Series connection

OR \Rightarrow parallel "

Step-3:

Expand F to derive P-network

Step-4:

Make connection of transistors

Step-5:

Connect n-network to GND and
,, P-network to VDD

(5V, 3.3V, or
2.6V
etc.)

Stick diagram of $F = \overline{A \cdot B} + C \cdot D$

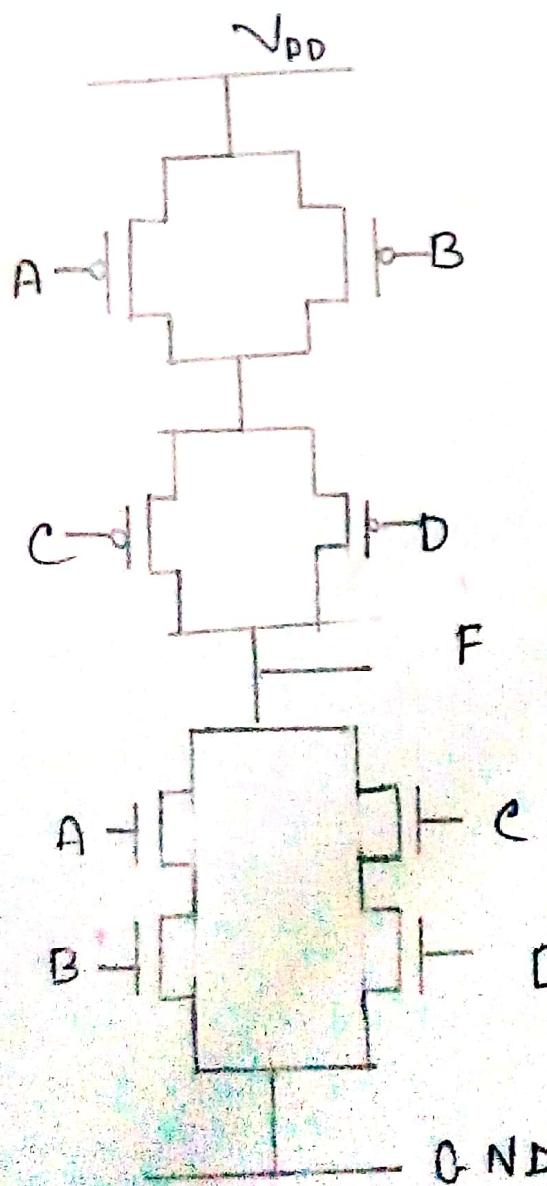
$$\text{Now; } F = \overline{A \cdot B} + C \cdot D$$

$$= (\overline{A} \cdot \overline{B}) + (C \cdot D)$$

$$= (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$$

$$\text{Again } F' = \overline{F} = \overline{\overline{A \cdot B} + C \cdot D}$$
$$= A \cdot B + \overline{C \cdot D}$$

\therefore Circuit diagram



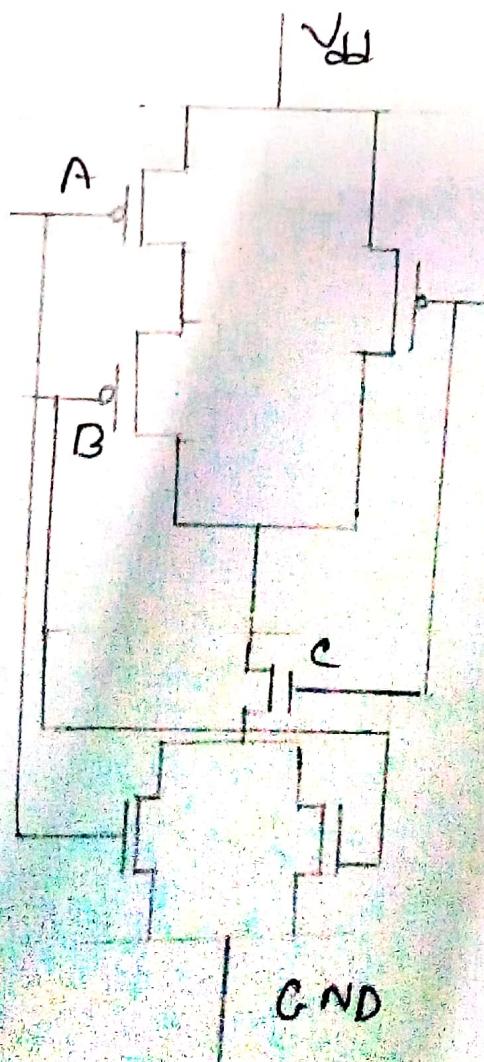
Circuit diagram of $f = \overline{(A+B)} \cdot C$!

PULL UP $f = \overline{(A+B)} \cdot C$

$$= (\overline{A} + \overline{B}) + \overline{C}$$

$$= (\overline{A} \cdot \overline{B}) + \overline{C}$$

PULL-down $f = (A+B) \cdot C$



About CMOS

→ CMOS always provide inverted output

like inverter

→ NAND
→ NOR
→ XNOR

→ Non-in

→ inverter is added with the CMOS output

B
if non-inverting
function is required

→ AND
→ OR

→ logic AND function

Circuit diagram of 2-input AND gate:

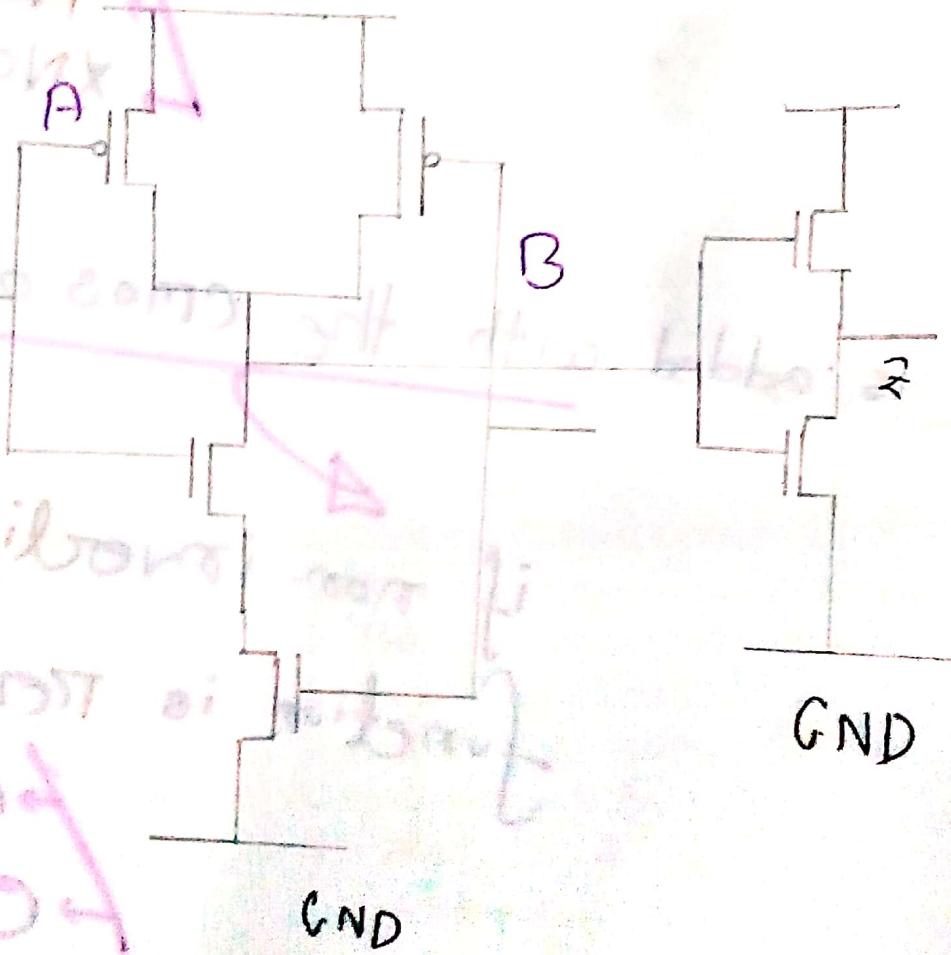


Fig: 2-input AND gate

Q) Circuit diagram of 2-input XNOR / XOR gate

$$\begin{aligned} \text{Pull up } f &= \overline{\overline{A} \oplus B} \\ &= \overline{\overline{A}B + A\overline{B}} \\ &= \overline{\overline{A}B} \cdot \overline{A\overline{B}} \\ &= (\overline{\overline{A} + \overline{B}}) \cdot (\overline{\overline{A}} + \overline{\overline{B}}) \\ &= (A + \overline{B}) (\overline{A} + B) \end{aligned}$$

$$\begin{aligned} \text{Pull down } f &= A \oplus B \\ &= \overline{\overline{A}B + A\overline{B}} \end{aligned}$$

Pull Up Network vs Pull Down Network



Pull Up	Pull Down
1) Used to make <u>output as logic</u> <u>High</u>	1) Used to make <u>output as logic</u> <u>Low</u>
2) It is made up of <u>PMOS transistor</u>	2) It is made up of <u>NMOS transistor</u>
3) W/L ratio of <u>PUN transistor</u> is <u>higher</u> → os mobility of PMOS < NMOS	3) W/L ratio of <u>PDN transistor</u> is <u>lower</u> → os mobility of NMOS > PMOS

Chapter 3 (PDVS)

Fabrication and Design Rules

NMOS Process

→ IC are manufactured on a wafer

having many chip position.

→ Circular wafer of 100 mm diameter

→ Accommodate
506 mm × 6 mm
chip.

→ fabrication of one MOS wafer requires

between 6 and 11
patterning levels

→ each pattern layer pattern leads to

the production of a mask



by photographic technique

Types of mask:

2 types

→ allows light through the defined

shape, but blocks light from
passing through other gaps

→ allows light through areas

external to the shapes

Steps of MOS procedure:

Step-1: material growth
New material is formed on or
(oxide)
in the surface of the wafer.

This is done by means of
→ evaporation
→ thermal growth
→ ion implantation

Step-2: layer patterning

Define the desired layer pattern

in the grown material

→ wafer is covered with photoresist

→ photoresist is exposed to UV-light

through the appropriate mask

Step-3: removal of unexposed resist:

→ positive or negative resist
can be used

Exposed to the light
are hardened
of opposite effect.

Step-4: oxide etch

→ underlying material is etched away

→ hardened ~~pre~~ photoresist is
protects its underlying material

from the etch

Step-5: final layer pattern

→ hardened photoresist is removed
by etching

Q Steps of nmos fabrication: (BND-17)

1. A thin wafer cut from a single crystal of silicon of high purity
in which required p-
impurities are introduced.
2. A layer of SiO_2 - typically 1 nm thick
is grown all over the surface
of the wafer

3. Surface is now covered with photoresist which is deposited onto the wafer

4. The photoresist layer is then exposed to uv-light through a mask

→ region into which diffusion is to take place together with ^{from} _{comistor channel}

5. There are one subsequently readily etched out together with underlying SiO_2

6. → Remaining photo resist is removed.
 - A thin layer of SiO_2 (0.1 nm) is grown over the entire chip surface
 - Polysilicon is deposited on top of this to form the gate structure.

→ Further photoresist coating and masking

allows the polysilicon to be patterned.

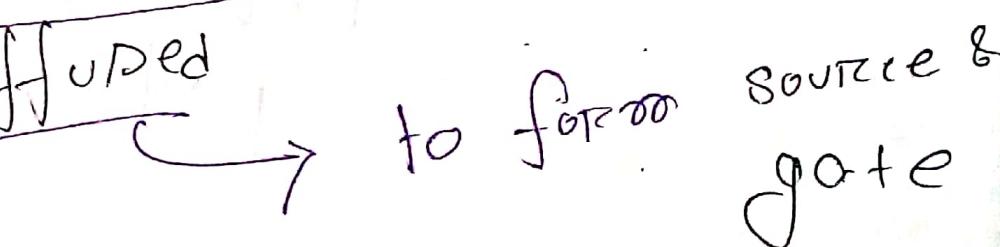
→ Thin oxide is removed



to expose areas into which

n-type impurities are to be

diffused



to form

source &
gate

→ Thick oxide is grown all over

→ Masked with photoresist.

→ Etched to expose selected areas
of the

where A connections to
be made.

9. \rightarrow metal layer is masked

\rightarrow " " is etched at

\hookrightarrow to form the
rewired interconnection
pattern.

CMOS fabrication:

approaches:

widely used in practice

→ P-well

→ n-well → also popular

→ twin-tub

→ Silicon on-insulators

P-well Fabrication Flow:

→ Start with n substrate (donor $N_d = 10^{15} \text{ cm}^{-3}$)

→ Form p-well region (Brown mask)

→ Define PMOS and NMOS active region
(Green mask)

→ Form field and gate oxidations

→ Form polysilicon (Red mask)

→ Implant Pt diffusion (Yellow mask)

- Jeoplene
- Jeoplene on diffusion (green mark)
- Create contact cut (black mark)
- metallization (blue mark)

n-well Fabrication flow:

→ Start with p substrate

→ Form n-well region

→ Define pmos and nmos active region

→ Form field and gate oxidation

→ Form polysilicon

→ Implant n+ diffusion

→ Implant p+ diffusion

→ Create contact cut

→ Metalization

NB

: n+ mask or its complement is used

* OTC P+

or "

" "

■ Photoresist:

A light-sensitive material used
in several processes

to form a patterned
coating on a surface.

■ Types of photoresist:

2 types

→ positive photoresist

→ negative photoresist

portion of the photoresist that
is exposed to light becomes soluble

portion of the photoresist
that is exposed to light becomes
insoluble

Appendix-C

The programmable logic array (PLA)

PLA:

Programmable logic device that provides the designer

→ systematic and regular way of implementing multiple output functions of

n variables in sum of products

→ programmed by the manufacturer

→ field " by the user → to meet require ments.

→ way in which PLA maps onto the
chip indicated by a floor plan

floor plan:

gives the notational area
and relative disposition
of particular circuit & subcircuit

Floor plan layout for a PLA:

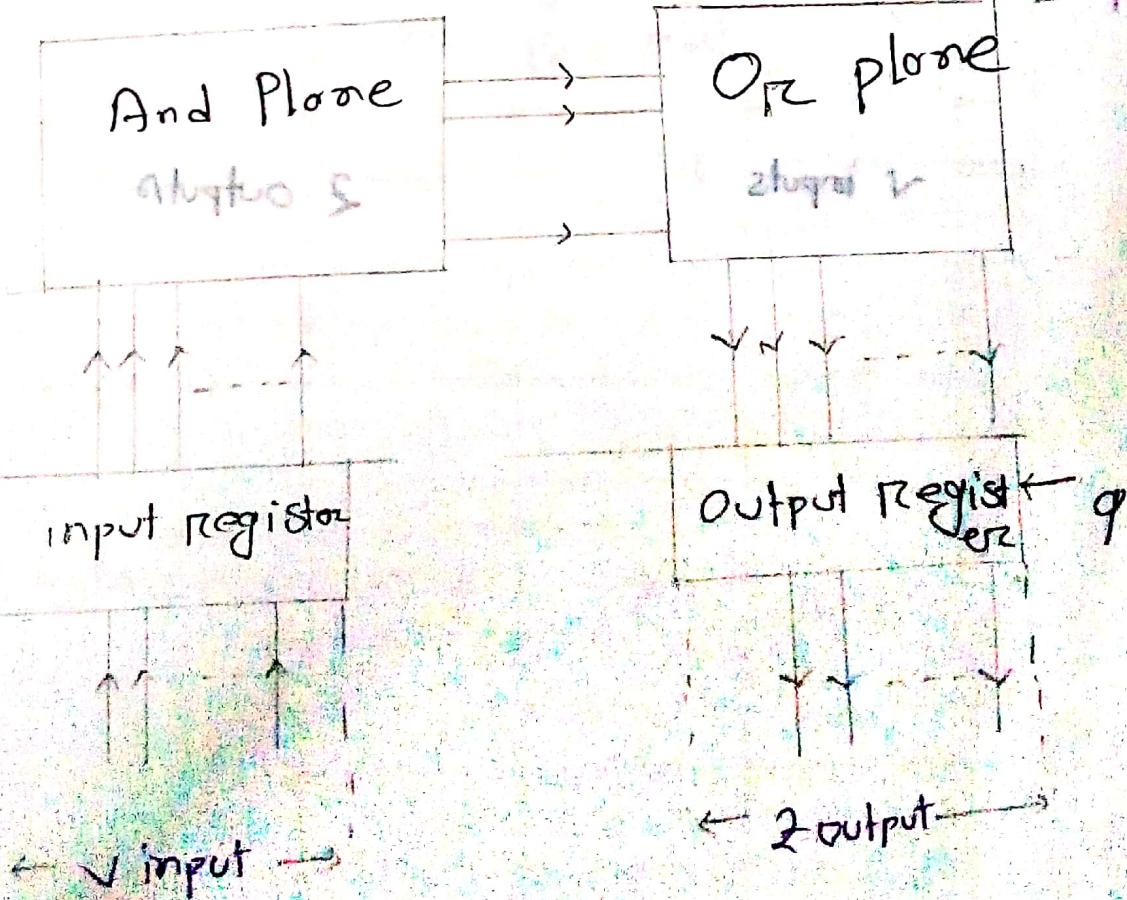


2 types of plan

→ And/Or based

→ NOR based

And/Or based:



← P products

NOR based:

NOR plane

P' products

NOR plane

2 sums

p
product

inverting
input register

ϕ

Sum 1

→ v inputs →

inverting
output register ϕ_2

Sum 2

→ 2 outputs →

題 2017-5(a)

(d) F-Block

Given that, *left row*

$$BA + BG = F_1 = ab + a\bar{e}$$

$$A + B\bar{B} = g, F_2 = ab\bar{e} + a\bar{e}\bar{e}$$

$$F_3 = ab + a\bar{e}$$

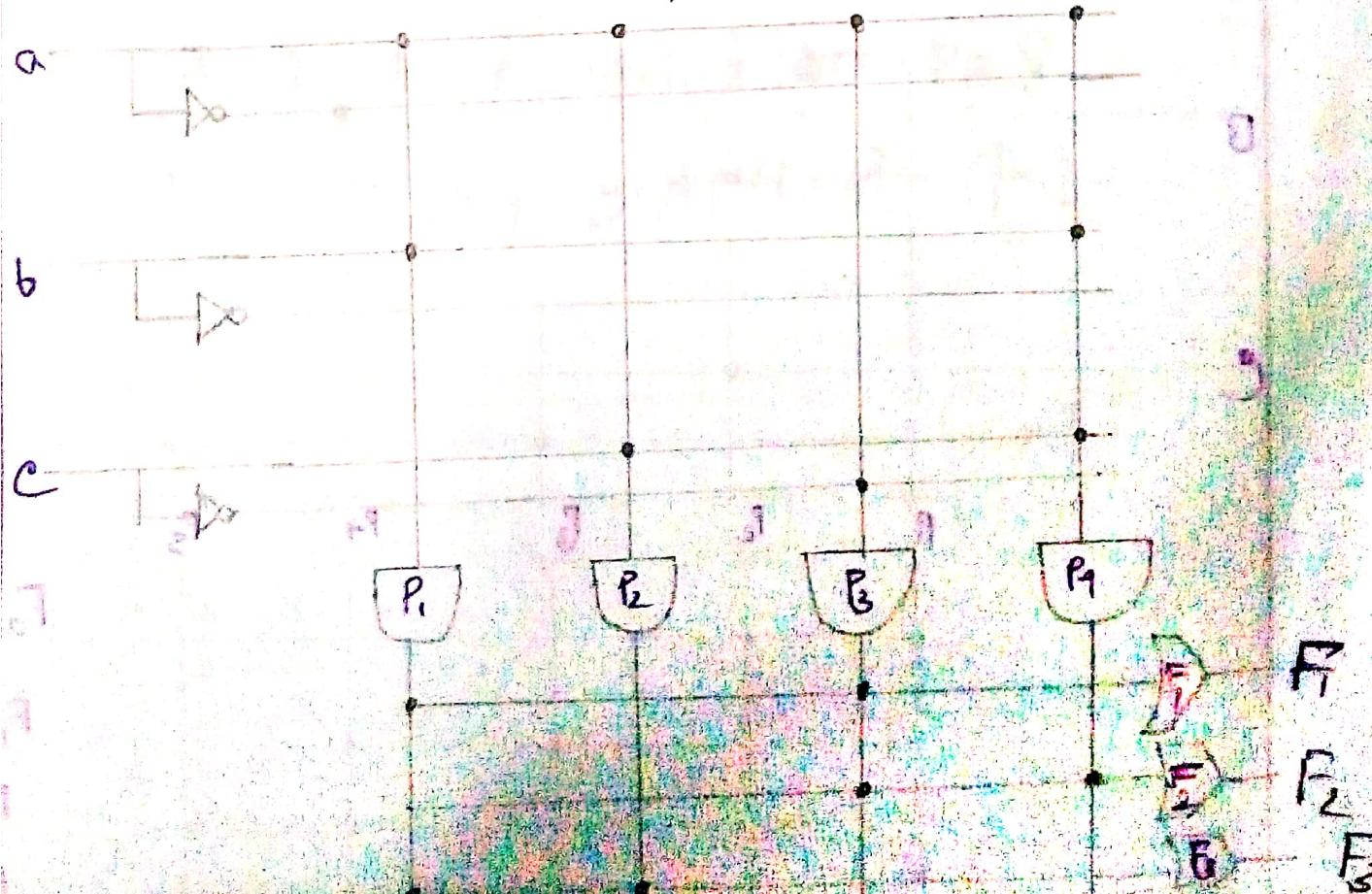
$\therefore A$ = number of inputs = 3

$B, \bar{B} = 2$ of Pre-term, $P = 1$

, of output, $Z = 3$

Let, $P_1 = ab$ $P_3 = a\bar{e}$

$P_2 = a\bar{e}$ $P_4 = abc$



2016-7(b)

(Q2-Flo)

Given that,

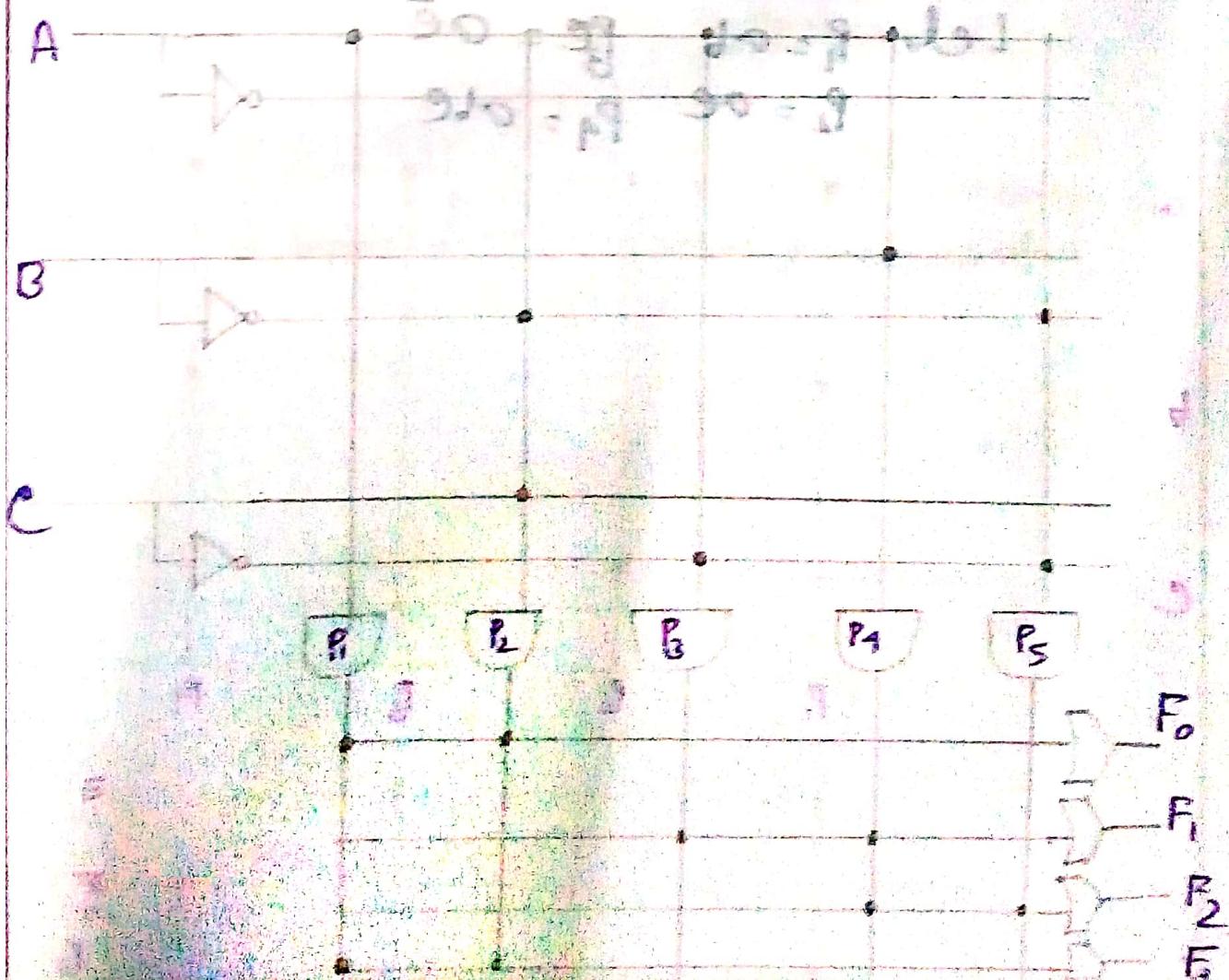
$$F_0 = A + \bar{B}C, F_1 = A\bar{C} + AB,$$

$$F_2 = \bar{B}\bar{C} + AB, F_3 = \bar{B}C + A$$

Let, $P_1 = A$, $P_2 = \bar{B}C$, $P_3 = A\bar{C}$.

$$P_4 = AB, P_5 = \bar{B}\bar{C}$$

S = ~~Let us find for~~



Given

Example-1:

Given that

$$Z_1 = \bar{a}\bar{b}\bar{c}e + \bar{a}\bar{b}\bar{c}\bar{d}\bar{e} + bce + de$$

$$Z_2 = \bar{a}\bar{c}e$$

$$Z_3 = bce + de + \bar{c}\bar{d}\bar{e} + bd$$

$$Z_4 = \bar{a}\bar{c}\bar{e}e + ce$$

Number of input, $N = 5$

" " of product term, $P = 8$

" " of output, $Z = 4$

a)  \rightarrow $F = 150 \text{ N}$

b)  \rightarrow $3b + d + 3b + 3d + 5d = 150$

c)  \rightarrow $3b = 150$

d)  \rightarrow $b + 3b + b + 9d = 150$

e)  \rightarrow $5b + 33d = 150$

$P_1, P_2, P_3, P_4, P_5, P_6, P_7, P_8$

$P \rightarrow \text{Huggel} + 0$

Z_1

Z_2

Z_3

Z_4

Design Representation:

entity selected as robot design

■ Levels of design

3 levels

→ Behavioral

→ High level design

→ intermediate design

→ Low level design

A design can be represented

at various levels from three

different angles:

1) Behavioral design means what the

2) Structural means to do

3) Physical

means how it is implemented in terms of the circuitry

★ Physical means the actual representation whether it is implemented on a chip / model cell.

NB: Can be represented by Y-diagram

■ Y-diagram

Behavioral
Domain

- Program
- Specification
- truth-table
- finite-state machine

Structural
Domain

- Gates
- Interconnects
- Registers
- Address

- Transistors/Layouts
- Cells
- Chips/Boards

Physical/Geometric
Domain

Gajski-Kuhn Y-chart

→ depicts the different perspective
in VLSI H/CO design

→ used for the development of
normal
JC

→ the issue in the H/CO development
is most often top down design

Problem:

This is ~~perceiv~~ perceived by the
three domains of

behavior

structure &

the layout

goes top-down

to more detailed
abstraction levels

- Outer shells are generalizations
- inner ones → refinements of the same subjects.

5 levels of Gajski-Kuhn Y-chart

- system level
- algorithmic level
- register-transfer level (RTL)
- logical level
- circuit level

System level:

Basic properties of an electronic system are determined behavior → abstraction of signals & their time response

Structure → CPU's ~~hardware~~ ~~implementation~~

Physical → chip implementation.

multiple transistors to

memory

clock

control

AVL tree ALA

Rebalanced

new node involved

new node has ~~been~~ been

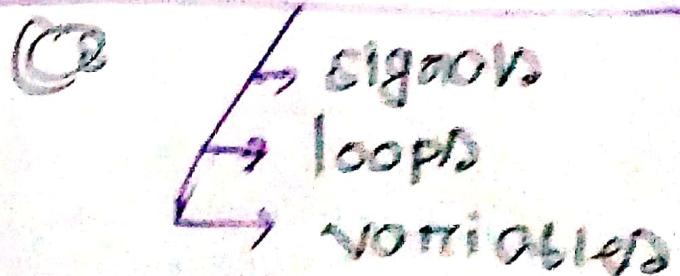
bad node is

↪ 3 nodes left in
tree one root node

Algorithmic level (or statements)

defined by the definition

of concurrent algorithm



Structure → ALU are in use

Register-transfer level

behavior between communicating registers and logic units is described.

→ data structure & data flows are defined

→ design set step of the floorplan

is located

bedimmed → in the geometric view

basic configurations 5d

filler cells

logical level:

described in the

behavioral perspective by Boolean equation

got the structural view

→ displayed with gates
→ flip-flop

→ the geometric domain

→ described by standard
cells

Circuit level:
Detailed description of the circuit behavior

By Beta

Behavior is described
by mathematics using

→ differential equation
→ logical

Structure → transistor

geometrie → transistor layout/

capacitors up to

crystal lattices

Alternative Representation of Y-chart

Algorithm → Processor → Chip
Floorplan

→ Finite state → Register → Model
machine ALU placement

→ Model description → Leaf → cell
placement

→ Boolean Equations → Transistor → Mask

→ It is a topdown approach

→ This is in helix shape

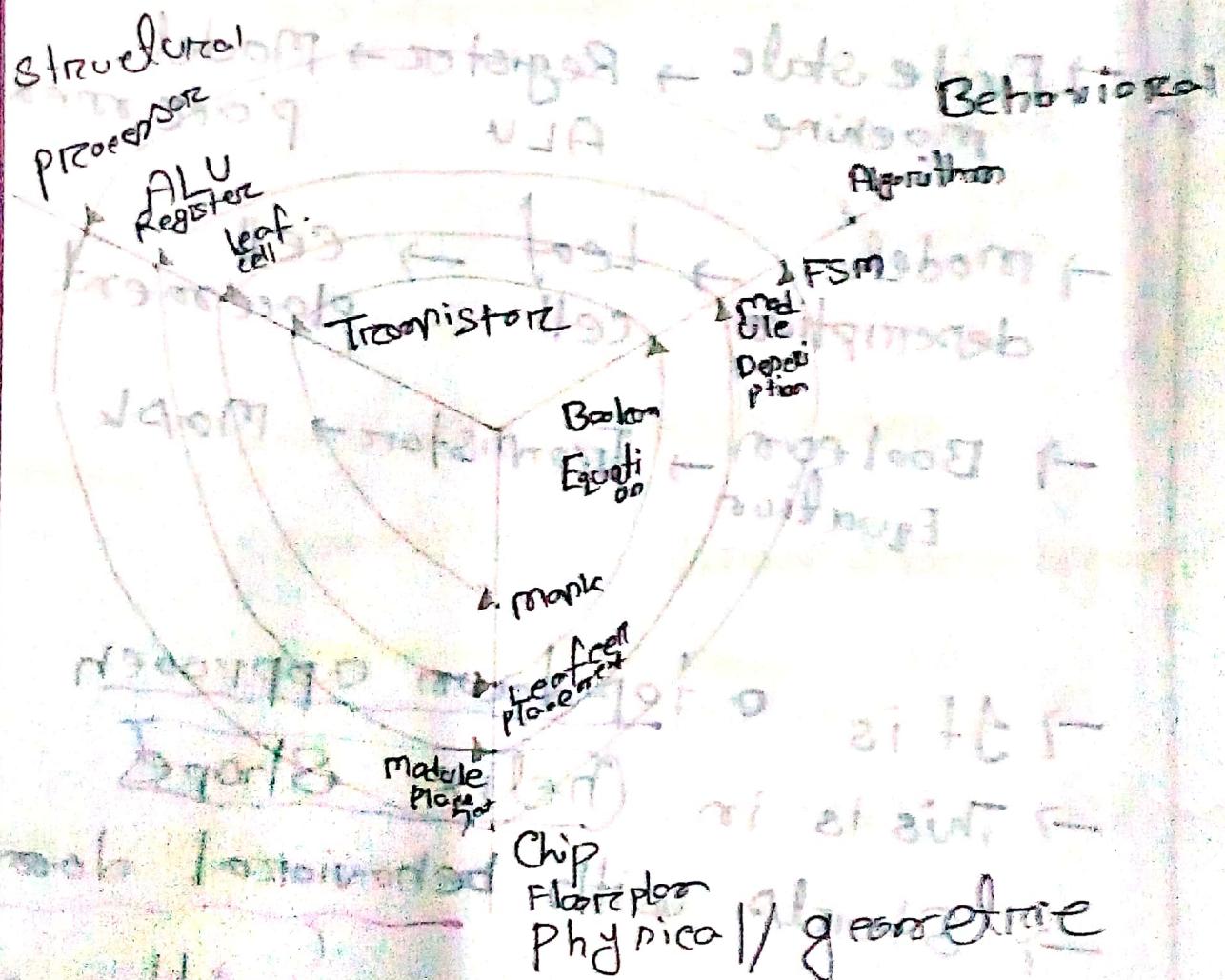
→ Starts with behavioral domain

→ finally moved to

↳ transistor &
→ mask level

Praktikum für Mechatronische Systeme

Qualität & Nachvollziehbarkeit von Software



Behavioral representation

Specifies how a particular design
should respond
→ to a given set of inputs

Specified by

→ boolean equation

tables of input & output
values

Algorithm written in
Standard HLL like C

* special HDL

like Verilog
or VHDL

NB: VHDL → Very High Speed Hardware Description Language

VHDL → Very High Speed Integrated Circuits

Structural representation

Specifies how components are interconnected.

In general the description is a list of modules and

their interconnections

called netlist

levels

functional level

gate

switch

circuit

Physical representation:

The lowest level of physical
specification.

↗ photo mask information

required by the various
processing steps

↗ in the fabrication
process

Physical Design Flow

Partitioning

Physical design

Design that converts a

circuit description into a geometric
description.

→ used to manufacture a
chip.

Physical design cycle

1. Partitioning
2. Floorplanning & placement
3. Routing
4. Co-optimization
5. Extraction & verification

Cell-based layout

Partitioning

Floorplanning &
placement

Routing

Circuit
Design

Fabrication

Compaction

Extraction

&
Verification

Circuit partitioning

It is the task of dividing a circuit into smaller boards.

→ Decomposition of complex system into smaller subsystems

→ Each subsystem can be designed

→ minimize the interconnection between the subsystems

→ decomposition

→ Decomposition is carried out hierarchically until each

subsystem is of manageable size

■ Objective: ~~Minimizing functional~~

to Partition a circuit into
parts such that every component
is within a prescribed range

of the number of connections

among the components
is minimized.

■ Partitioning lead to

→ Blocks with well-defined
areas and shapes (hard blocks)

→ Blocks with well defined

areas and flexible
shapes (soft blocks)

→ A netlist specifying connections between the blocks

■ Floorplanning: inputs to the floorplanning problem:

→ A set of blocks, hard or soft

→ Pin locations of hard blocks

→ A netlist

■ Objective of floorplanning:

→ minimize area

→ reduce wirelength for critical nets

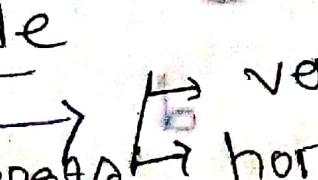
→ determine shape of the soft blocks.

Slicing floorplan:

A slicing floorplan can be represented by a slicing tree.

Slicing tree:

A binary tree where

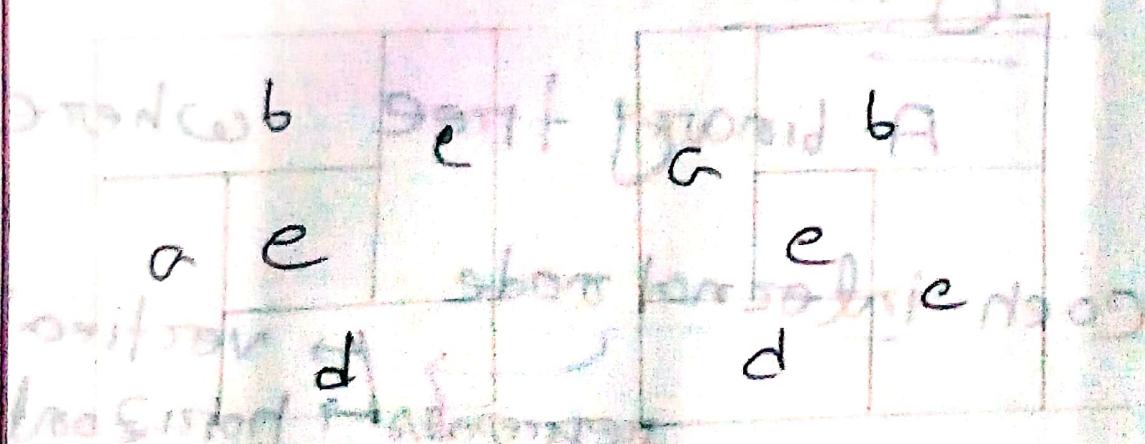
each internal node represents  vertical cut  horizontal "

of each leaf node  or basic rectangle

■ non-slicing floor plan:

One that ~~can't~~ ~~be~~ ~~obtained~~ by repetitively subdividing alone.

Also called WHEEL



■ Types of slicing tree

2 types

→ skewed slicing tree

→ non-skewed " "

Skewed binary tree

A skewed tree in which no

node has its right child like the
one below

core

↳ skewed binary tree:

non-skewed binary tree; that is not skewed

Some rules (options):

- block of left side \rightarrow left
- " of right .. \rightarrow right
- " of top side \rightarrow right
- " of bottom " \rightarrow left

Wavy structures are formed by
one, one, one one one

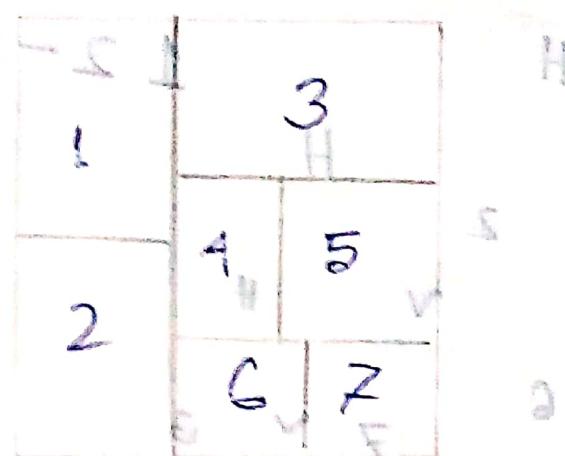
that can be obtained by
repeatedly splitting rectangles.

Wavy patterned or a
vertical line
into wavy rectangles.

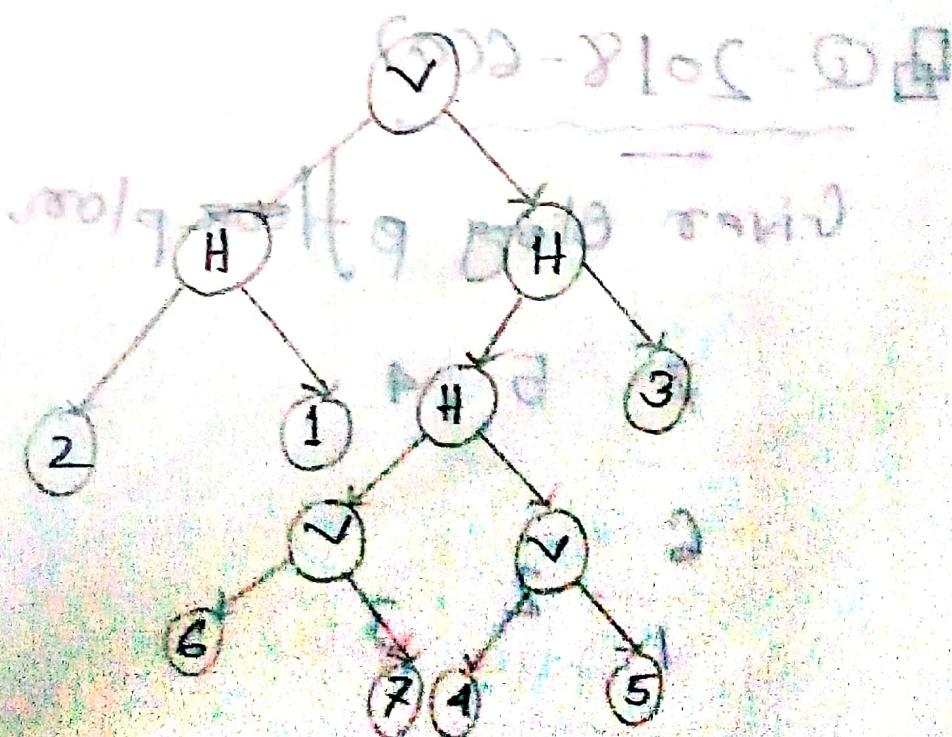
Wavy patterned or a
vertical line
into wavy rectangles.

Example 1

Given slicing floor plan.



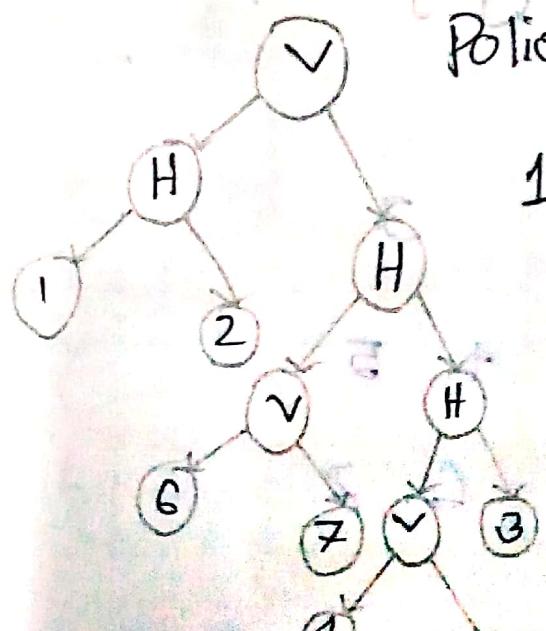
Skewed slicing tree:



Polish notation:

21-671951-3-1

Non skewed slicing tree

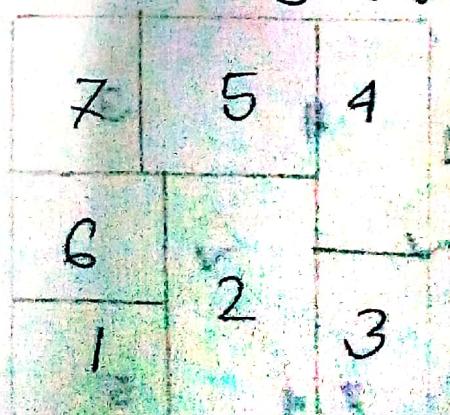


Polish rotation:

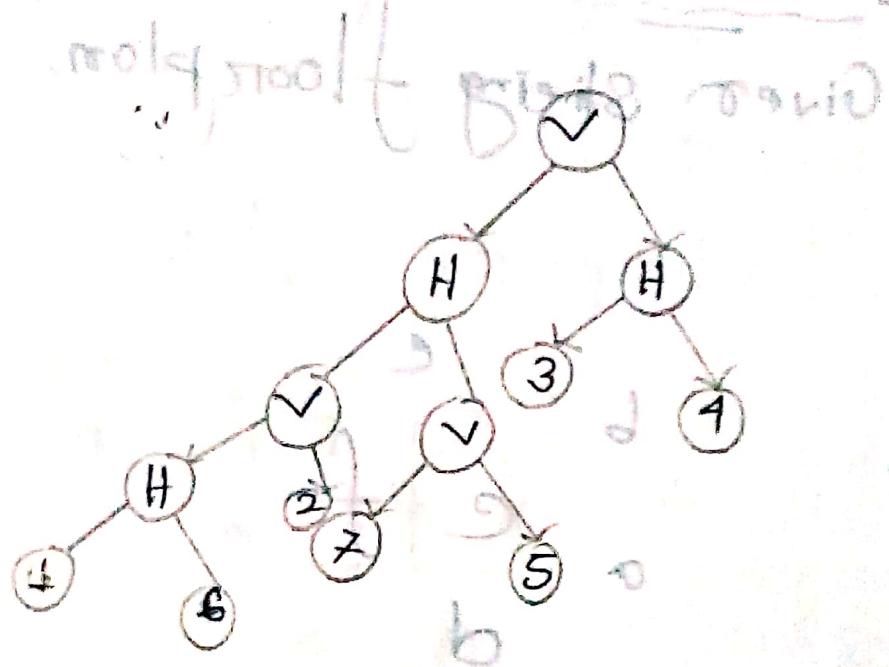
1 2 - 6 7 1 4 5 1 3 - -

Q-2018-6(a)

Given slicing p floor plan,



Skewed Slicing tree:



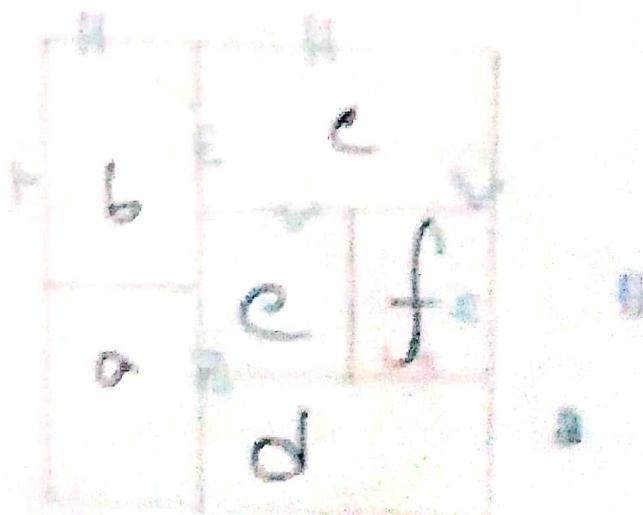
Polish notation:

1 6 - 2 1 7 5 1 - 3 4 -

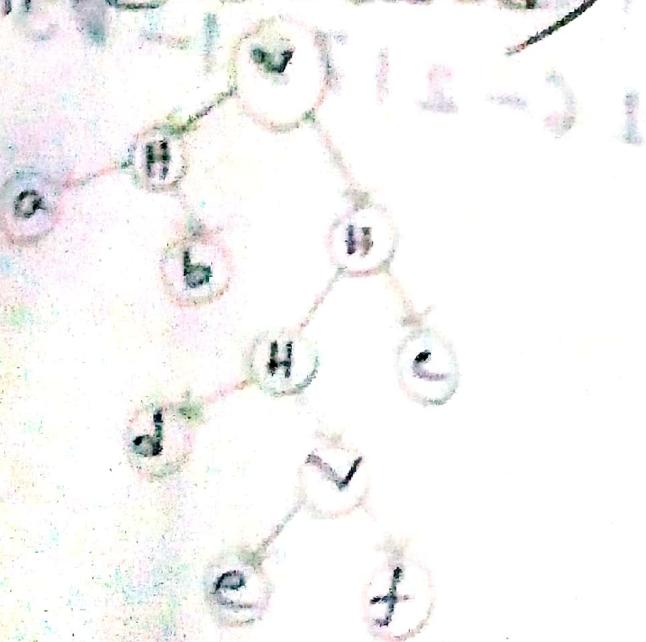
1 - 3 - 1 7 9 6 - 4 0

Example-2

Given step floor plan.



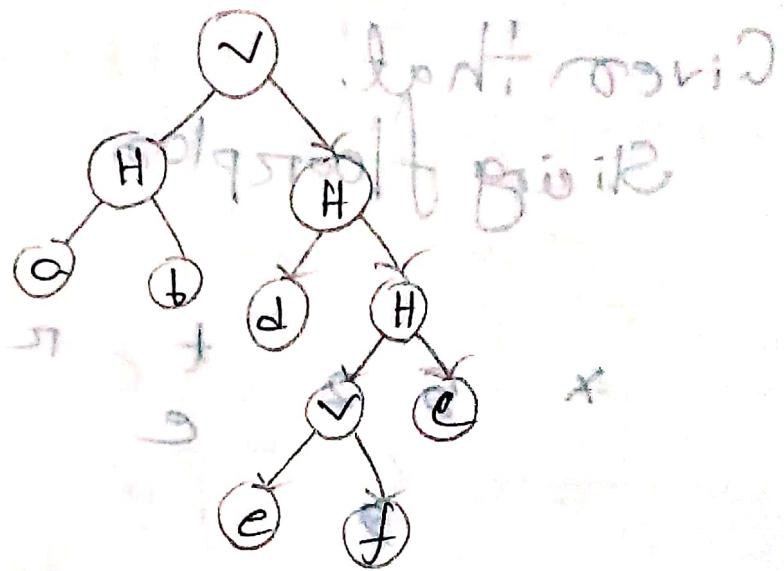
String tree (Levelled) too clean



Polish expression:

ab-defh-e-l

Slewing tree (non-skewed)



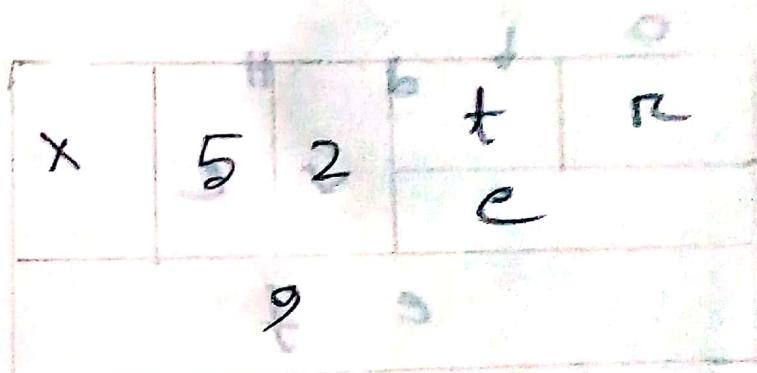
Polish expression:

ab-d-e/fc- -1

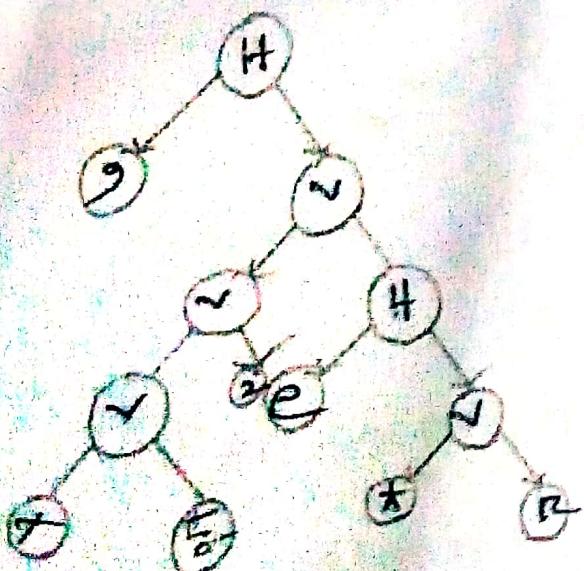
~~Strengths - OTG Smart Grid~~
BQ-2017-6(b)

Given that,

Slicing floor plan



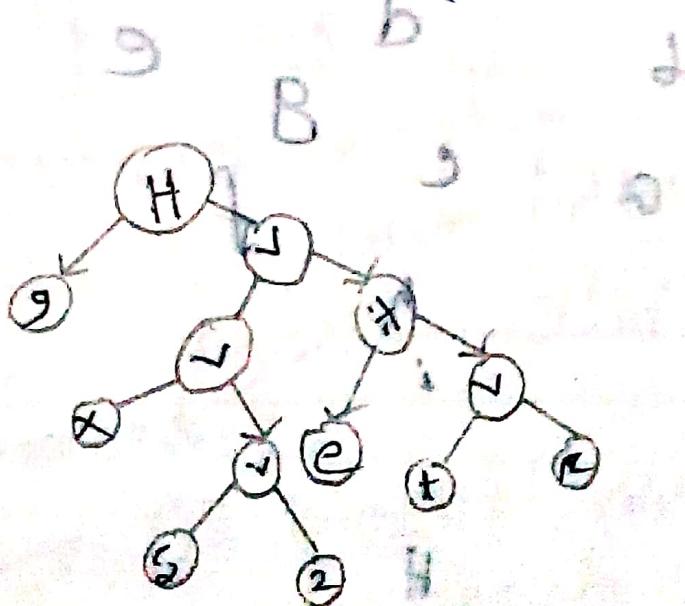
Slicing tree CS (ewg)



Polish notation:

possible with hints & guide
9 * 5 / 2 ^ e t r 1 - 1 -

Slicing tree (non skewed)



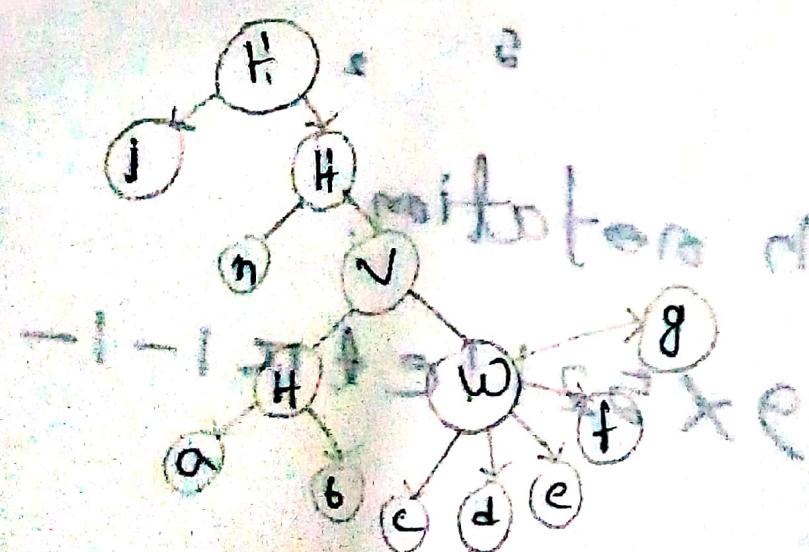
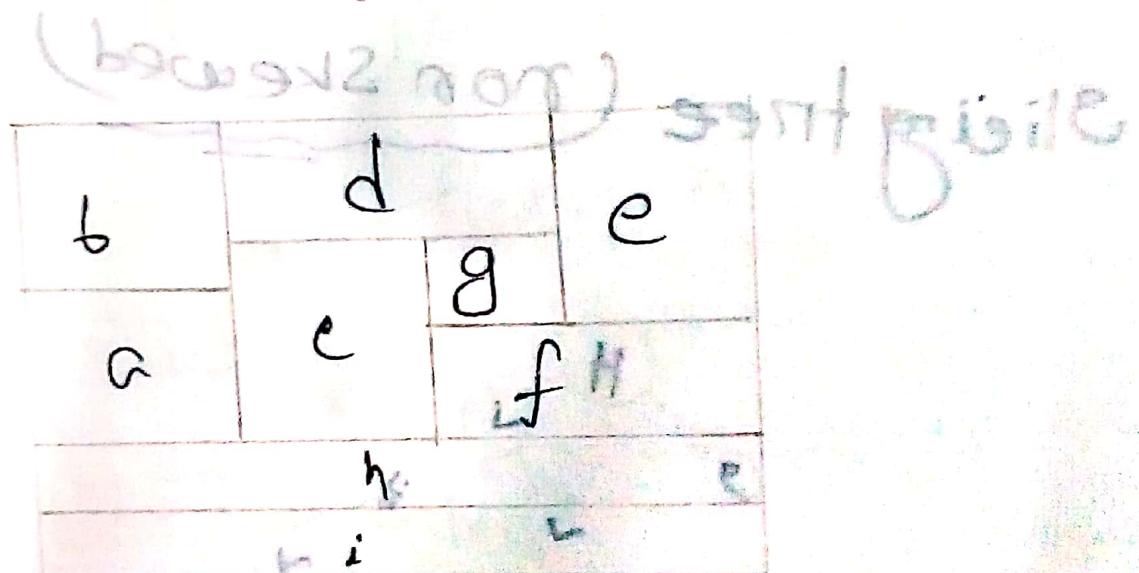
Polish notation:

9 * 5 / 2 ^ e t r 1 - 1 -

Given

 Example -3 / Hierarchical
 → 1st floor plan

Given Slicing floorplan,



Floor planning Vs Placement



In floor planning,

→ some of the blocks may be flexible

→ exact location of the pins are not fixed

In placement:

→ All blocks have well-defined geometrical shapes

with defined position.

→ separate space for routing

Routing

It involves generating metal wires to connect the pin of some digital logic to the pins of some other logic.

to connect

the pin of some digital logic to the pins of some other logic while obeying manufacturing design rule.

N.B.:

Before routing is performed on the design, cell placement has to be carried out.

B Types of routing:

2 types

→ Global routing

→ Line routing
maze

→ Detailed routing

→ Channel routing
Switch box

B Global routing:

→ Generates a "loop" route

→ Each net is assigned to a set of routing reg.

→ Doesn't specify equal layout of wires

Billing to and from
different regions

eggs

Chickens

Detailed routing

- A subset of wires gets
fixed routes
- For each routing region,

each set passing through
that region, is assigned particular
routing track.

■ Routing region:



Region through which interconnecting wires are laid out.

■ Types of routing regions:



3 types

→ Horizontal channel

→ parallel to the x-axis

→ pins at their top and bottom boundaries

→ vertical channel

→ parallel to the y-axis

→ pins at their left and right boundaries

→ switchbox

→ rectangular region

→ pins to all four

sides

How to define these regions?

Ans:

Partition the routing

area into a set of

non-intersecting rectangular

regions

Types of channel junction

3 types

1) L-type

2) T-type

3) + - type

L-type: 
→ occurring at the corner of layout surface

→ ordering is not important

→ during
high level detailed routing

→ can be routed using

→ channel routing

wireless boards to app田



app田 S

L - app田

app田 - T

T-type:

→ leg of the "T" must be
routed

before the
shoulder

3rd time



app田 T

→ legs routed using
3 channel routers

+ - type: laboratory

→ more complex
B → require switchbox routing

→ require switchbox routing
- difficult

→ Advantages to convert

+ junction to T-junction

laboratory to switch



39 ft E

bind f

laboratory

switchbox

→ GND connection
bitwise

laboratory

laboratory

laboratory switchbox

bitwise

Graph model:

- used in global routing
- routing regions and their relationship
- modeled as graph

Types of graph model:

3 types

- Grid graph model
- Checker board " most suitable for area routing
- Channel interconnection graph model

most suitable for global routing

Order of routing: Regions:



1) Slicing placement topology

→ one's slice can be routed
by considering channels
in Bitwise, 2nd and 3rd in order
along wall of switch

2) Non-slicing placement topology

→ Channels with cyclic constraints
→ some of the routing
regions are to be
considered as switchbox

WTF 03/09/11

Routing Models to robot

2 types to model grids

1) Grid based model

→ A grid is superimposed on the routing regions
→ wires follow paths

along the grid lines

2) Gridless model

→ Does not follow the gridded approach

Models for multi-Layer Routing:

→ Unreserved layer model
Any net segment is allowed
to be placed in any layer

→ Reserved layer model
certain types of segments
are restricted to particular
layers

★ Two-layer $\xrightarrow{\text{HV}}$

★ Three-layer $\xrightarrow{\text{VHV}}$

$\xrightarrow{\text{HVB}}$

Testing in VLSI

Why do we need testing?

Sol:

- Possibility of errors during the design process
- Possibility of faults during fabrication / packaging
- There can even be bugs in the translation process
- Fault may occur anywhere
 - Design
 - Manufacturing

Types of defects

- {
 - Package
 - Field

→ Faults are usually costly

→ Longer ~~circuits~~ circuits

→ Dramatically increase defect rates

Binub affec. to filidies of

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ai aped 3d ress noo gisnt f

Assing mblancit sif

bes snifgo nusse form Huot f

objet Sibdego

binoboy f

Objectives of testing:

- to determine presence of faults in a given circuit/chip
- we usually use verification along with testing

Follow-up test

** Testing is used to ~~not~~ guarantee

guarantee that a circuit/chip is fault-free.

→ No amount of testing can give this guarantee

→ Using testing we can increase our confidence → in the correctness

working of the circuit/chip

↳ percentage of faults of f

→ Fault Coverage(FC)

Percent of total number
of logical faults

that can be
tested using
the help of test net

$$FC = \frac{\text{Number of detected faults}}{\text{Total number of bits for transmission}}$$

faults + strip

Bitset size

number of bits two

■ Yield (Y):

~~Brinable~~ fraction of the chips that

are fabricated which are good

$$Y = (1 - P)^n$$

where

P : probability that a
transistor is faulty

■ Defect Level (DL)

Fraction of shipped parts

that are defective:

$$DL = 1 - Y^{(1 - F)}$$

Sources of faults:

- Because of errors during the fabrication process
 - missing contact window
 - parasitic transistors
- Because of ageing
 - electron migration
 - loss of insulation
- Because of defects during packaging
 - contact degradation
 - disconnection

→ Because of ~~all~~ defects in the materials

→ surface impurities

→ cracks in the substrate

■ Parasitic transistors

→ Unwanted transistor

formation in an integrated circuit (IC) structure.

Bias

work of

multiple biasing

Types of faults:



2 types

→ permanent

→ Non permanent

Permanent

Non permanent

Permanent fault:

Fault that change the functional behavior of a chip in a time-independent way

→ Easier to detect

Ex:

design errors

incorrect connection

Non-persistent fault: can be asymptotic

a. Fault that occurs randomly
and at unpredictable times
and for "time limitation"

- ~~G1:~~
- difficult to detect
 - fault may not show up
- * On-line testing is a popular method.

Types of non-permanent faulting

best 2 types last faults

→ triaxial

→ intermittent

~~triaxial fault~~

Coupled due to environmental condition

→ loop connection

→ vertical

timing caused due to environmental conditions

→ charged particles

→ variations in pressure

→ vibration

→ temperature

Physical Failures

Manufacturing defects

→ Silicon defects

→ Lithographic problem

→ processing problem

Work out:

→ High current densities

→ Ion migration

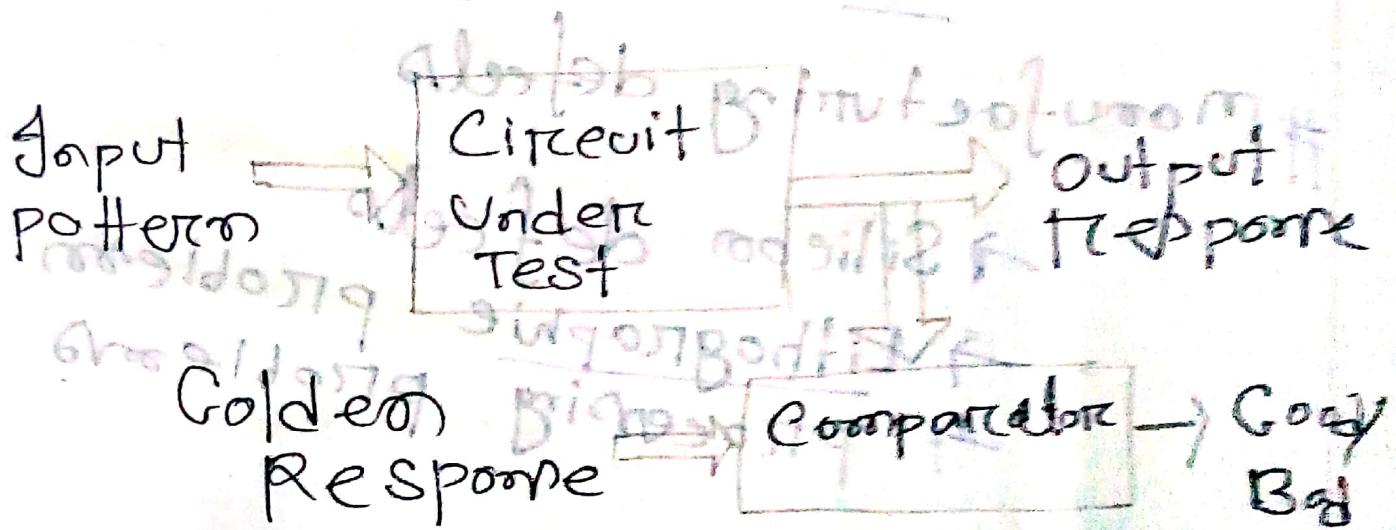
→ "Hot" electron trapping

→ Corrosion

→ failures are technology-dependent

(1960 hot - Hg - HgO)

Basic testing principle:



Process of testing

- ★ → Fault Modeling
- Test generation
- Fault simulation
- Design for testability (DFT)
- Built-in self-Test (BIST)

Fault modeling:

→ Abstract the physical defects & define a suitable logic fault model

→ Specifies the scope of test generation.

Test generation:

Given a circuit & a set of faults F . Determine a set of test vectors T

that detects all faults in F .

in T there are m test vectors

Fault simulation: Bilgeson Huot

Given a circuit,
a set of faults and
a set of test vectors.

Determine the faults in F
that are tested by the
vector int.

Design for Testability (DFT):

Formulate a set of
design rules that if followed,
results in a circuit that
will be ~~really~~ testable.

Built-in self Test (BIST)

→ Test generation and
response evaluation of
the circuits → performing
on chip

→ the chip contains itself structure

↳ has to be checked and adjusted

■ When to do testing?

Sol^a:

: after manufacturing

Can be carried out at various levels:

→ At the chip-level → when chip are manufactured

→ At the board-level

→ At the system-level

several boards are assembled together

when chips are integrated on the board

Rule of thumb

★ ★ Detecting a fault early reduces the cost of testing.

Empirical Rule:

If it is 10 times more expensive to test a device

as we move to the next higher level (chip → board → system)

Chapter 7 (B VD)

Subsystem design process

too bad software A

Shifters:

→ Table to shift increasing data
by up to $n-1$ places

→ right shift

→ left shift

→ useful for arithmetic operations

→ bit field extraction

→ Latch based shift registers

can shift only one bit

bet per clock cycle

overcome the problem
of cross bar switch

Barrel Shifter:

* A shifter that can perform n -bit shifts in a single cycle with efficient layout.

Structure of barrel shifter:

- Accepts 2^n data inputs and n control input signals.
- producing n data outputs
- selects arbitrary configuration of n bits out of 2^n input bits

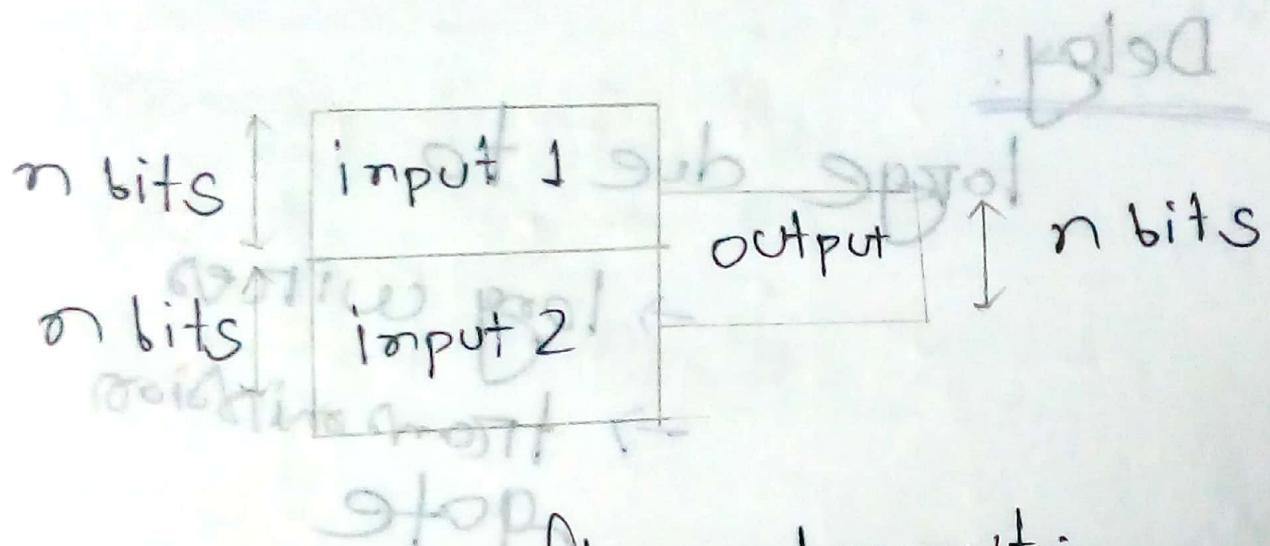
Right shift:

data into top,
into bottom

Left shift:

data into top
bottom

Rotate: ~~most 1's no signal~~
data into top & bottom
~~most 1's no signal~~



Barrel shifter layout:

- ★ → 2-D array of 2^n vertical $\times n$ horizontal cells
- input data travels upward diagonally
- output travels horizontally
- control signal runs vertically
- ★ Exactly one control signal is set to 1.

★ turning on all transmission gates in that column

Delay:

large due to

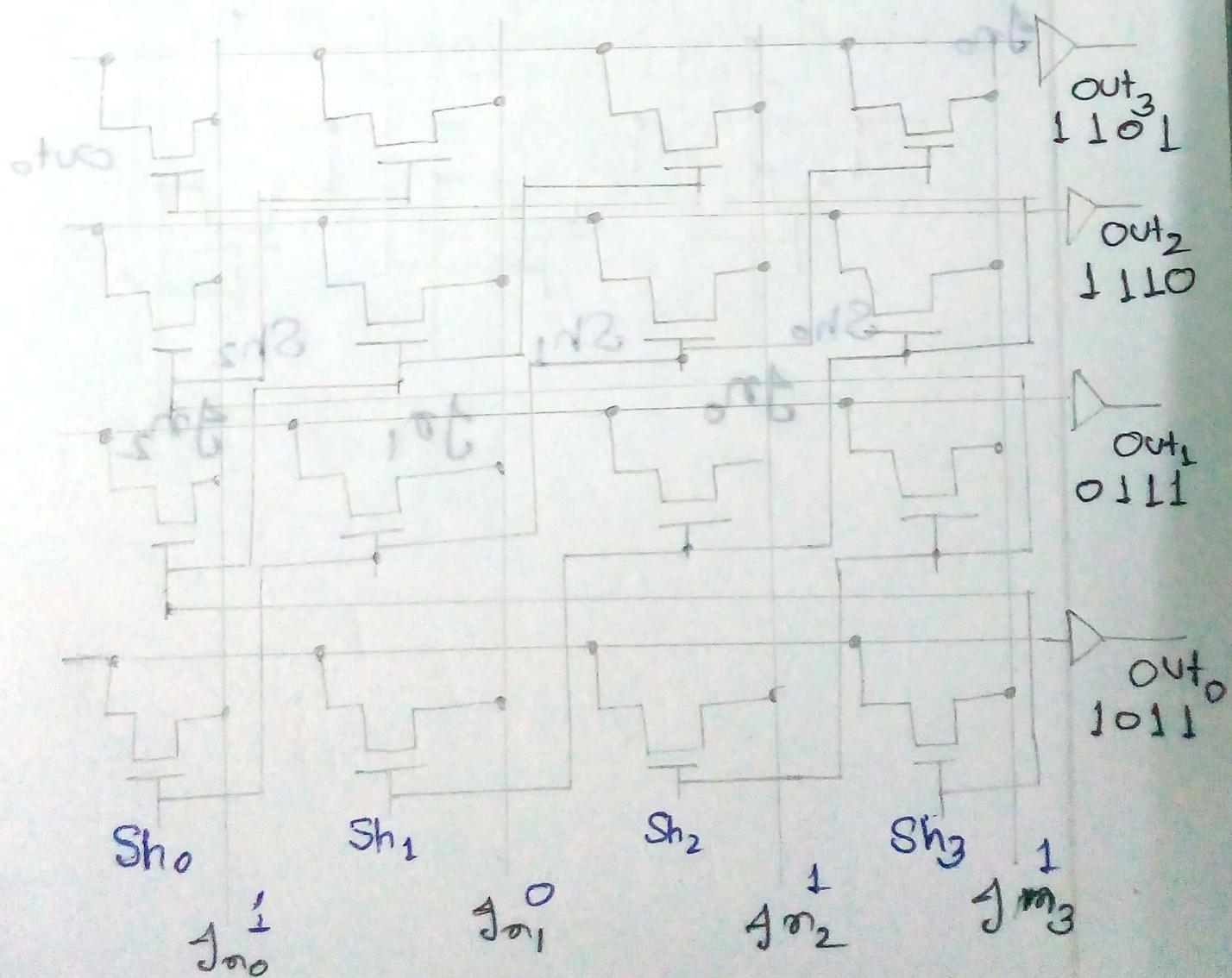
→ long wires

→ transmission gate

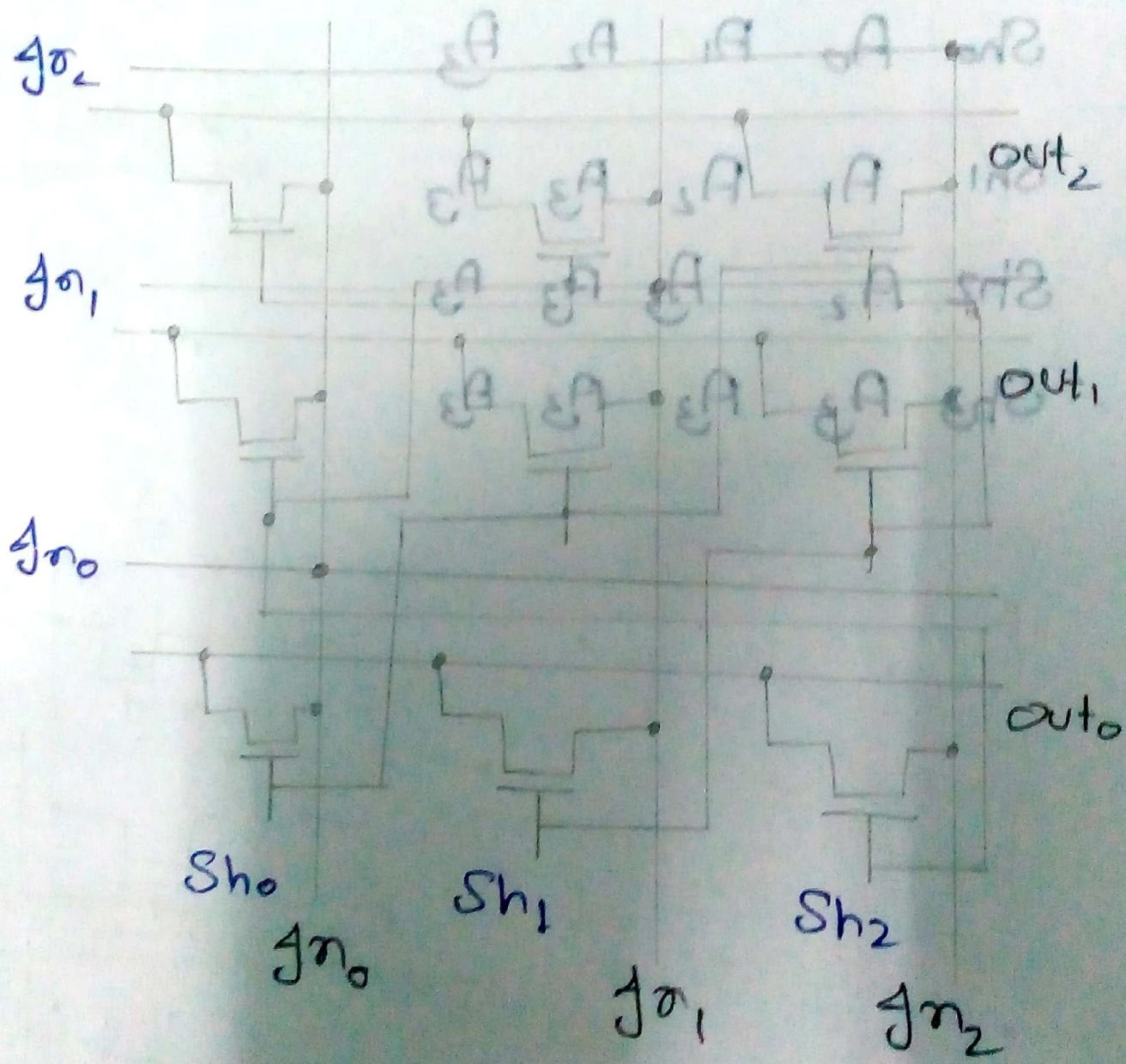
4x1 barrel shifter

B₀ B₁ B₂ B₃

Sh ₀	A ₀	A ₁	A ₂	A ₃
Sh ₁	A ₁	A ₂	A ₃	A ₃
Sh ₂	A ₂	A ₃	A ₃	A ₃
Sh ₃	A ₃	A ₃	A ₃	A ₃



3x3 bitserial Shifter



Chapter-9 (BND)

Memory, registers and

accepts of system timing

Memory organisation:

n-data input line

k address line

Memory Unit

Read

2^k words

Write

n-bits per word

n-data output line

A memory of 10 address bits and
16 data bits.

Here, $k = 10$

$n = 16$

$$\therefore \text{Memory size} = \frac{2^{10} \times 16}{1024 \times 16}$$

Memory Address memory content

Binary Decimal

0000000000	0	010100000110
0000000001	1	1101101010110

Memory Address

1111111111 1023

all 1's

10101111110101

last

negative

first

negative address

bit counter 01 to Processor A B
bit pid 01 to

Here, $k=10$
 $21=m$

21 = m
21 = n
21 = k = 10
21 = s

Types of memory

- Read-only memory (ROM)
- Random-access memory (RAM)
- volatile memory
- Non-volatile memory

Volatile memory

memory units that lose

stored information

when power is turned off

Ex:

- SRAM
- DRAM

Non-volatile memory

Memory units that retain stored information
when power is turned off

Ex: ~~Block diagram~~

→ ROM

→ PROM

↓ ~~Block diagram~~ → EEPROM

→ EEPROM

→ flash memory

↓ ~~Block diagram~~ → disk etc.

RAM • ~~Block diagram~~
DRAM •

Read-only memory (ROM)

- can perform only the memory read operation.
- Electrically or UV-erasable ROMs allow the ROM to be erased. Erasable ROMs require special processing.

Random access memory (RAM):

- can perform both read & write operations
- RAM takes the same time to access memory
- * serial memory takes different times to access information

SRAM vs DRAM



~~SRAM vs DRAM~~ ~~RAM~~

SRAM

DRAM

- 1) Consists of internal latches that stores binary information.
- 1) Stores information in the form of electric charges on capacitor.
- 2) SRAM is faster than DRAM than SRAM
- 3) SRAM is expensive 3) DRAM is cheap
- 4) It is used in coche memory 4) It is used in main memory
- 5) It is static 5) It is dynamic
- 6) The stored info. remain valid as long as power is applied to the RAM 6) Capacitors must be periodically recharged by refreshing the DRAM

Disadvantages of DRAM

SRAM

- It is expensive
- SRAM takes more size than DRAM

DRAM

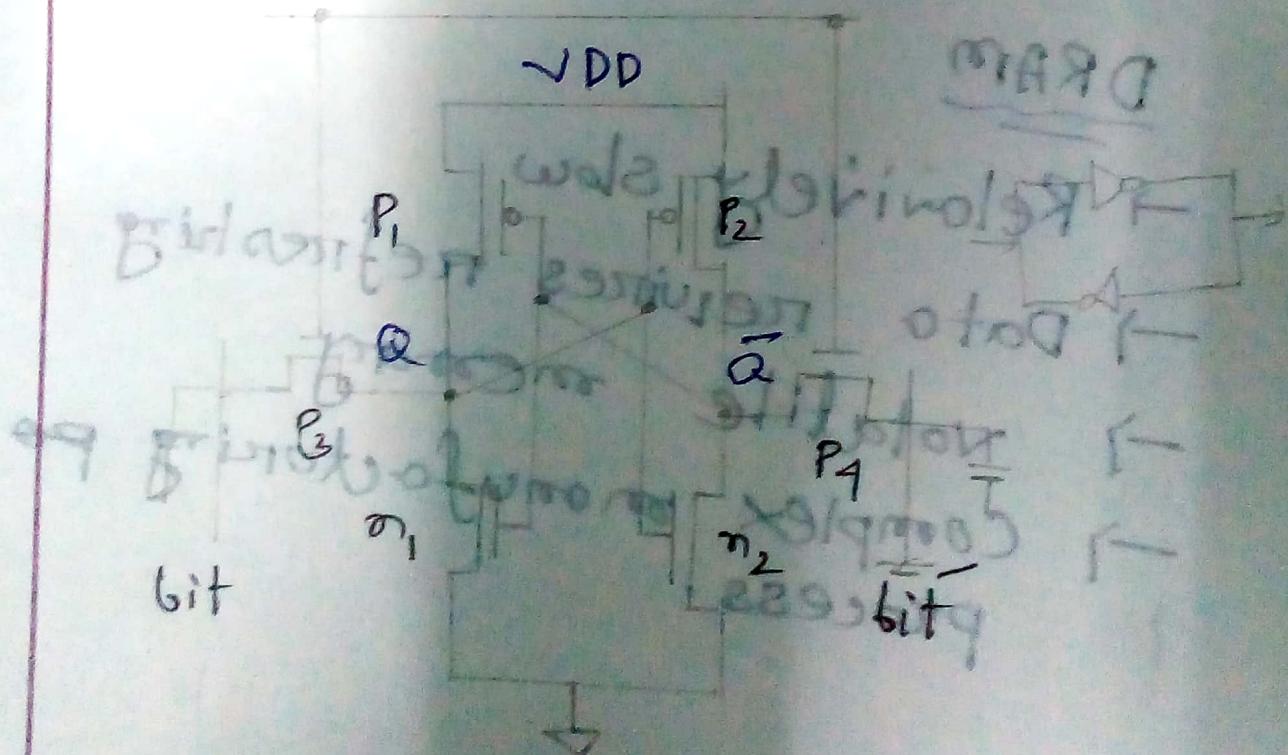
- Relatively slow
- Data requires refreshing
- volatile memory
- complex manufacturing process.

Six-transistor SRAM

★ → Core cell uses 6-transistor circuit

soft size
→ value is stored symmetrically

→ value is stored symmetrically;
only; select word (WL)



Read:

$$D^m : Q = 1$$

→ Precharge bit and bit

to VDD. 2) $C_{LP} = 1$ of

→ Set Select line

high

$$3) \text{bit}/\overline{\text{bit}} = \text{O/P}$$

4) Precharged capacitor

$$5) \overline{\text{bit}} = V_{DD}$$

→ One bit line

$$6) \text{bit} \& \overline{\text{bit}}$$

will be pulled down

Sense amplifier or
comparator

$$\overline{\text{bit}} = 1$$

$$1) \underline{m} : Q = 0 \\ \overline{Q} = 1$$

$$2) \omega_L = 1$$

$$3) \text{bit}/\overline{\text{bit}} = \text{O/P}$$

$$4) \text{Precharged capacitor} = V_{DD}$$

$$5) \text{bit} = V_{DD}$$

$$6) \overline{\text{bit}} = 0$$

Write

$$1) Q = 0 \quad \overline{Q} = 1$$

- Set bit and bit lines to desired value
- Set select line high
- 3) bit / bit \leftarrow J/P

$$4) \overline{bit} = GND$$

- 4) Drive on bit lines will flip state if necessary
- 5) $\sim \rightarrow$ Discharge

$$Q = 1$$

$$0 = Q \quad \overline{Q} = 1$$

$$1 = \overline{Q} \quad \overline{Q} = 0$$

$$I = J \quad K = P$$

$$Q = \overline{Q}$$

$$Q = \overline{Q}$$

$$I = J \quad K = P$$



One transistor DRAM:



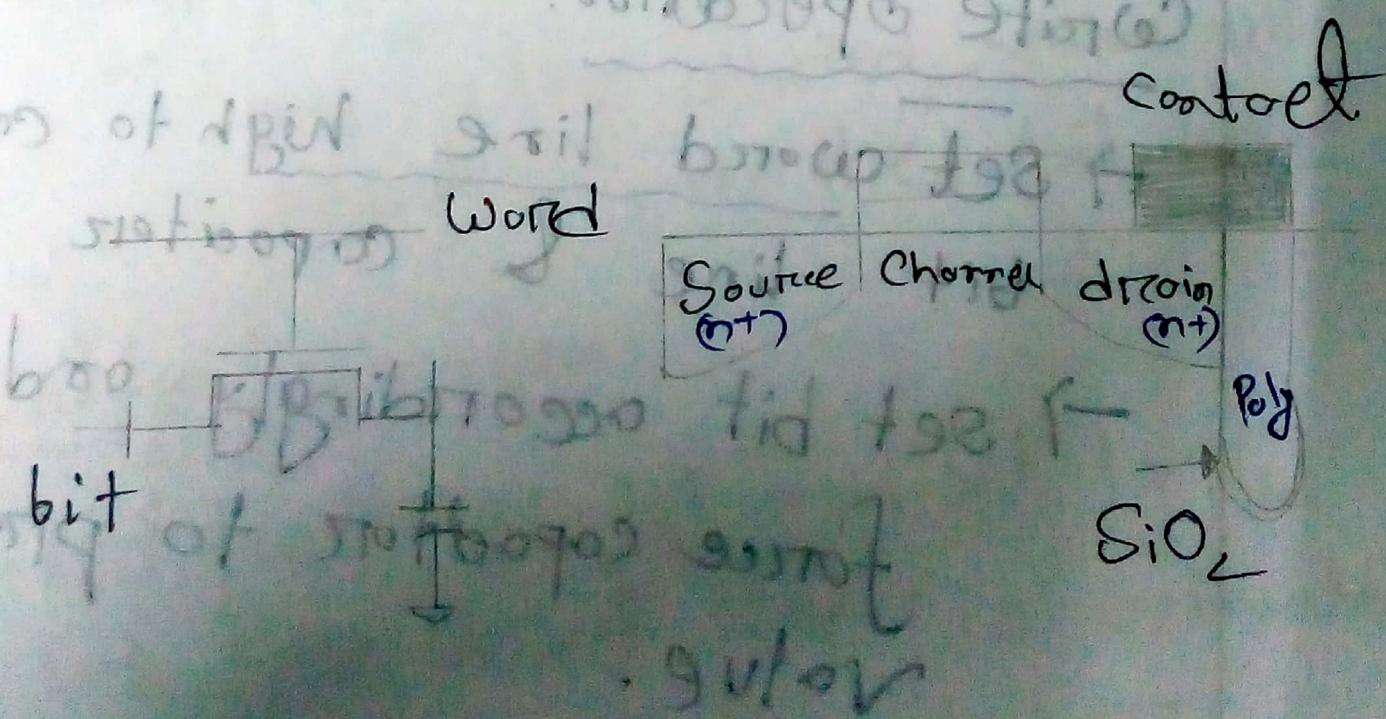
→ value is stored on a capacitor

→ DRAM loses values due to
charge leakage.

so it must

be refreshed periodically

→ popular in embedded system.



Read operation:

- Precharge bit line to Vdd
- Active word line
- The value stored on the capacitor → passed to bH line

Write operation:

- Set word line high to connect word bit line & capacitor
- set bit accordingly and force capacitor to proper value.

4 transistor DRAM

Read operation:

→ Precharge bit odd bit to V_{DD}

→ T_2 becomes on \bar{R}_{odd}
 T_1 off

→ Capacitor discharge through T_2
and the stored value will
appear in the bit line

Write operation:

→ Precharge bit odd bit to V_{DD}

→ Row select line is activated
as soon as the column
select line is activated

→ Capacitor is charged through

$T_3 \& T_4$

at T_1 → The value of the bit line is stored in the capacitor.

