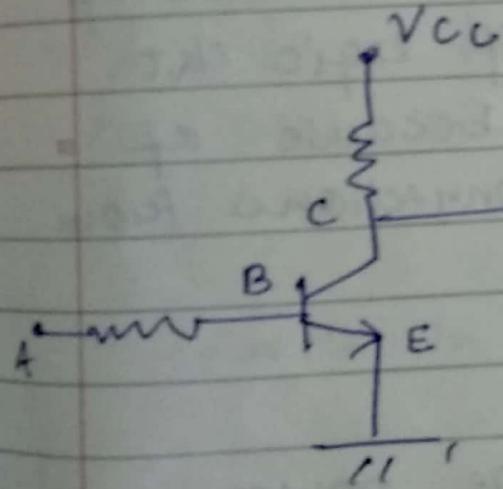


[UNIT - 5]

LOGIC FAMILIES



IC is a set of electronic ckts on one small flat piece of semiconductor material normally Si.

The IC technology has advanced in the last five decades from SSI through MSI, LSI, VLSI to GSI.

SSI \rightarrow 1 to 12 gates.

MSI \rightarrow 13 to 99

LSI \rightarrow 100 - 1000 gates.

VLSI \rightarrow 1000 \rightarrow ~~several billion~~ 10¹²

According to moore's law every 18th months tx. density will double.



SHOT ON MI A1
MI DUAL CAMERA

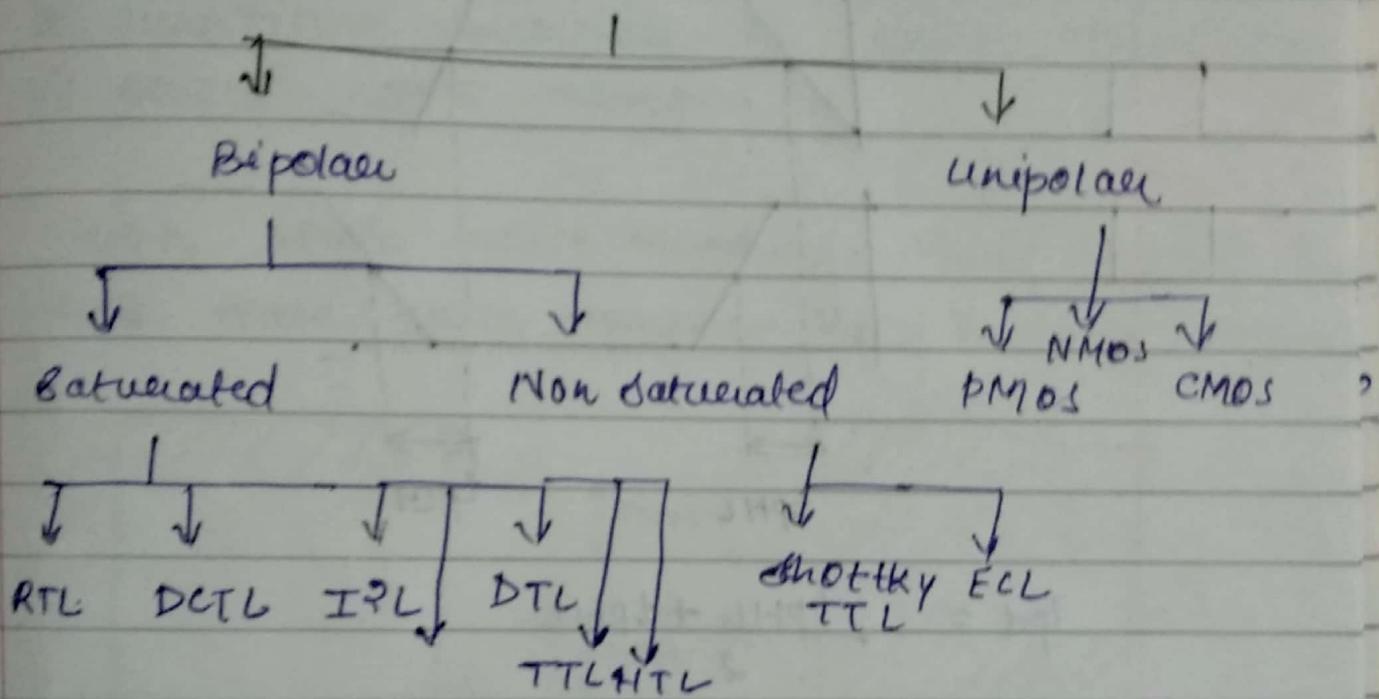
Advantages of using IC in digital system -

- 1) Reductn of the overall size of the digital ckt.
- 2) Reductn of the cost because of extremely small size of mass producing volume of similar ICs.
- 3) lower power consumption because of extremely small size of logic ckt.
- 4) Increased reliability because of reduced external interconnections from one device to another.

Disadvantage -

- 1) It cannot handle large power.
 - 2) ICs cannot easily implement electrical devices. (Inductor transformer, large size capacitors)
- In order to understand the operation of such digital systems, it is important to know the electrical characteristics of the some of the main IC logic families.

Logic Family



faster in switching - BJT

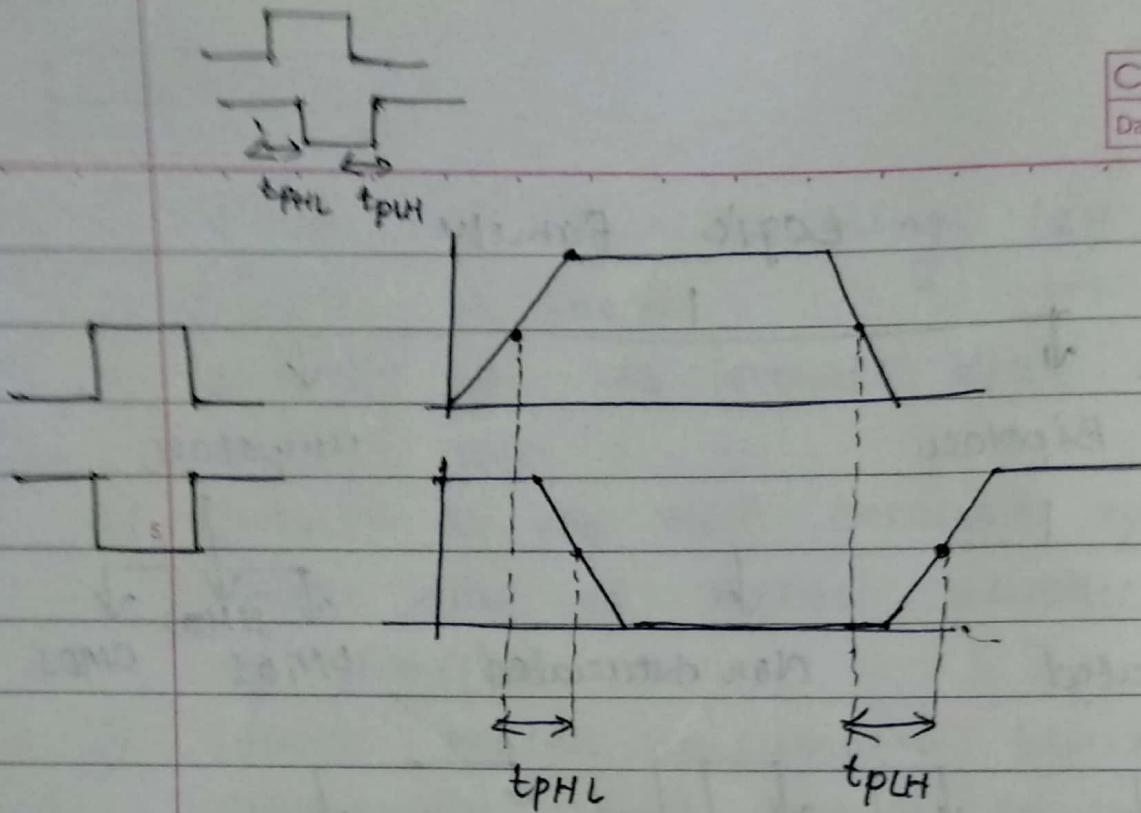
Amplifier - FET

specifications for logic families -

1) propagation delay - A logic output signal always experience a delay in going through a circuit. This delay is known as propagation delay & determines the speed of the IC.

t_{PHL} → Delay time in going from the high state to the low state.

○ t_{PSHOT} → time in going from the low state to the high state.
MI DUAL CAMERA



$$10 \quad t_{pd} = \frac{t_{PHL} + t_{PLH}}{2}$$

2) power dissipation - PD per logic gate.

$$15 \quad P_D = V_{cc} \times I_{avg}$$

(microwatts to mW)

3) figure of merit - it is defined as the product of propagation delay and PD of gate.

$$20 \quad FOM = t_{pd} \times P_D \quad (\text{nS} \times \text{mW} = \text{PJ})$$

A low value of speed power product is desirable for good IC.

4) Noise Margin - The noise immunity of a logic CKT refers to the CKT ability to tolerate noise without

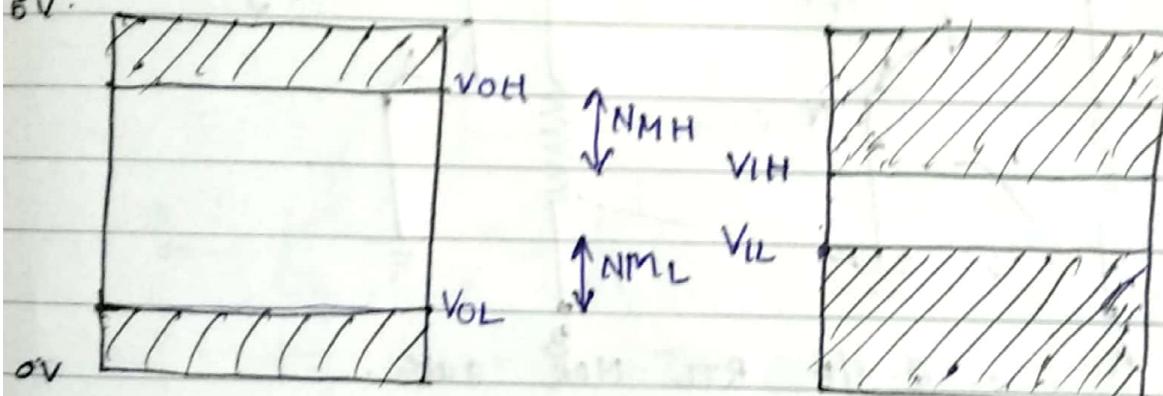
causing changes in the output voltage.

A quantitative measure of noise immunity is called noise margin.

high state noise margin - $V_{NH} = V_{OH(\min)} - V_{IH(\max)}$

low state noise margin - $V_{NL} = V_{IL(\max)} - V_{OL(\min)}$,

5V.



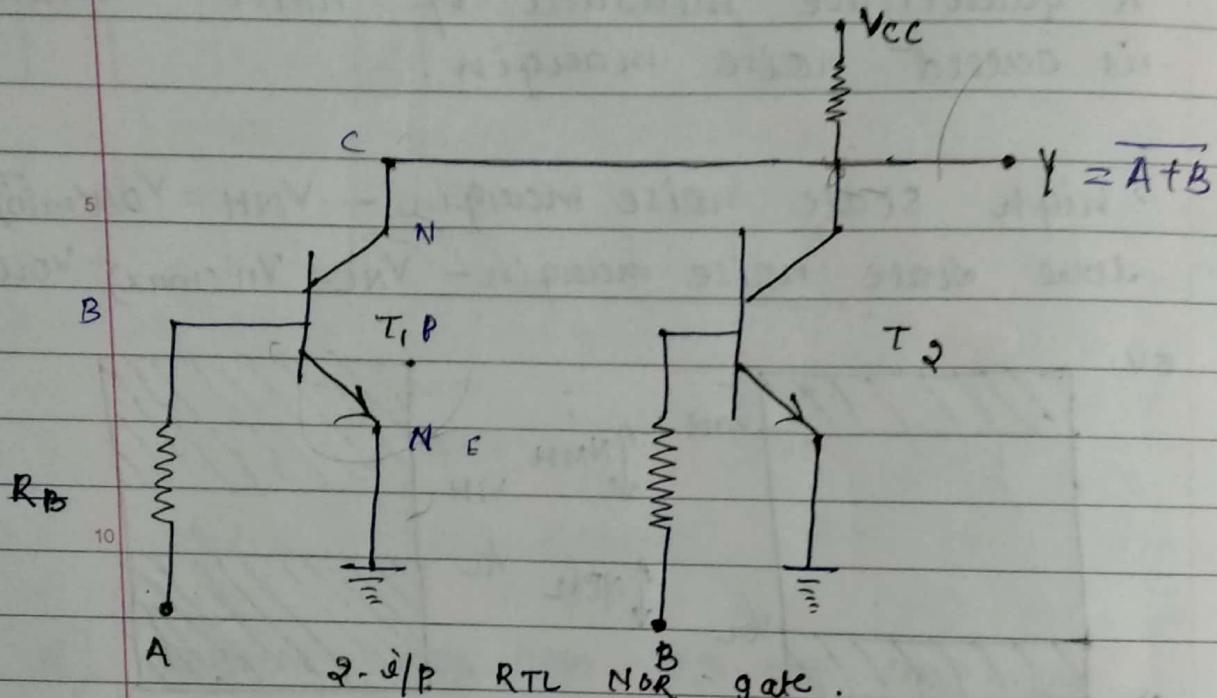
~~Do~~ 0 (0.1, 0.2, 0.3, 0.4)
1 (4.9, 4.8, 4.7, 4.6)

Fan in and fan out -

fan in represents the no. of inputs that can be connected to a logic gate.

The fanout specifies the max no. of similar logic gates which can be driven by a logic gate.

RTL (Resistor Transistor logic)



2-i/P RTL NOR gate.

A	B	T ₁	T ₂	Y
0	0	off	off	1
0	1	off	on	0
1	0	on	off	0
1	1	on	on	0

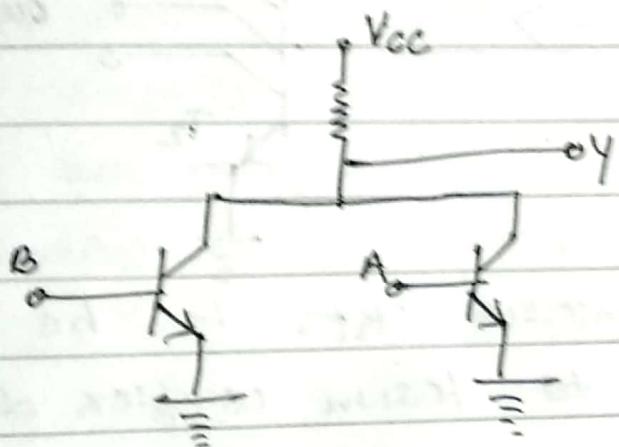
$$Y = \overline{A} \overline{B} = \overline{A+B}$$

characteristic -

- 1) Basic gate - NOR
- 2) tpd = 50ns
- 3) μ pd = 10mW
- 4) fOM = 500PJ
- 5) Noise margin = 0.2V.
- 6) fanout = 3
- 7) mixed AND logic

Disadvantage -
 low noise immunity.
 poorer fan out capabilities.
 low speed & high power dissipation.

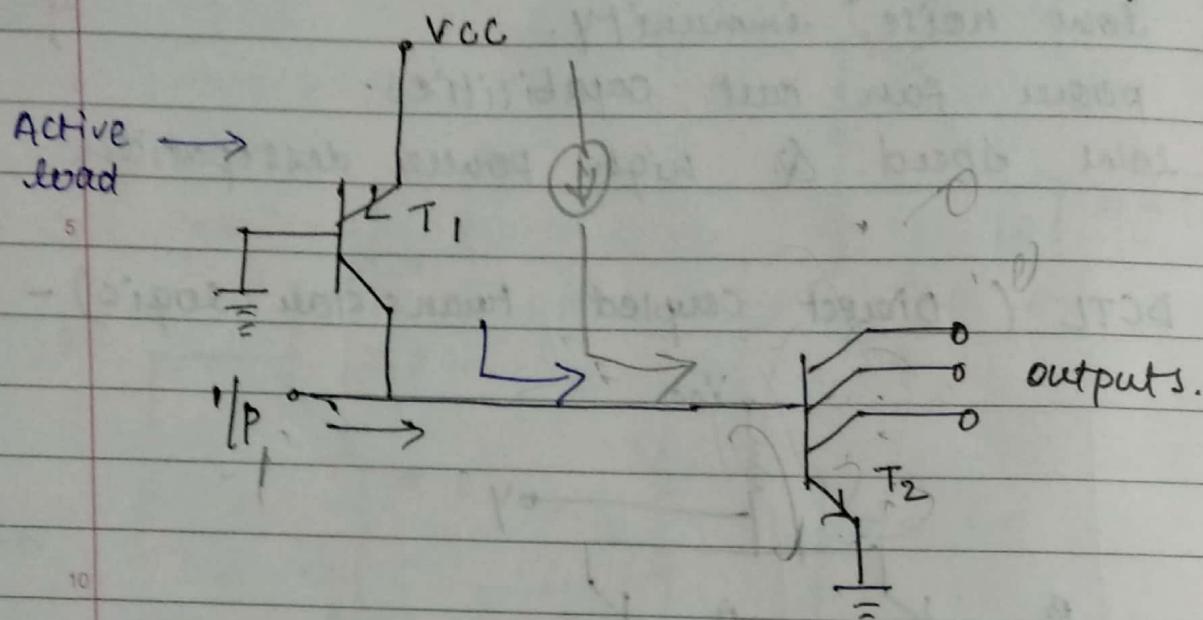
DCTL (Direct coupled transistor logic) -



A	B	T ₁	T ₂	Y
0	0	off	off	1
0	1	off	on	0
1	0	on	off	0
1	1	on	on	0

- In RTL logic family if Reg. are removed then RC time constan. decrease & speed of operation may increase.
- current hogging is there when all iff is at logic 1. during the tx. having lower VBE voltage will become on & it will not allow other

DTB IIL (Integrated Injection Logic)



This allows more ckt's to be placed in the chip to form complex digital function. hence IIL logic family is used mostly for LSI & MSI.

The IIL basic gate is similar in operation to the RTL with following modifications.

- 1) The basic structure of an IIL exhibits a single i/p and multiple o/p's.
- 2) The base Resistor which is used in RTL is removed completely in IIL
- 3) it uses multiple collectors tx instead of individual tx as in RTL.
- 4) The collection reg. in RTL gate is

replaced by npn ty. that also act as a load.

$T_1 \rightarrow$ serves as the current source.

The base ckt has a pnp ty T_1 , connected to supply voltage V_{CC} .

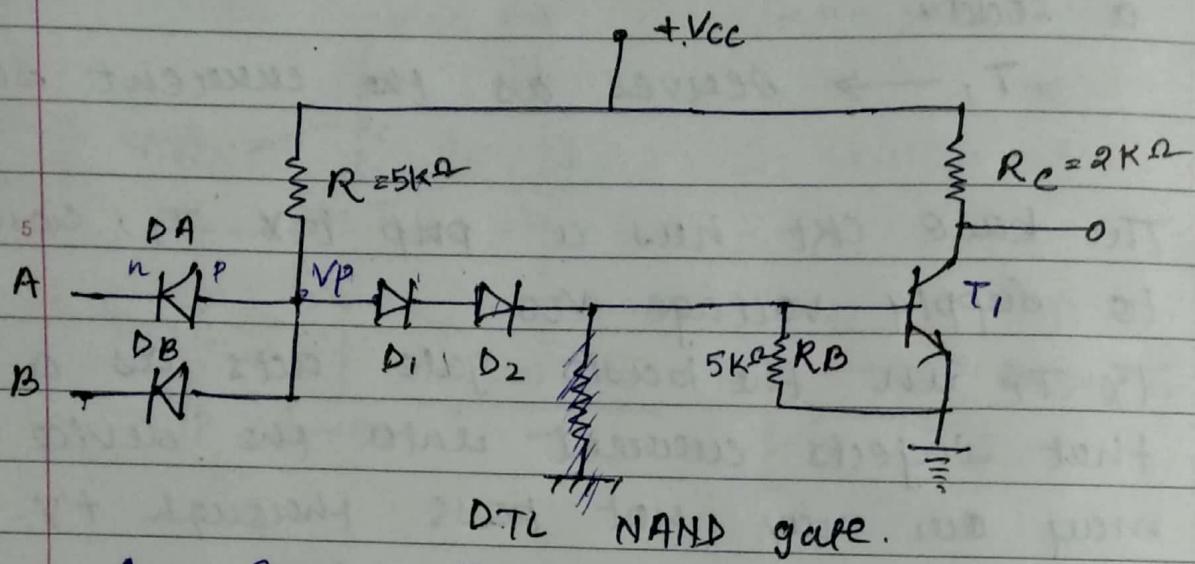
T_2 & T_1 in the basic gate acts as a load that injects current into the device which may or may not pass through ty. T_2 depending on the logic state of \bar{Q}/P .

Y_P	T_2	\bar{Q}/P
0	off	1
1	on	0

- 1) power dissipation is less
- 2) best fom compared with other logic family.
- 3) due to multicollector o/p fanout is also more.

Also known as TTL (Transistor logic)

DTL (Diode Transistor logic)



A	B	T ₁	y
0	0	off	1
0	1	off	1
1	0	off	1
1	1	on	0

$$\begin{aligned} \rightarrow V_p &= V_{BEQ_1} + V_{D1} + V_{D2} \\ &= 1.8 \text{ V} \end{aligned}$$

$$\rightarrow V_p =$$

features of DTL

$t_{pd} = 25 \text{ ns.}$

$t_{cl} = 8 \text{ mW.}$

$f_{OPM} = 240 \text{ P.J.}$

$NM = 0.75 \text{ V.}$

$\text{fan out} = 3$

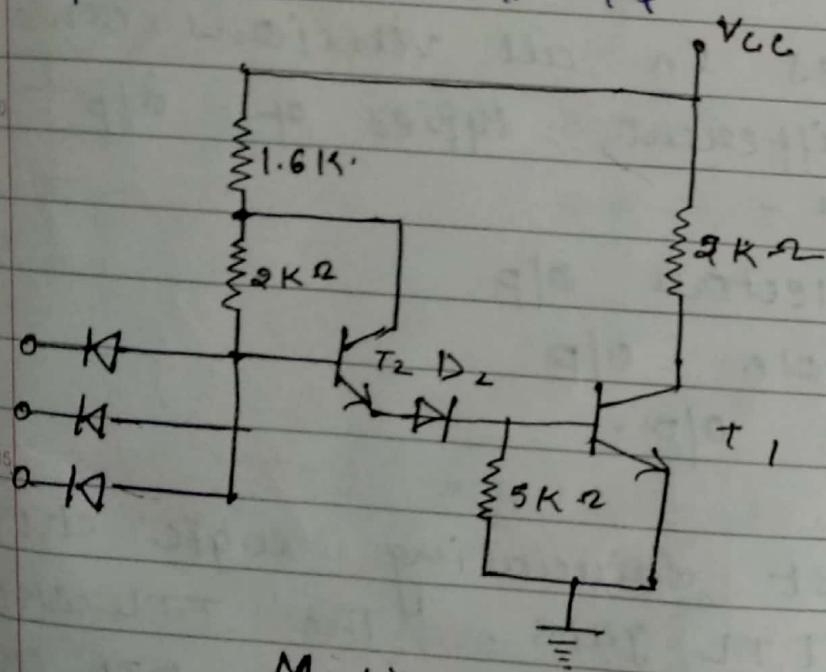
Disadvantages -

Slower speed.

Fanout =

If one more diode D_3 is connected then it may improved noise margin but it will reduce fanout.

In order to improve fanout diode D_1 is replaced with T_1 . T_2



Modified DTL

fanout = 8

TTL \rightarrow (Tri. Tri. logic)

The original basic TTL gate was a slight improvement over the DTL gate. There are many versions of the TTL basic gate.



SHOT ON MI A1
MI DUAL CAMERA

TTL (Transistor Logic) versions -

T	tpd(ns)	PD	SP(PJ)
Standard TTL	10	10	100
Low power TTL	33	1	33
High speed TTL	6	22	132
Low power Schottky TTL	9.5	2	19
Schottky TTL	3	19	57

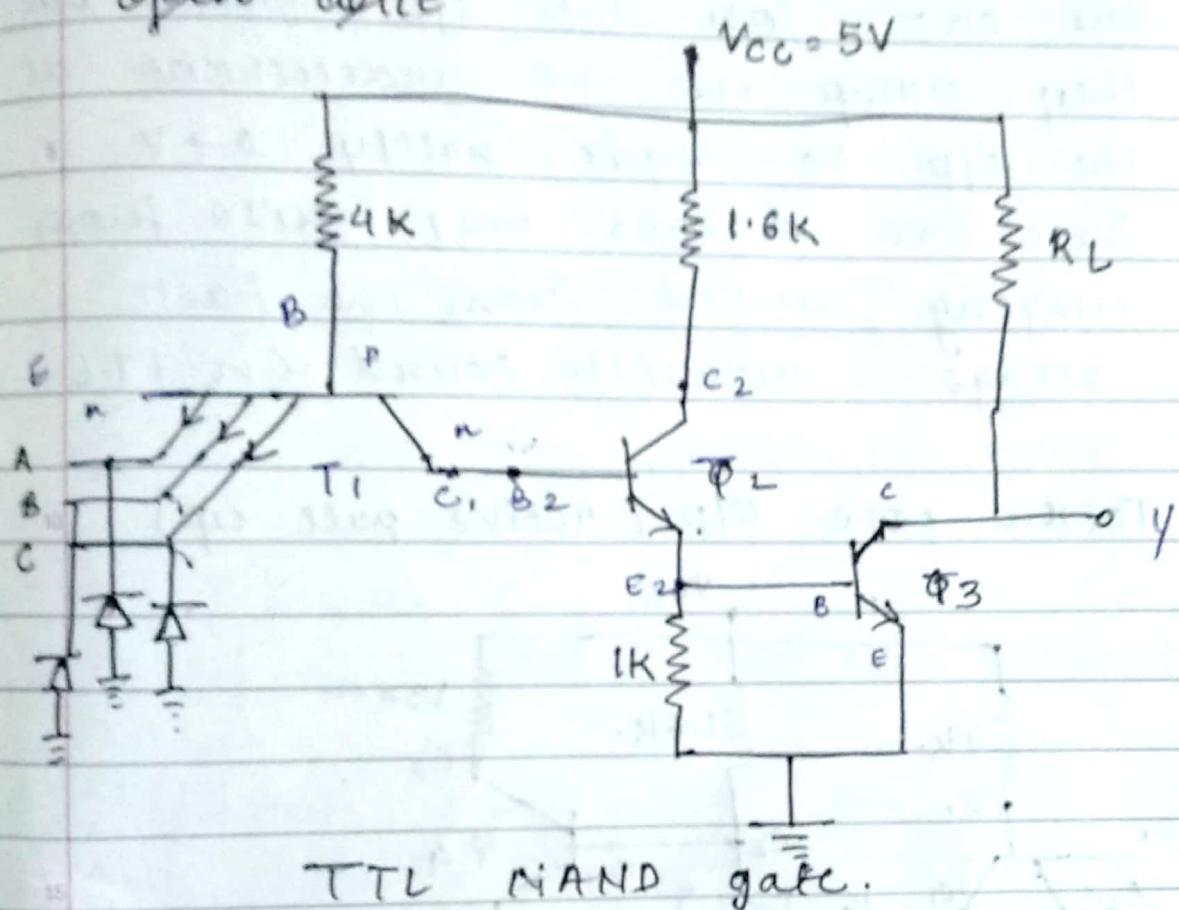
TTL gates in all versions come in 3 different types of O/P configurations -

- 1) open collector O/P
- 2) Totem pole O/P
- 3) Tri-state O/P.

The fastest saturating logic circuit is the TTL gate. The TTL circuit has the topology of the DTL circuit with the emitter junction of multi-emitter transistor Q_1 acting as the sink diodes D_A , D_B and D_C of the DTL gate and the collector base junction of Q_1 replacing the diode D_1 . Diode D_2 is replaced by emitter base junction of another transistor Q_2 .

and both CKTs have an o/p tx.

open collector



open collector TTL

A	B	T ₁	T ₂	T ₃	Y
0	0	on	off	off	1
0	1	on	off	off	1
1	0	on	off	off	1
1	1	off	on	on	0

clamping diodes.

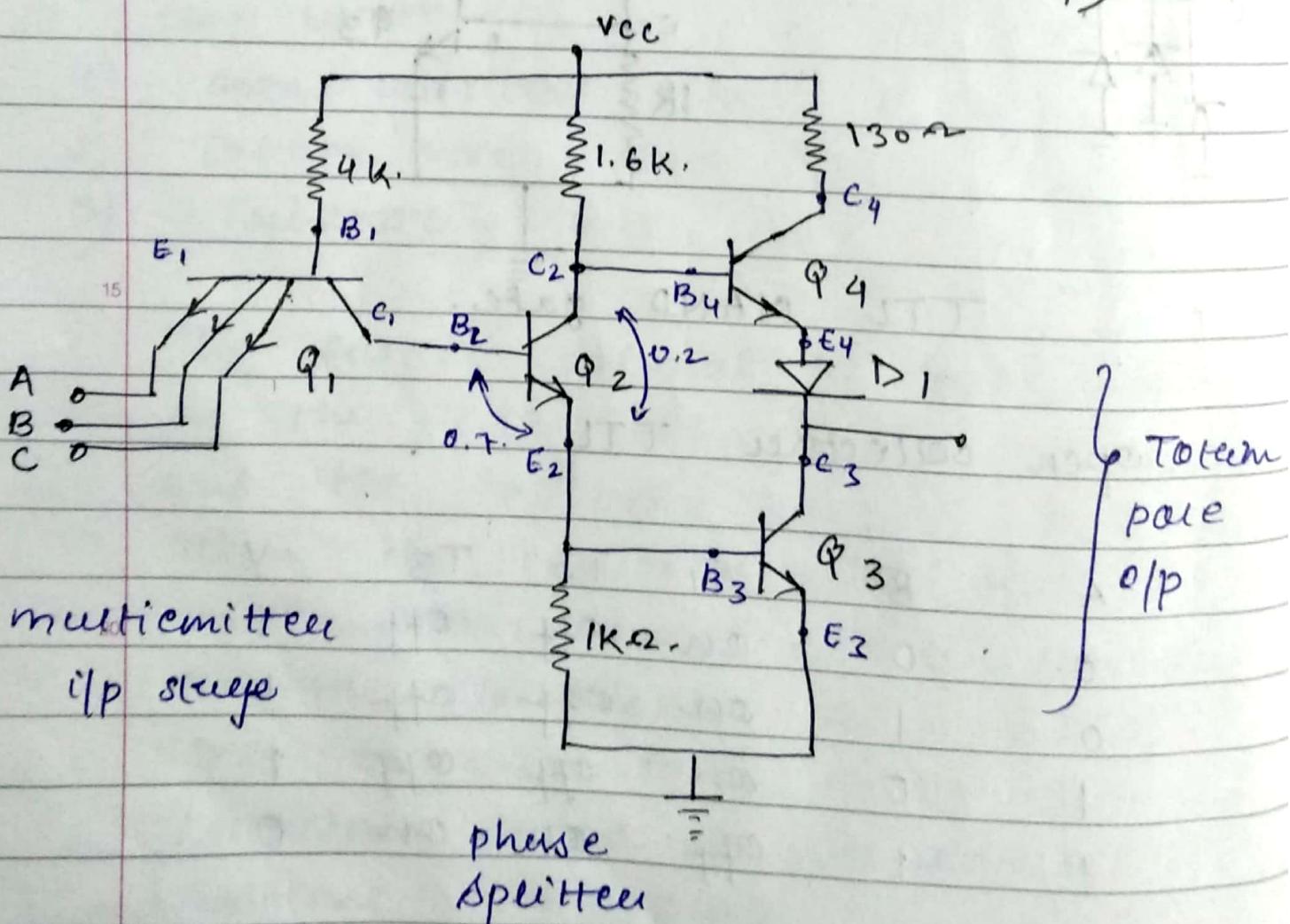
clamping diodes are often included

from each o/p to ground.

These diodes are effectively out of the CKT for +ve o/p signals, but they clamp the -ve undershoot at the o/p to approximately 0.7V.

These -ve signals may derive from ringing caused from the fast voltage transients found in TTL.

10 Totem pole o/p (Active pull up)



The ckt shown in figure is standard TTL logic family basically contains 3 stages -

- 1) multivibrator o/p stage
- 2) phase splitter
- 3) Totem pole or active pullup o/p stage.

Diode D is connected in o/p stage in order to cutoff t_{xc}. T₄ when T₃ is on.

A	B	T ₁	T ₂	T ₃	T ₄	Y
0	0	on (Active)	off	off	on (sat)	1
0	1					
1	0					
1	1	R.A.	sat	sat.	cutoff	0

hence basic gate in TTL logic family is NAND gate.

$$tpd = 10 \text{ ns.}$$

$$Pd = 10 \text{ mW.}$$

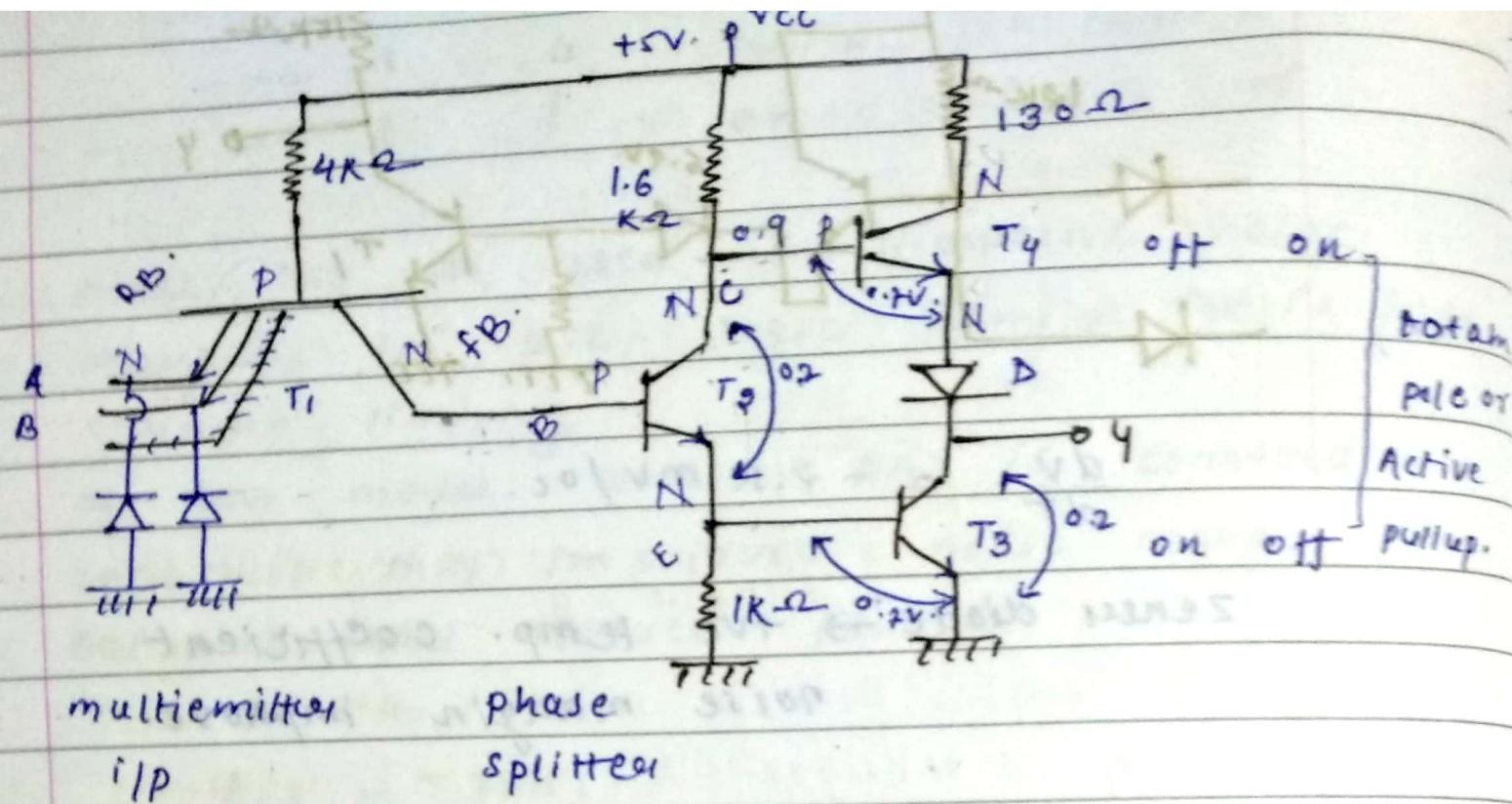
$$\text{fanout} = 10$$

$$FOM = 100 \text{ PJ.}$$

$$NM = 0.4 \text{ V.}$$

Advantage -

- 1) high speed of operation
- 2) fanout also more
- 3) Pd less.



multiemitter i/p phase splitter

The ckt shown in figure is standard TTL logic family. It basically contains 8 stages. 1st is multiemitter i/p stage, 2nd is phase splitter & 3rd one totem pole or active pullup o/p stage.

A	B	T_1	T_2	T_3	T_4	Y
0	0	A	C	C	S	1
0	1	A	C	C	S	1
1	0	A	C	C	S	1
1	1	R	A	S	S	0

operation of TTL logic family -

In the ckt shown in figure if any one of the input is low then emitter base junction of transistor T_1 is in FB & collector base junction is RB. due to this tr. T_1 is in active mode. T_2 & T_3 is in cut off & T_4 is in sat. & o/p is logic 1.

When all ip are logic 1 then emitter base junction of tr. T_1 is in RB & collector base junction is FB due to this tr. T_1 is in RA mode, T_2 & T_3 are in saturation whereas T_4 is in cut off & o/p is logic 0.

hence basic gate in TTL logic family is NAND gate.

t_{pd} - 10ns.

P_{diss} - 10 mW.

fanout - 10

fOM - 100 pJ.

NM - $0.4V$ / $V_{TH} = 0.4$, $V_{IH} = 0.0V$.

$V_{IL} = 0.8V$, $V_{OL} = 0.4V$)

Advantage of totam pole state -

- 1) high speed of operation.
- 2) fanout also more.
- 3)

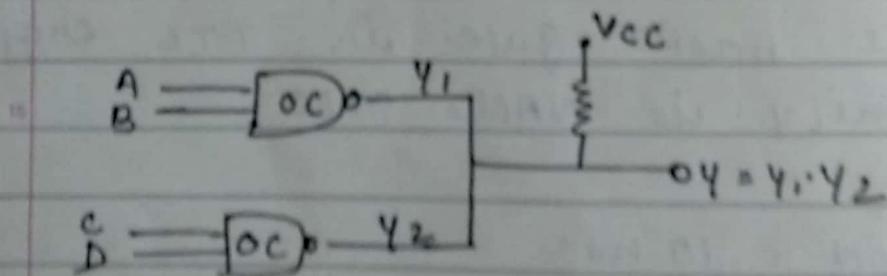
SHOT ON SONY A1

MICRO PICTURE STAGE IS NOT USED FOR ALIEN AND OPERATOR.

Wired logic -

When 2 totem poles are tied together with the top one gate is high while that for a second gate is low the excessive amount of current drawn can produce enough heat to damage transistors in the ckt. hence wired logic must not be used for totem pole o/p ckt bcoz of current spikes problem.

TTL ckt with open collector o/p are available which can be used for wired AND logic.



- In TTL logic family if resistance value decreases then RC time constant decreases & speed of operation increases & resulting logic family is known as high speed TTL.
- To provide logic polarity TTL resistance value decreases.

SHOT ON MI A1
MI DUAL CAMERA

Schottky diode is used in TTL logic family to increase speed of operation of Schottky diode is placed blue base and collector junction it will remove storage time or saturation delay due to this propagation delay of Schottky TTL is 3 ns.

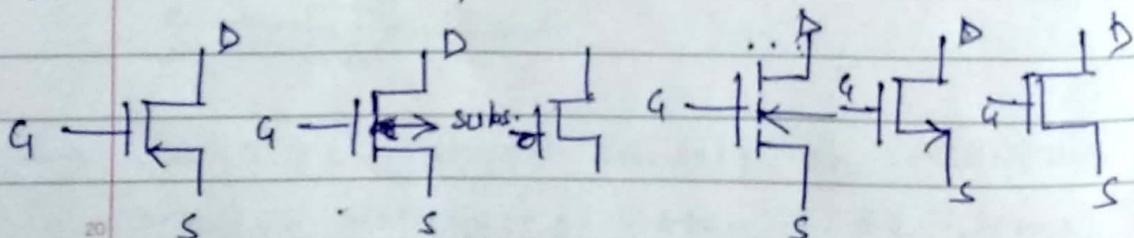
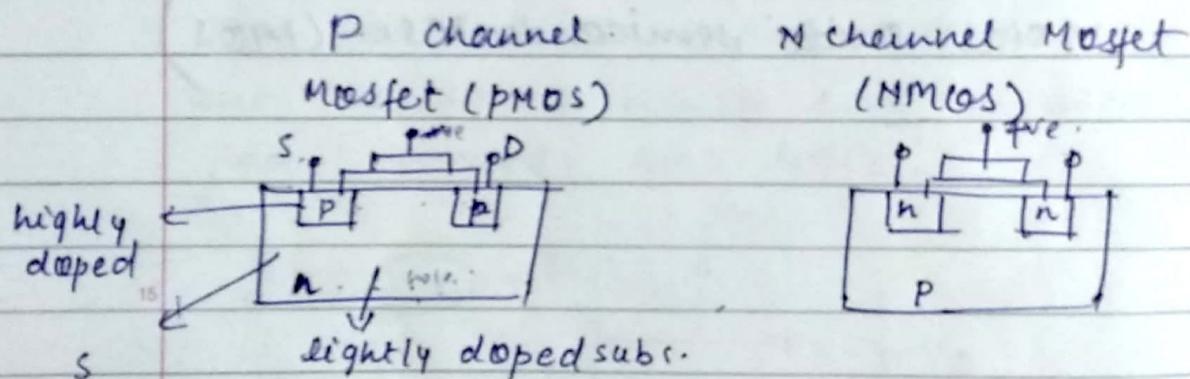
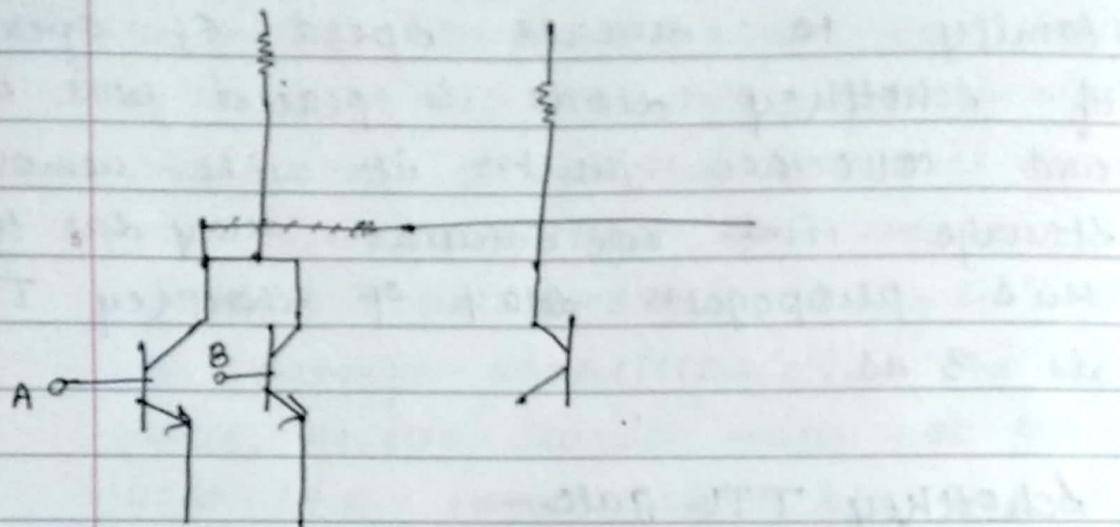
Schottky TTL gate -

Metal Oxide semiconductor-(MOS)



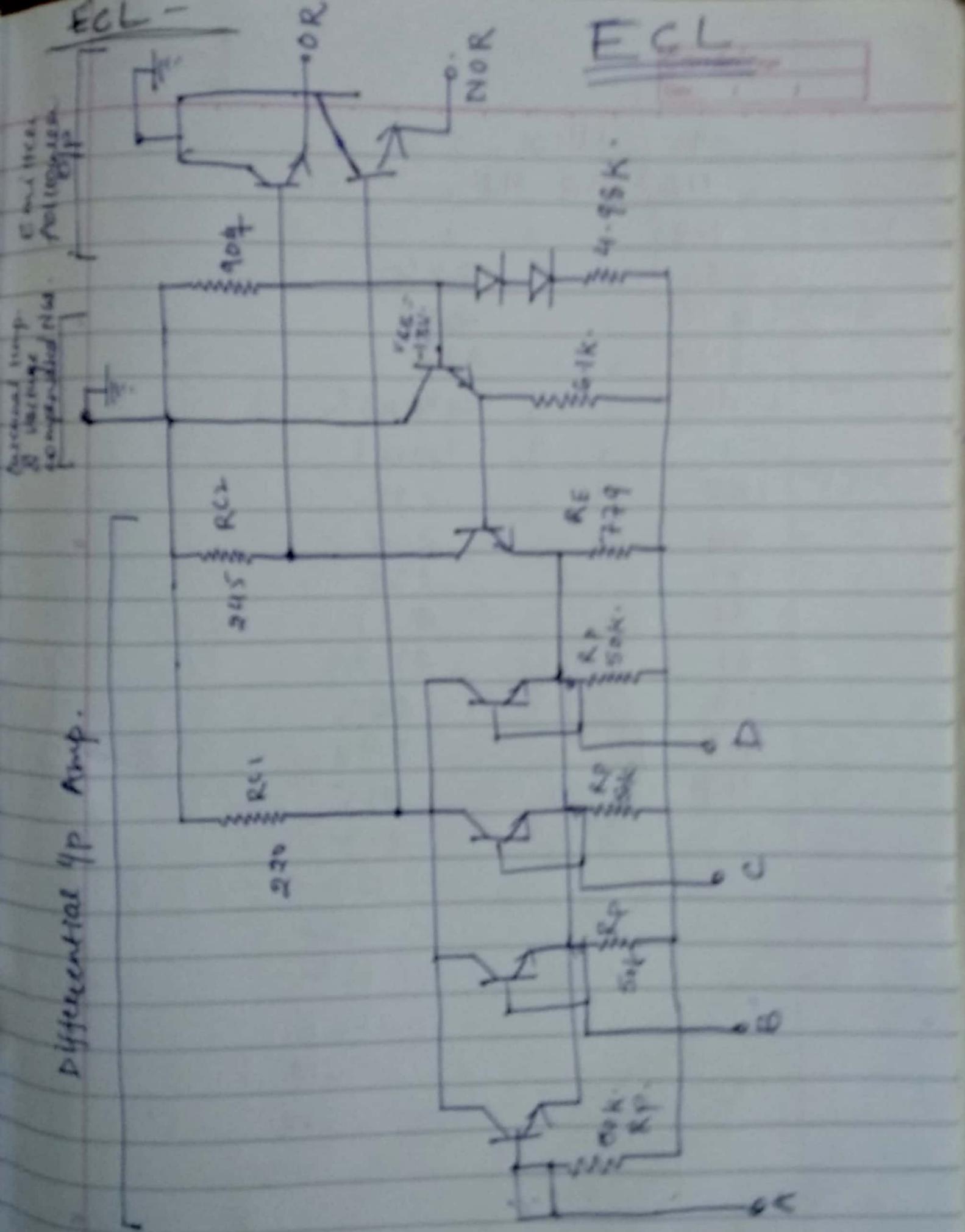
SHOT ON MI A1
MI DUAL CAMERA

Emitter coupled logic -



-Ve (0 logic) \rightarrow on
+Ve (logic 1) \rightarrow off

NMOS \rightarrow (logic 0)-off
logic 1-on.



SHOT ON MI A1

fastest logic family.

ECL logic family contain 4 stages -

differential emitter amp i/p stage.
common collector out emitter follower,
o/p stage.

due to use of differential amp. comp.
o/p are available in ECL logic family.

→ ECL have basic gate NOR TOR gate.

→ due to use of CC O/P fanout is more.

→ propagation delay is 1 nsec.

→ power → 55 mW.

→ fanout = 25.

ECL
RTL } open-'0'
DCTL

TTL
DTL } → open-'1'
HTL

ECL uses -ve power supply due to this
any power supply ripple or noise or
spikes or even glitches will not effect
operation of ECL gate.

$$V_{OL} = -1.7V$$

$$V_{IH} = -1.1V$$

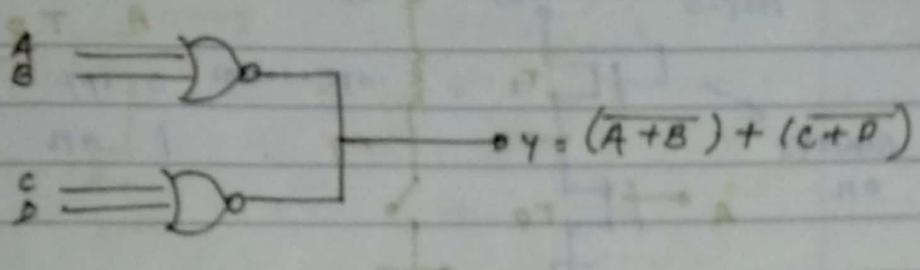
$$V_{IL} = -1.4V$$

$$V_{OH} = -0.8V$$

NM of ECL is 0.3.

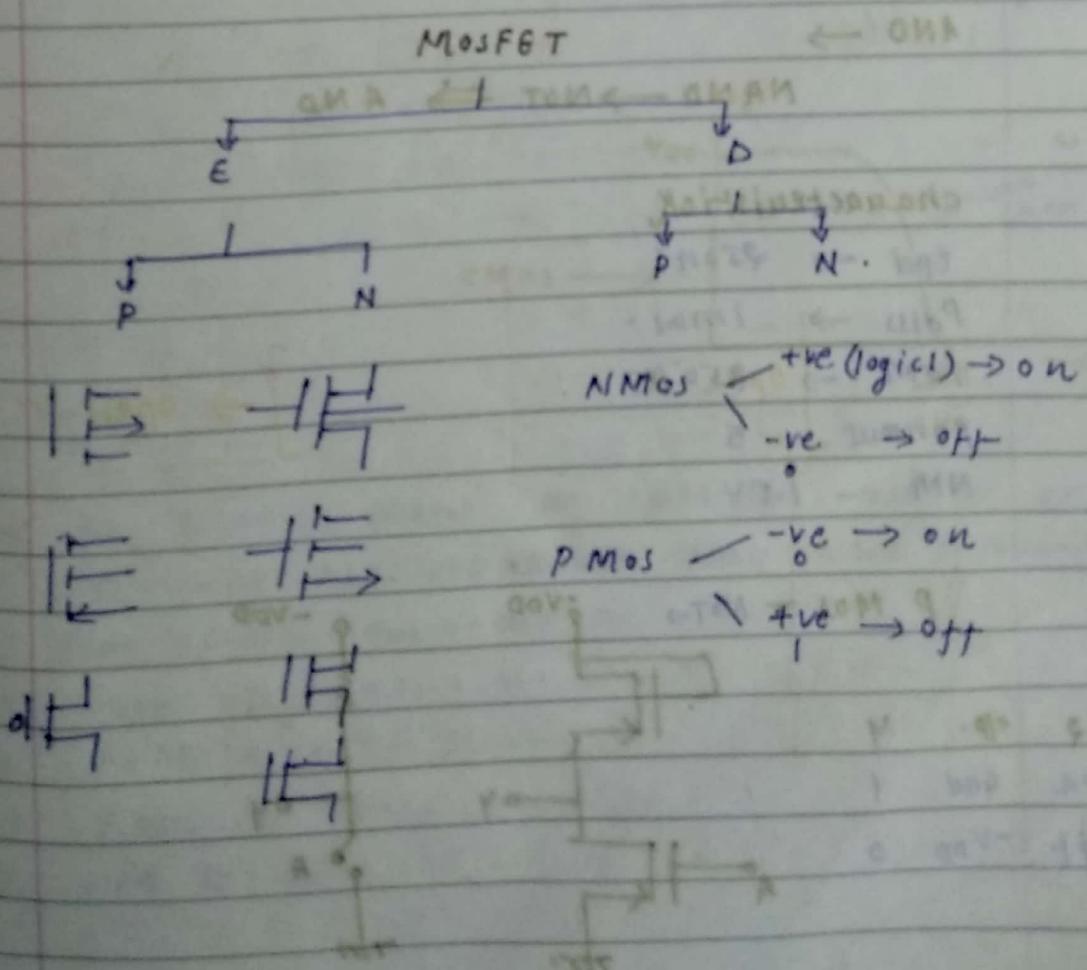
SHOT ON MI A1
MI DUAL CAMERA

→ ECL logic family provide inverted OR operator



ECL is known as current mode logic family.
(CML).

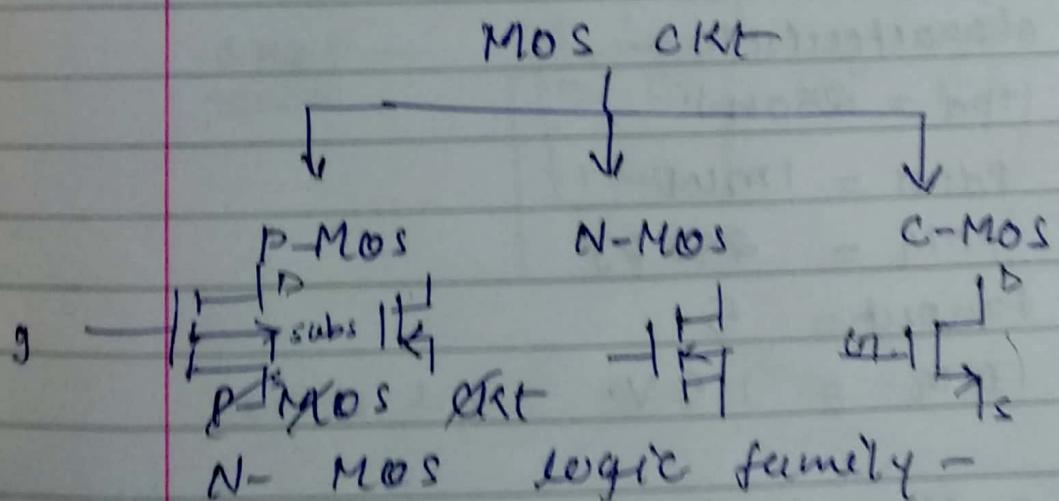
- higher speed of operation.
- fanout is more.
- power dissipation more.
- voltage levels are not compatible with other logic families.



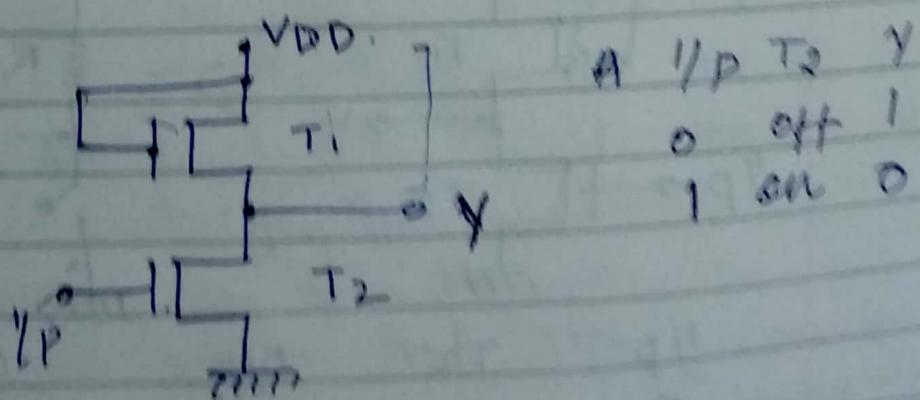
SHOT ON MI A1
MI DUAL CAMERA

Advantages of MOS IC

- 1) The MOS IC is relatively simple & inexpensive to fabricate.
- 2) The MOS device size is small and it consumes less power.
- 3) The MOS ICs can accommodate a much larger no. of ckt elements on a single chip.



- 1) NOT gate -



SHOT ON MI A1
MI DUAL CAMERA

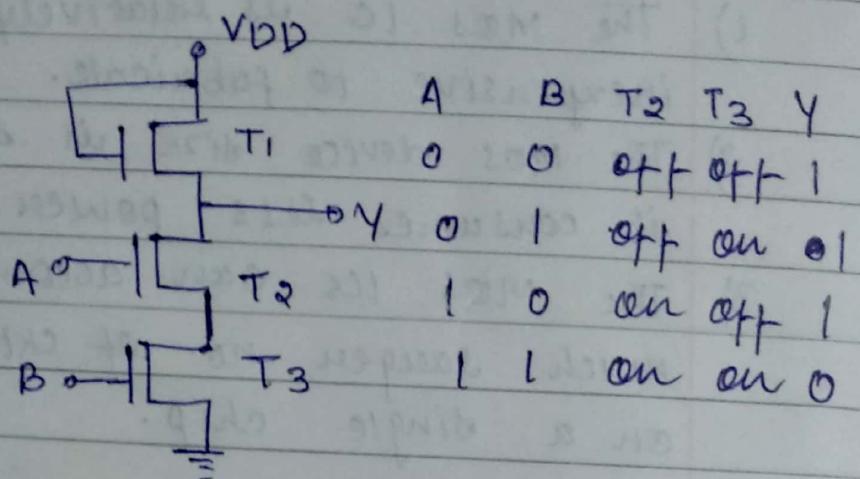


Q'

NAND gate -

A·B

A+B



characteristic -

$t_{pd} = 250\text{ ns}$.

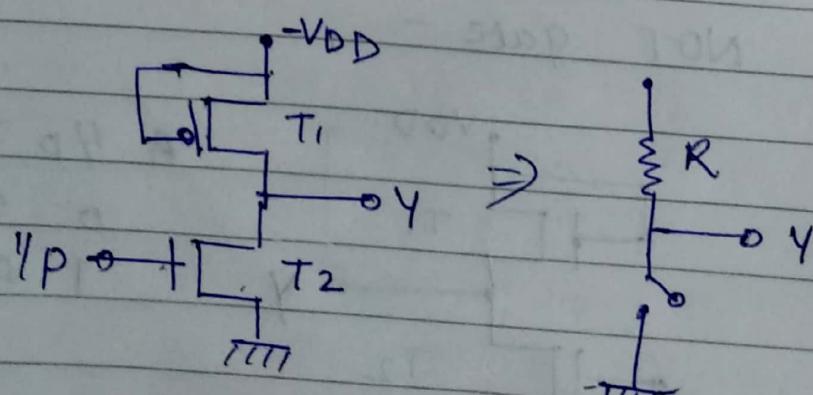
$P_{diss} = 1\text{ mW}$

$f_{OM} = 250\text{ PJ}$

Fanout = 5

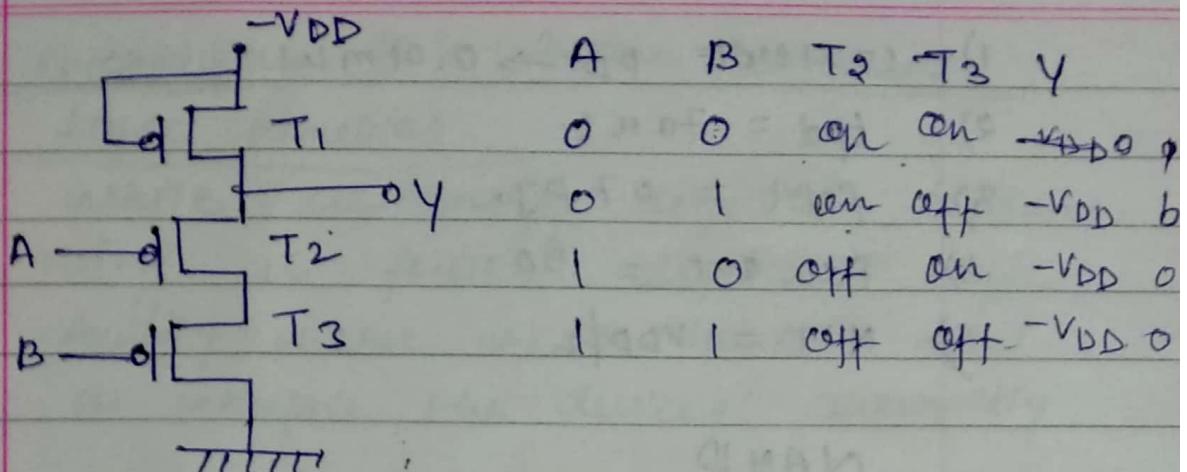
$V_M = 1.5\text{ V}$.

P-MOS logic family -

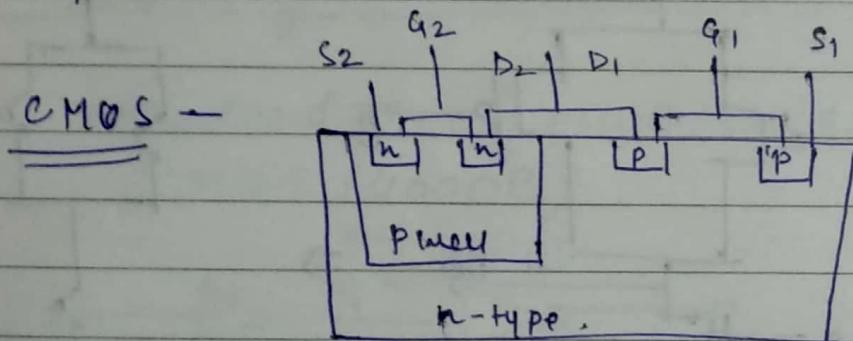


Y _P	T ₂	O/P	Y
0	on	-V _{DD}	0
1	off	-V _{DD}	0

SHOT ON MI A1
MI DUAL CAMERA

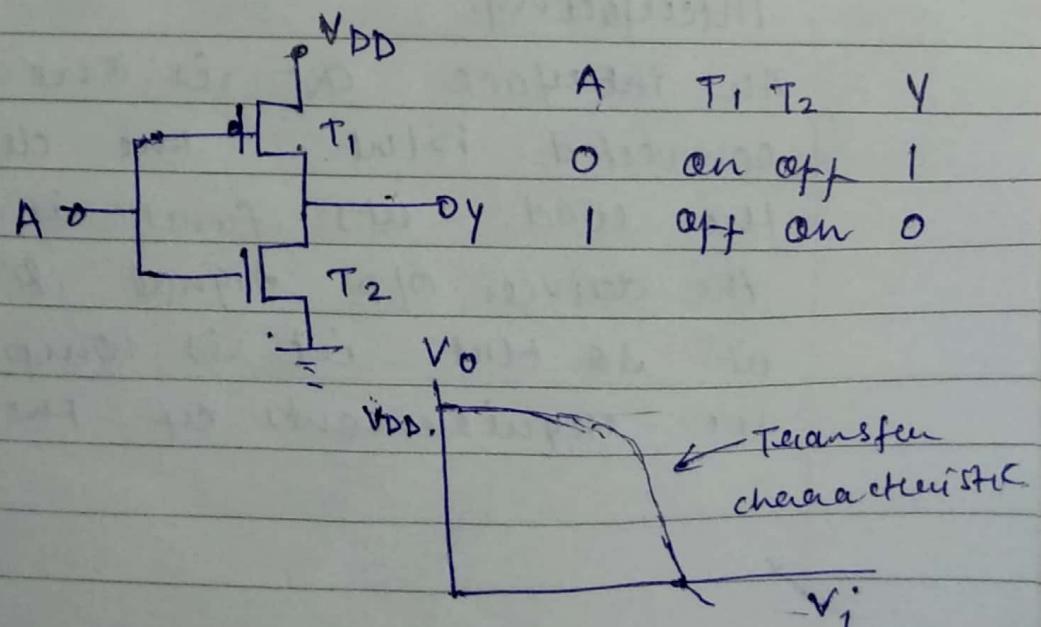


$$t_{pd} = 300 \text{ ns.}$$



cmos logic gate ckt \rightarrow

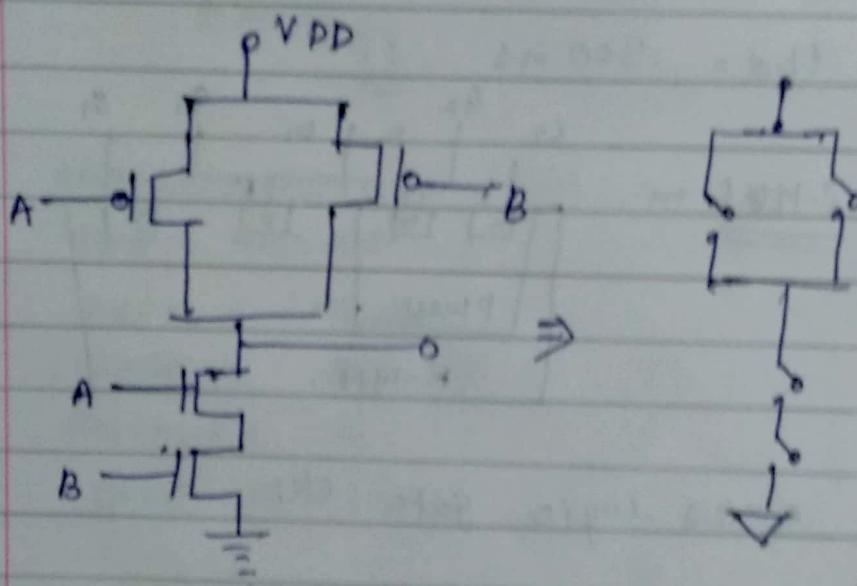
~~NAND~~ NOT gate -



SHOT ON MI A1
MI DUAL CAMERA

- 1) convert $p_D \rightarrow 0.01 \text{ mJ/L}$
- 2) $t_{PD} = 70 \text{ nS.}$
- 3) $f_{OM} = 0.7 \text{ PJ.}$
- 4) $\text{fan out} = 50.$
- 5) $N_M = V_{DD}/2$

NAND



Interfacing.

An interface ORT is one that is connected b/w the driver and the load. Its function is to take the driver's o/p signal & condition it so that it is compatible with the requirements of the load.



SHOT ON MI A1
MI DUAL CAMERA

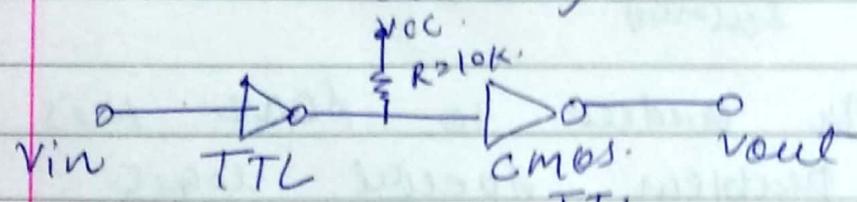
Interfacing ICs from different logic families -

While designing digital systems using IC from different logic family, there is a strong need to interface the devices correctly.

Interfacing TTL to CMOS

Standard TTL (7400 series)

CMOS (4000B)



max. logic level o/p of 0.4 V

max. —————— CMOS = 1.5 V .

TTL @ high level o/p $\rightarrow 2.4 \text{ V}$.

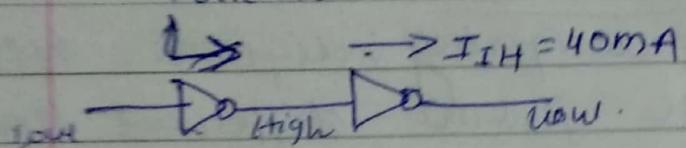
CMOS expects $- 3.5 \text{ V}$. ↓

unacceptable.

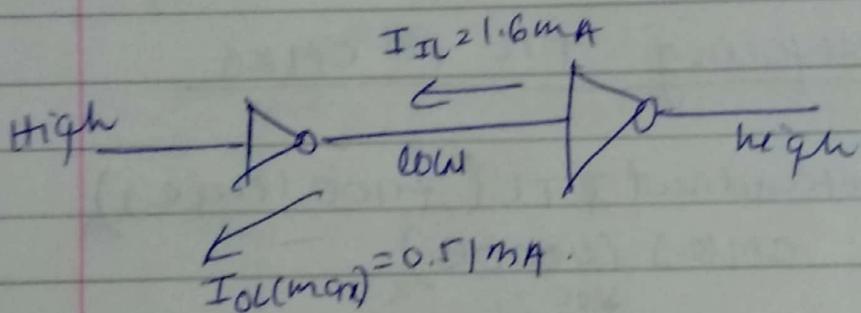
This problem is solved by connecting a resistor between CMOS & V_{CC}

CMOS TO TTL (Voltage level are no problem)

$$I_{OH(\text{max})} = 0.51 \text{ mA}$$



4069B 7404
CMOS TTL



In order to solve this problem special logic device buffer have been designed buffer can provide high output when required.

Level Shifting.

There is another problem that arises when we interface logic gates from the IC logic families that have different supply voltages.



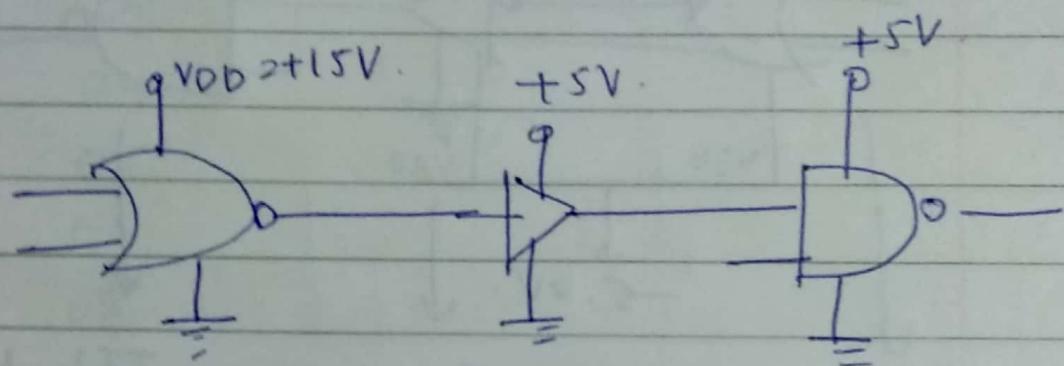
SHOT ON MI A1
MI DUAL CAMERA

CMOS (4000B)

\downarrow
 $+3V$ to $+15V$.

ECL

\downarrow
 $-5.2V$.



2000
 \downarrow

8192

2014

\downarrow

8222

8192
31

2000

3×16

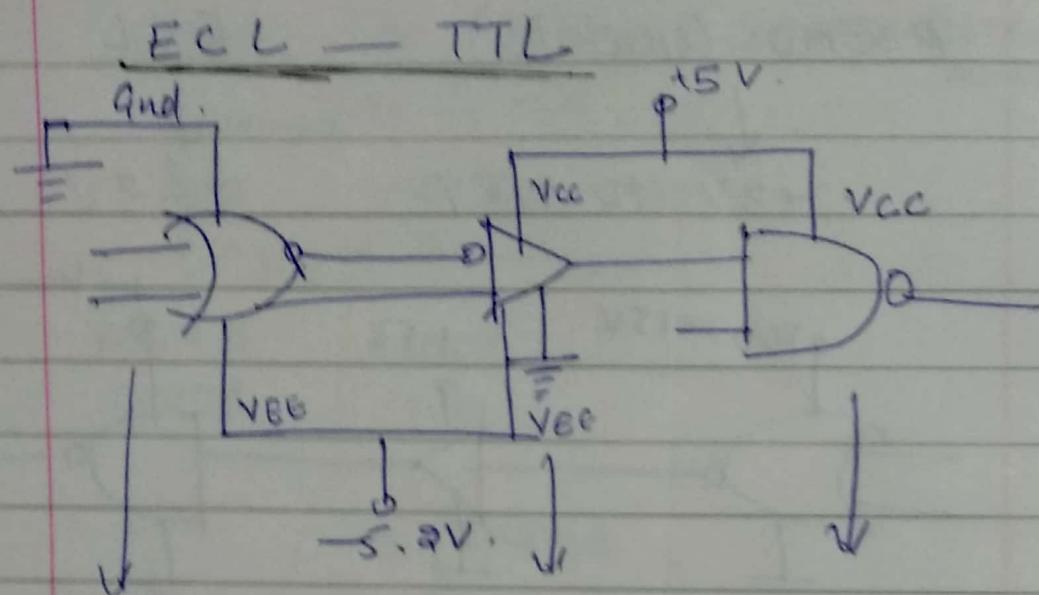
2×16^5

$$2 \times 16^3 + 16^1 = f(x)$$

$$4096 + 16 + 15$$

$$4096 + 31$$

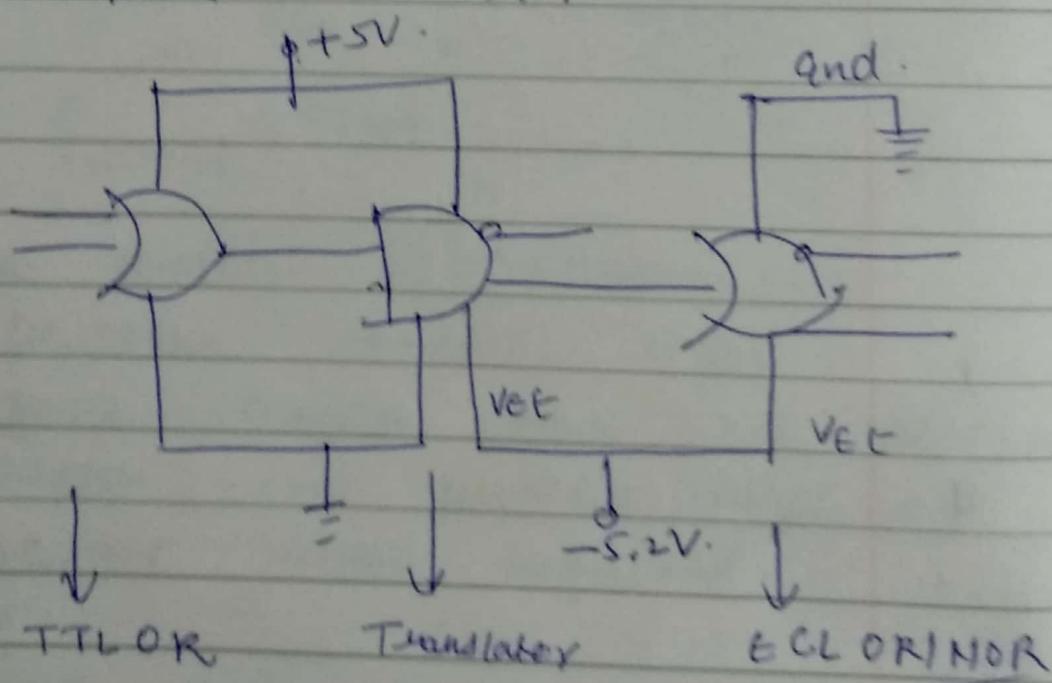
SHOT ON MI A1
 MI DUAL CAMERA



ECL OR/NOR

Translator.

TTL NAND



TTL OR

Translator

ECL OR/NOR