ES Examination

Exam: End-Sem_Exam_DEC-2020_CS3CO29_Digital Electronics

Digital Electronics (T) 0/60

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Not Answered
Which of the following best describes the action of pulse-triggered FF's?
A. The clock and the S-R inputs must be pulse shaped.
❷ B. The data is entered on the leading edge of the clock, and transferred out on the trailing edge of the clock.
C. A pulse on the clock transfers data from input to output.
D. The synchronous inputs must be pulsed.

The output is false only if all the inputs are true, which gate is this?

A. NOR

❷ B. NAND

C. EXOR

D. EXNOR

Which logic family has highest fan out?

A. DTL

B. TTL

C. ECL

❷ D. CMOS

4.	Not	Answered
Which of	the following 4-bit combinations is/are invalid in the BCD code?	
⊘ A.	1010	
B.	10	
C.	101	
D.	1000	

5.		Not Answered
Data inp	uts of a memory is also known as	
A.	Data entries	
B.	Data lines	
C.	Data ports	
⊘ D.	Data buses	

6.		Not Answered
How mai	ny different states does a 3-bit asynchronous counter have?	
A.	2	
B.	4	
⊘ C.	8	
D.	16	

7		Not Answ	vered
V	/ithout a	any additional circuitry an 8:1 MUX can be used to obtain	
	A.	Some but not all Boolean functions of 3 variables	
	В.	All function of 3 variables but none of 4 variables	
	C.	All functions of 3 variables and some but not all of 4 variables	

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⊘ D. All functions of 4 variables

Not Answer	
One of t	ne major drawbacks to the use of asynchronous counters is
A.	low-frequency applications are limited because of internal propagation delays
B.	high-frequency applications are limited because of internal propagation delays
C.	asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications
⊘ D.	asynchronous counters do not have propagation delays and this limits their use in high-frequency applications

9.		Not Answered
f both in	puts of an S-R flip-flop are low, what will happen when the clock goes HIGH?	
A.	An invalid state will exist.	
⊘ B.	No change will occur in the output.	
C.	The output will toggle.	
D.	The output will reset.	

10.		Not Answered
he term	ninal count of a modulus-11 binary counter is	
A.	1010	
B.	1000	
C.	1001	
⊘ D.	1100	

11. Not Answered

For a function with large number of variable, which minimization technique is better

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A.	K-Map
B.	Boolean algebra
⊘ C.	Tabulation Method
D.	Venn diagram

	Not Answered
t of addition of two BCD numbers 1001 and 0101 will be	
11100	
1111	
1110	
10100	
	1111 1110

13.		Not Answered
The exce	ess-3 code for 5786 is given by	
⊘ A.	100010101111000	
B.	1000101000111001	
C.	1100101000111010	
D.	1000101110111000	

14.		Not Answered
Which one of the following has capability to store data in extreme high densities?		
A.	Register	
B.	Capacitor	

C.	Flip-Flops
⊘ D.	Semicondutor

15.		Not Answered
Which Ic	gic family has highest noise margin?	
⊘ A.	CMOS	
B.	DTL	
C.	ECL	
D.	TTL	

6.		Not Answered
he full f	orm of VLSI is	
⊘ A.	Very Large Scale Integration	
B.	Very Long Scale Integration	
C.	Very Long Signal Integration	
D.	Very Large Signal Integration	

17.		Not Answered
f a funct	ion F(A,B) consists of all four minterms then its simplified expression is	
A.	A	
B.	В	
C.	0	
⊘ D.	1	

18. Not Answered

The bac	sic elemen	t of con	niconduc	tar mamar	ai v
THE Das	sic elemen	t or sen	niconduc	ioi memoi	y 15

⊘ A.	memory cell
B.	Registers
C.	Flip-Flops
D.	Counters

19.		Not Answered
In standa	ard TTL the 'totem pole stage refers to	
A.	The multi-emitter input stage	
В.	The phase splitter	
⊘ C.	The output buffer	
D.	Open collector output stage	

20.		Not Answered
low mar	ny 2:4 decoder used to represent 4:16	
A.	2	
B.	1	
⊘ C.	4	
D.	3	

21.		Not Answered
If A, B	are the inputs of a half adder then the carry is given by	
⊘ A.	A AND B	

В.	A OR B
C.	A XOR B
D.	A'B

22. Not Answered Which type of special IC's is programmed by user as per user requirement? **ASIC** A. **⊘** B. PLD C. **VLSI** D. **FPGA**

23. Not Answered One that is not the outcome of magnitude comparator is ____ a > b A. a - b**⊘** B. a < b C. a = bD.

24. Not Answered The number of Boolean functions which can be generated with four variables is A. 4 B. 16 C. 256 **⊘** D. 65536

25.		Not Answered
A Memor	ory which uses the Electrical altrable process is	
⊘ A.	EPROM	
B.	EPRAM	
C.	PRAM	
D.	PROM	

26.		Not Answered
Each cel	l of SRAM and DRAM are consist of which opction respectively	
⊘ A.	Flip-Flop and MOSFET	
B.	Diode and MOSFET	
C.	Diode and BJT	
D.	Flip-Flop and BJT	

27.		Not Answered
he float	ing input in TTL logic written as	
A.	0	
⊘ B.	1	
C.	niether 0 nor 1	
D.	10	

28. Not Answered

Which is the decimal equivalent of largest possible 16 bit binary number?

A.	65536
⊘ B.	65535
C.	32768
D.	32767

29.		Not Answered
How mar	y cells are there in a four variable K-Map?	
A.	4	
В.	8	
⊘ C.	16	
D.	32	

30. Not Answered The output of an exclusive-NOR gate is HIGH if _____. The inputs are equal **⊘** A. One input is HIGH, and the other input is LOW B. The inputs are unequal C. One input is LOW, and the other input is HIGH D.

31. Not Answered Find the value of x in (211)x=(152)8. A. 5 B. 6 **⊘** C. 7

D. 4

32.	Not Answered	t
If enable	input is high then the multiplexer is	
A.	Enable	
⊘ B.	Disable	
C.	Saturation	
D.	High Impedance	

33.		Not Answered
By taking	g 1's complement again of the 1's complement of a binary number, we get	
A.	2's complement	
⊘ B.	the original number	
C.	the signed magnitude form of the number	
D.	its gray equivalent	

34 .		Not Answered
Vhich of	these sets of logic gates are designated as universal gates?	
A.	OR, NOT, AND	
B.	XOR, NOR	
⊘ C.	NOR, NAND	
D.	NAND, XNOR	

35. Not Answered An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?

A.	Three
B.	One
C.	Two
⊘ D.	Fifteen

36.	Not Answer	ed
The full r	name of EPROM Memory is	
⊘ A.	Erasable and Programmable Read Only Merory	
B.	Empty and Programming Read Only Merory	
C.	Erased and Programmed Read Only Merory	
D.	Enabled and Programmed Read Only Merory	

37.		Not Answered
he way	to speed up DTL is to add as across intermediate resistor is	
⊘ A.	small "speed up" capacior	
B.	large "speed up" capacior	
C.	large "speed up" transistor	
D.	small "speed up" transistor	

38.		Not Answered
NAND ga	ate is also known as	
⊘ A.	Bubbled OR	
B.	Bubbled NOR	

C.	Bubbled AND
D.	Bubbled NOT

39.		Not Answered
Solve by	BCD adder (1000 0101)BCD + (0111 0110) BCD =()10	
A.	85	
B.	76	
C.	162	
⊘ D.	161	

10.		Not Answered
⊺he bina	ry equivalent of 3F2A is	
A.	11011100101010	
⊘ B.	11111100101010	
C.	11011000101010	
D.	11011000100101	

11.		Not Answered
Vhich st	atement BEST describes the operation of a negative-edge-triggered D flip-flop)?
⊘ A.	The logic level at the D input is transferred to Q on NGT of CLK	
B.	The Q output is ALWAYS identical to the CLK input if the D input is HIGH.	
C.	The Q output is ALWAYS identical to the D input when CLK = PGT.	
D.	The Q output is ALWAYS identical to the D input.	

42. Not Answered

How many maxterms are possible with three variables			
A.	5		
В.	6		
C.	7		
⊘ D.	8		

43.		Not Answered
In FPGA	the vertical and horizontal directions are separated by	
A.	A line	
⊘ B.	A channel	
C.	A strobe	
D.	A Flip-Flop	

Which of the following control signals are selected for read and write operations in a RAM?

A. Data buffer

B. Chip select

OC. Read and Write

D. Memory

Which option is correct regarding DRAM

A. Dynamic Read Access Memory and data stored in form of inductor charged

B. Dynamic Random Access Memory and data stored in form of capacitor discharged

⊘ C.	C. Dynamic Random Access Memory and data stored in form of capacitor charged	
D.	Data Read Access Memory and data stored in form of capacitor discharged	

46.		Not Answered
For BCD	to 7 segment display how many digits represented in output	
⊘ A.	10	
B.	7	
C.	15	
D.	9	

17 .	Not Answe
As a ger	neral rule for stable flip-flop triggering, the clock pulse rise and fall times must be
A.	very long.
⊘ B.	very short.
C.	at a maximum value to enable the input control signals to stabilize.
D.	of no consequence as long as the levels are within the determinate range of value.

	Not Answered
ircuits consume power	
Equal to TTL	
Less than TTL	
Twice of TTL	
Thrice of TTL	
	Equal to TTL Less than TTL Twice of TTL

49. Not Answered

The full form	of CTDL is
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⊘ A.	Complemented Transistor Diode Logic
B.	Complemented Transistor Direct Logic
C.	Complementary Transistor Direct Logic
D.	Complementary Transistor Diode Logic

50.		Not Answered
The gray	code is a	
A.	reflective code	
B.	sequential code	
C.	alpha-numeric code	
⊘ D.	unit distance code	

51.	Not Answered
Cache m	nemory acts between
⊘ A.	CPU and RAM
В.	RAM and ROM
C.	CPU and Hard Disk
D.	None of these

52 .		Not Answered
How man	y flip-flops are required to make a MOD-32 binary counter?	
A.	3	

B.	45
⊘ C.	5
D.	6

53.		Not Answered
Го detect	a 1101 sequence by Finite sequence machine, how many states are made?	
A.	2	
B.	3	
⊘ C.	4	
D.	5	
E.	1	
	A. B. ② C. D.	To detect a 1101 sequence by Finite sequence machine, how many states are made? A. 2 B. 3 C. 4 D. 5

54.	Not Answered
MOSFET	Γ is also known as
A.	UJT
B.	BJT
C.	CMOS
⊘ D.	IGFET

55.		Not Answered
Which ty	pe of output current flow towards or into the output terminal in a logic circuit	
A.	sourcing current	
B.	Conventional current	
⊘ C.	sinking current	
D.	draining current	

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IN RTL NOR gate, the output is at logic 1 only when all the inputs are at

O A. logic 0

B. logic 1

C. 10 V

D. Floating

57.		Not Answered
Edge-trig	gered flip-flops must have	
A.	very fast response times.	
B.	at least two inputs to handle rising and falling edges.	
⊘ C.	a pulse transition detector.	
D.	active-LOW inputs and complemented outputs.	

58.		Not Answered
A main a	advantage of TTL with toem-pole output as compared to other TTL types are	
A.	Higher FIFO	
⊘ B.	Fast switching and low power dissipation	
C.	Higher noise margin and low cost	
D.	slow swirching and high power consumption	

59.	Not Answered
For a mu	ultistage counter to be truly synchronous, if
⊘ A.	Cp, the same clock input line
B.	CE, the same unclock input line

C.	the terminal count output
D.	both input lines

60.		Not Answered
As comp	pared to TTL, ECL has	
⊘ A.	Lower propagation delay	
В.	Lower power dissipation	
C.	Higher propagation delay	
D.	Higher noise margin	