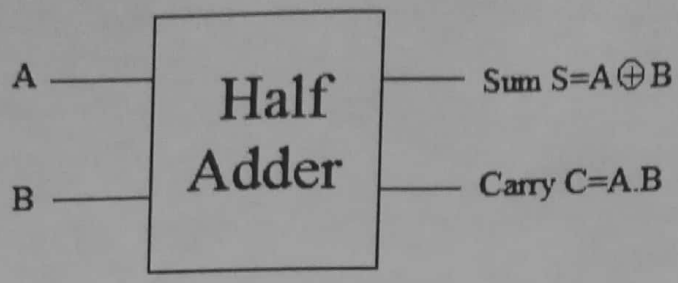
MEDI-CAPS UNIVERSITY, INDORE		
Department of Electronics & Communication	Lab Session No.	Page No.
Digital Electronics	**Enrol. No.**	Batch No.

Performance Evaluation:

Name							
Performing on		First Submission	Second Submission				
Extra	regular						
Grade and Remarks by the Tutor							
1.	**Clarity about the objective of the experiment**						
2.	**Clarity about the problem statement**						
3.	**Submitted the work in desired format**						
4.	**Shown capability to solve the problem**						
5.	**Contribution to the team work.**						
Others:							
Grade	A	B	C	D	F	Signature	

Experiment No. 3

1. **TITLE:** Implementation of half adder and full adder circuits.
2. **AIM:**
   a. To understand Binary addition using adder.
   b. Implementation of Adder using logic gates.
   c. To learn about the combinational circuits.
3. **OBJECTIVE**: After performing this experiment students will be able to understand:
   a. The concept of binary addition and its utility.
   b. The utility of logic gates to implement half adder, full adder.
4. **PROBLEM STATEMENT:**
   a. To design the circuit of adder using IC7408, 7404, 7432, 7486.
   b. Perform the addition operation using these circuits.
5. **Apparatus required:**
   a. Prototyping board (Bread board).
   b. DC power supply 5V battery.
   c. Light Emitting Diodes (LED's).
   d. Digital IC's: 7408 Quad 2 input AND gate, 7432 Quad 2 input OR gate, 7486 Quad 2 input XOR gate.
   e. Connecting wires.
6. **THEORY:**
   a. **Half Adder:** A half adder is a logical circuit that performs an additional operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits. The drawback of this circuit is that in case of a multi-bit addition, it cannot cater to carry.



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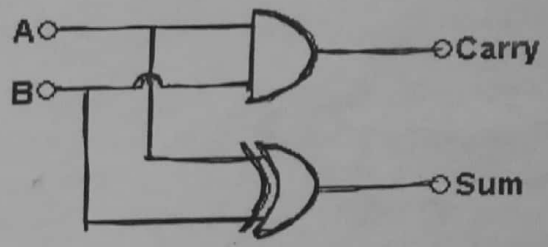
Truth Table of Half Adder

Inputs		Outputs	
A	B	Sum(S)	Carry(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean expression for sum and carry of half adder

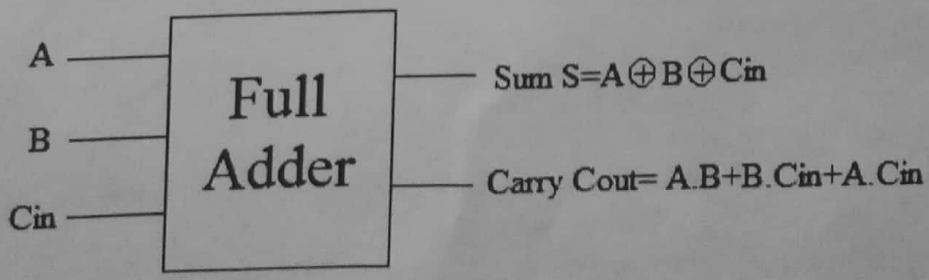
$SumS = \overline{A}B + A\overline{B}$

$CarryC = A.B$



Logic Diagram

b. Full adder: A full adder is a logical circuit that performs an additional operation on three binary digits. The full adder produces a sum and a carry value, which are



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both binary digits. It can be combined with other full adders (see below) or work on it's own.

Truth Table of Full Adder:

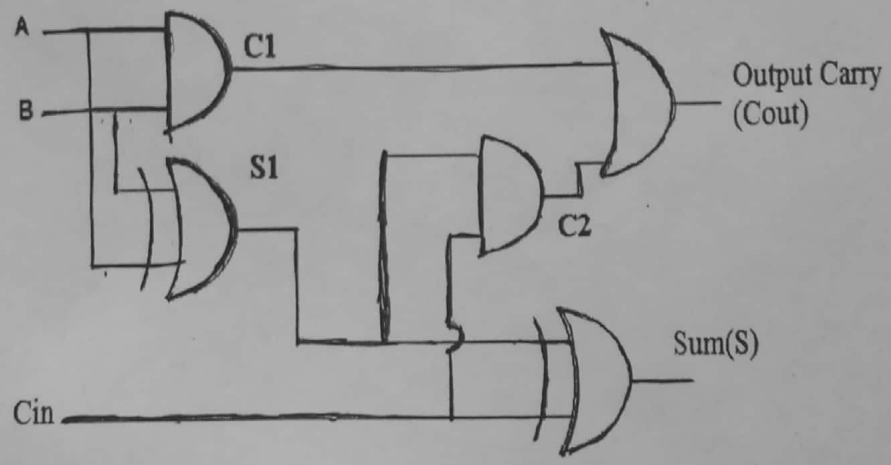
X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Expression:

Sum $S=A'B'C_{in}'+A'B'C_{in}+A'BC_{in}'+AB'C_{in}'+ABC_{in}$

Carry $C_{out}=AB+AC_{in}+BC_{in}$

Circuit Diagram:



7. **Result:** (students have to write the result by their own what result occurs)
8. **Self assessment:**
   a. Define combinational logic?
   b. Define full adder and half adder?
   c. Implement full adder using half adders.
   d. How can we implement SOP & POS in full adder?
   e. How can we implement the full adder with two half adder & an OR gate?
   f. Make the half adder using AND, OR and NOT gate?
   g. Make the half adder by NAND gate?

Prepared by	Date	Modified on
Nayan Bhale	21/8/17	