Digital Electronics

Unit-1 Number System :-

Instruction to binary numbers, data representation, binary, octal, hexadecimal no. System and their conversion, Various Coding schemes such as BCD codes, Excess 3 Code, Gray Code. Binary Arithmetic Boolean Algebra, Basic Theorem & properties of boolean Algebra. Boolean fun. Canonical and Standard forms, minimization techniques, SOP & POS simplification, Karnaugh's Map method, Quine McCluskey method.

Unit II :- Logic Gates And Combinational Logic :-

Digital Logic gates such as AND, OR, NAND, NOR EX-OR, EX-NOR. Realization of boolean fun using logic gates. Adders, Substractors, BCD adder, magnitude comparator, decoders & encoders, Multiplixer and demultiplixer Code Converters Analysis & design of Combinational circuits Implementation of Combinational logic using multiplixer decoders etc.

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Unit 3 :- Sequential Circuits :-

Introduction, Comparision of sequential and combinational circuits. Various types of flip-flops and their conversion, triggering of flip-flops, timing issu. setup and hold times, registers, counters, ring, johson, asynchronus and synchronus. Finite State Machines, Moore and Mealy, design of synchronous ~~an~~ sequential circuits.

Unit 4 :- Memories :-

ROM, PLA & PAL. Memories : Organisation and construction of RAM, SRAM, DRAM, ROM, PROM, EPROM, EEPROM.

Unit 5 :- LOGIC FAMILIES :-

DTL, RTL, TTL, IIL, PMOS, NMOS & CMOS logic families, Interfacing between TTL & MOS vise versa.

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Number System

~~Contd~~

1) Convert decimal to base (binary 2, Octal 8, hexadecimal 16)

$(\quad)_{10} \longrightarrow (\quad)_2$, $(\quad)_8$, $(\quad)_{16}$ (Devide by base)

2) Converting from any base to decimal

$(\quad)_2$, $(\quad)_8$, $(\quad)_{16}$ $\longrightarrow (\quad)_{10}$

(multiply by base ~~base~~ power)

3) Converting from ~~hex~~ binary to hexadecimal or vice versa (Table pair of 4)

4) Converting from octal to binary or vice versa (Table pair of 3)

5) Converting from Hex to Octal (~~Pair of 4~~ Hex binary → octal)

6)

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6) $(16)_{10} \longrightarrow (100)_x$

$1 \times x^2 + 0 \times x^1 + 0 \times x^0 = 16$

$x^2 = 16$ $\boxed{x = 4}$

Codes

→ Symbol to discrete data.

Two types of code :-

1) numeric code
2) Alphanumeric code (Alphabatic + special case) (ASCII / EBCDIC code)

(Extended binary Coded Decimal Interchange code)

① Straight binary Code :- Binary Conversion to decimal value.

② BCD code :- Binary coded Decimal.

Decimal (0-9) represent in group of 4 bits

$(45)_{10} = (01000101)_{BCD}$ [Four Pair this is not binary Conversion]

Disadvantage — biggest code
Advantage — In Add + Sub.

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01001 → +9 | 11001 → 25 (unsigned), 9 (signed) | 0 + 1 → non-zero

Numeric Code

Weighted

The weight always have position ways principal

BCD – 8 4 2 1

2^3 2^2 2^1 2^0

Nonweighted

[Gray Code]

(is nonweighted code move one step to another step change of only one bit & also called unidistance code)

7 – 0111
8 – 1000

* Excess 3 code

(Another form of BCD code)

This is addition of 3 (~~0+3~~ 0+3 to 9+3)

$(24)_{10}$

+3 ↓ ↓

(5 7) ⟶ (0101 0111) Excess 3 (4 bit binary code)

11110110

+6

11110100

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Sign complement System)))
Sign magnitude System

NAND
NOT + AND
NOR
OR + NOT

Non Weighted Code

EX-OR
EX-NOR

1) Gray Code Conuersion

* Binary to Gray Code :

① $(1101 10)_2 \longrightarrow$ Gray

$(101101)_{Gray}$

② $(10110)_2 \rightarrow$ Gray

$(11101)_{Gray}$

EX-OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

7 — 0111 =
8 — 1000

* Gray to binary

① $(110111)_{Gr} \rightarrow (\ )_2$

$(100101)_{Gray}$

② $(1010111)_{Gr} \longrightarrow (\ )_2$

$(1100101)_2$

0111
(0101)$_{Gr}$
0111 — 7
(0100)$_{Gr}$
1000 — 8
(1100)$_{Gr}$

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Binary Arithmetic

1+0=1
1+1=10

(1)
```
   1 1 1
   1 1 1 1
 + 1 0 1 1
 -------
 1 1 0 1 0
```

```
  10
+  1
  --
  11
```

(2)
```
  10 10 10
  1 0 1 0
- 0 1 1 1
 --------
  0 0 1 1
```

0-0=0
1-0=1
10-1=1

→ Signed binary No Representation

binary no are represented ~~by~~ it with a seperate sign bit along with magnitude

ex:- In an 8 bit binary no. MSB represents sign bit. Rest of the 7 bit represent the magnitude

MSB
[D7] [D0]
Sign 7 bit (magnitude) LSB

0+

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① $(25)_{10}$ → (sign binary represent)

2	25 — 1
2	12 — 0
2	6 — 0
2	3 — 1
	1

11001

$\boxed{0 \mid 0011001}$

② $(-25)_{10}$ → $\boxed{1 \mid 0011001}$

* Represent of no. in Complementary no

Complement of no:— $(101110)_2$

(010001) — 1's

$+ 1$

010010 — 2's

Direct — 2's

Write the digit u get the 1st one and then reverse the rest one

(101100)

(010100) 2's

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−ve no Represent in Three Way

1) Sign magnitude
2) In once Complem
3) 2's Complement

$(-51)_2 \rightarrow$

2	51
2	25 − 1
2	12 − 1
2	6 − 0
2	3 − 0
	1 − 1

sign magnitude

$\boxed{1}$ 0(110011)

1's = (−51)

00(110011

11001100 — 1's

+ 1

11001101 — 2's

* For +ve no. sign magnitude, 1's & 2' are same.

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(2) 9 − 4.

9 → 8 bit binary.
4 → 8 bit binary
1's-comp.
2's-comp.

9
+
9 + (−4).

9 − 4 (by 2's comp)

2 | 9 − 1
2 | 4 − 0
2 | 2 − 0
| 1

1001 = 9 = 9 + (−4)

2 | 4 − 0
2 | 2 − 0
| 1

100 = 4

(−4). → 2's

1001
00

00000100

11111011 − 1's
+ 1

11111100

+1001

2 | 5 − 1
2 | 2 − 0
| 1

101

(00001001)

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20 Addition in 2's Comp. System

1. $(9)_{10} + (8)_{10}$

2	9 – 1
2	4 – 0
2	2 – 0
	1

2	8 – 0
2	4 – 0
2	2 – 0
	1

```
  00001001
+ 00001000
----------
  00010001  –(17)10
```

2	17 – 1
2	8 – 0
2	4 – 0
2	2 – 0
	1

(2) $9 - 4 = 9 + (-4)$

(3) $(26)_{10} - (16)_{10}$

2	26 – 0
2	13 – 1
2	6 – 0
2	3 – 1
	1

2	16 – 0
2	8 – 0
2	4 – 0
2	2 – 0
	1

```
00011010 – (26)
11110000 – (–16)
----------------
(00001010)
```

```
00010000
11101111 – 15
       + 1
----------
11110000 – 15
```


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④ 19 + (−26)

2	19 − 1
2	9 − 0
2	4 − 0
2	2 − 0
	1

00011011 − (19)
11100110

11111001

(If there is carry & discard the carry & final Result but if not then take 2's c)

1 so result is negative

~~1 so result is negat~~

00011010
10100101
+ 1
11100110

11111001

00000110
+ 1
(− 00000111) (−7)

26
19
07

⑤ (−9) + (−4)

9 = 00001001

11110110 ← 1's
+ 1

4 = 00000100
11111011
+ 1
11111100
11111101
+ 1

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Here discard the Carry & Convert it into 2's

1 1 1 1 0 0 1 1

$\boxed{0\,0\,0\,0\,1\,1\,0\,0}$

⑥ $-9 + (+9)$

Subtraction in 2's Complement System

Neget the subtrant (sec) and add it to the minund. (- first)

1's Complement

If there is carry add the Carray to Result
If not than only take 1's Comlement

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① $(37)_{10} - (24)_{10}$.

2	37	1
2	18	0
2	9	1
2	4	0
2	2	0
	1	

2	24	0
2	12	0
2	6	0
2	3	1
	1	

00100101 — 37

~~+ 11011010 — 1's~~

11101101

11000001

+ 1

11000011

00010000 — 24

11100111 — 1's

00100101

+ 11100111

00001100

+ 1

~~00001101~~

00001100

Saturday

24

BCD addition

Add (1001) + (0100)
9 + 4

If carray generate

```
  1001
+ 0100
  1101
  0110 — 6
  10011
```

Add (6)
Correction factor 0110

0001 0011

Sunday

1 3

0	0	0	— 0
0	0	1	— 1
0	1	0	— 2
0	1	1	— 3
1	0	0	— 4
1	0	1	— 5
1	1	0	— 6
1	1	1	— 7

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Digital Electronics

(i) $(235.75)_{10} = (\quad)_2$

$0.75 \times 2 = 1.50 = 1$
$0.5 \times 2 = 1.0 = 1$

2	235 – 1
2	117 – 1
2	58 – 0
2	29 – 1
2	14 – 0
2	7 – 1
2	3 – 1
	1

$(11101011.11)_2 =$

1×2^0
1×2^1
0×2^2
1×2^3
0×2^4
1×2^5
1×2^6
$2^7\times1$

1 2 8 32 64

32 × 2 = 64

$= 235.75$

(ii) $(0.375)_{10} = (\quad)_8$

$0.375 \times 8 = 3 \quad (0.3)_8$

0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13

$0.375 \times 8 = 3.000$

$\therefore (105.72)_{16} = (\quad)_8$

0001 0000 0101 . 0111 0010

$0(4\ 0\ 5 . 3\ 4\ 4)_8$

5×8^0

$= 261.344$

$256 + 5$

$261 + 0.375 + 0.0625 + 7.8/10^3 =$

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March 2012

Tuesday

27

K-MAP
(Karnaugh Map)

SOP – $\bar{A}C + \bar{B}C + ABC$

POS. – $(A+B) \cdot (B+\bar{C}) \cdot (\bar{C}+A)$

bit high – at no. (0–7).

A \ B	0	1
0	0	1
1	2	3

$y = \Sigma(0, 2)$

$\boxed{Y = \bar{B}}$

AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

A \ B	$\bar{B}$	B
$\bar{A}$	0	0
A	0	1

$Y = A \cdot B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

A \ B	$\bar{B}$	B
$\bar{A}$	0	1
A	1	1

$\boxed{Y = A + B}$

1 – SOP Pairing

0 – POS

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A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

X-OR

A \ B	$\bar{B}$	B
$\bar{A}$	0	1
A	1	0

$Y = \bar{A}B + A\bar{B}$

3 bit Input

	A	B	C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	0 1	1 1	3 0	2 0 2
A 1	4 1	5 1	7 0	0 6

$\cancel{\bar{A}\bar{B}C + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C}$

$\Sigma(0,1,4,5)$

$\boxed{Y = \bar{B}}$

——	= 0
Not bar	= 1

$\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$

$\bar{A}\bar{B}(\bar{C}+C) + A\bar{B}(\bar{C}+C)$

$\bar{A}\bar{B}(1) + A\bar{B}(1)$

$\bar{B}(\bar{A}+A) = \bar{B}$

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	0	0	1
A	1	0	0	1

$\bar{C}$

1	0	0	1
0	0	1	1

2 pair

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AB \ C	0	1
00	0	1
01	2	3
11	6	7
10	4	5

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 0	1 0	3 1	2 0
$\bar{A}B$	4 0	5 0	7 1	6
AB	12 1	13 0	15 1	14 0
$A\bar{B}$	8 0	9 1	11 0	10 0

$\bar{A}CD + BCD + AB\bar{C}D + A\bar{B}\bar{C}D$

$\Sigma(3, 7, 12, 15, 9)$

$\Sigma(1, 4, 5, 7, 9, 11, 13)$

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 -	1 1	3	2
$\bar{A}B$	4 1	5 1	7 1	6
AB	12	13 1	15	14
$A\bar{B}$	8	9 1	11 1	10

$\bar{C}D + \bar{A}B\bar{C} + \bar{A}BD + A\bar{B}D$

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SOP

~~POS~~ = (1) baar at 0.

$Y = \Sigma_m (1, 5, 7, 9, 11, 13, 15)$

Π_m (max term)

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1 (1)	3	2
$\bar{A}B$	4	1 (5)	1 (7)	6
AB	12	1 (13)	15	14
$A\bar{B}$	8	1 (9)	1 (11)	10

2 → because of gray code

quad 1 = $\bar{C}D$

quad 2 = DB

quad 3 = AD

$Y = \bar{C}D + DB + AD$

$\boxed{Y = D(\bar{C} + B + A)}$

(2) $Y = \underbrace{\bar{A}\bar{B}\bar{C}}_{m0} + \underbrace{\bar{A}\bar{B}\bar{C}}_{m2} + \underbrace{\bar{A}BC}_{m3} + \underbrace{A\bar{B}C}_{m5}$

Minimize the expression using K-map

$\bar{A}$ \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1 (0)	0 (1)	1 (3)	1 (2)
A	0 (4)	1 (5)	0 (7)	0 (6)

Pair 1 :- $\bar{A}B$

Pair 2 :- $\bar{A}\bar{C}$

Isolated one :- $A\bar{B}C$

$Y = \bar{A}B + \bar{A}\bar{C} + A\bar{B}C$

$Y = \bar{A}(B + \bar{C}) + A\bar{B}C.$

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31 Q $Y = \underbrace{\bar{A}\bar{B}CD}_{m_3} + \underbrace{\bar{A}BC\bar{D}}_{m_6} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D} + A\bar{C} + \bar{B}$

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1 (0)	1 (1)	1 (3)	1 (2)
$\bar{A}B$	0 (4)	0 (5)	0 (7)	1 (6)
AB	1 (12)	1 (13)	0 (15)	0 (14)
$A\bar{B}$	1 (8)	1 (9)	1 (11)	1 (10)

octat 1 :- $\bar{B}$
quard :- $A\bar{C}$
pair :- $\bar{A}CD$

$\cancel{Y = \bar{A}\bar{B} + CD\bar{A} + A\bar{B}} +$

$$\boxed{Y = \bar{A}C\bar{D} + A\bar{C} + \bar{B}}$$

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POS form (0 pairing) using K-map (Π_M)

A \ B	B	$\overline{B}$
A	$A+B$	$A+\overline{B}$
$\overline{A}$	$\overline{A}+B$	$\overline{A}+\overline{B}$

A \	$B+C$	$B+\overline{C}$	$\overline{B}+\overline{C}$	$\overline{B}+C$
A	$A+B+C$	$A+B+\overline{C}$	$A+\overline{B}+\overline{C}$	$A+\overline{B}+C$
$\overline{A}$	$\overline{A}+B+C$	$\overline{A}+B+\overline{C}$	$\overline{A}+\overline{B}+\overline{C}$	$\overline{A}+\overline{B}+C$

$Y = \Pi_M(0, 2, 3, 5, 7)$

A \	$B+C$	$B+\overline{C}$	$\overline{B}+\overline{C}$	$\overline{B}+C$
A	0 (0)	1 (1)	0 (3)	0 (2)
$\overline{A}$	1 (4)	0 (5)	0 (7)	1 (6)

Pair 1 :- $\overline{A}+\overline{C}$
Pair 2 :- $\overline{B}+\overline{C}$
~~single~~ :- $A+\overline{B}$ ~~B~~
Pair 2 :- C

$Y = (\overline{A}+\overline{C}) \cdot (\overline{B}+\overline{C}) \cdot (A+\overline{B})C$

1 X

* Don't Care Condition :-

(d/x)

excess 3

0000
0011 — 0011

If I have X, so it is treated as 1.

$0 \rightarrow 0011$

0001 — 0100

0011

$1 \rightarrow 0100$

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* $\Sigma m(1,4,7,10,13) + \Sigma d(5,14,15)$

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	1 (1)	0 (3)	0 (2)
$\bar{A}B$	1 (4)	X (5)	1 (7)	0 (6)
AB	0 (12)	1 (13)	X (15)	X (14)
$A\bar{B}$	0 (8)	0 (9)	0 (11)	1 (10)

quard 1 = BD
pair 1 = $AC\bar{D}$
pair 2 = $\bar{A}B\bar{C}$
pair 3 $\bar{C}D\bar{A}$

* $\Sigma m(4,5,7,12,14,15) + \Sigma d(3,8,10)$

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	0 (1)	X (3)	0 (2)
$\bar{A}B$	1 (4)	1 (5)	1 (7)	0 (6)
AB	1 (12)	0 (13)	1 (15)	1 (14)
$A\bar{B}$	X (8)	0 (9)	0 (11)	X (10)

quad 1:- $A\bar{D}$
pair 1 :- $C\bar{D}\bar{A}$
pair 2 :-

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5 Variable K-Map

$\bar{A}$

BC \ DE	$\bar{D}\bar{E}$	$\bar{D}E$	DE	$D\bar{E}$
$\bar{B}\bar{C}$	1 0	1	1 3	1 2
$\bar{B}C$	4	5	7	6
BC	1 12	1 13	15	14
$B\bar{C}$	8	9	1 11	1 10

2

A

BC \ DE	$\bar{D}\bar{E}$	$\bar{D}E$	DE	$D\bar{E}$
$\bar{B}\bar{C}$	1 16	1 17	1 19	1 18
$\bar{B}C$	1 20	1 21	23	22
BC	28	29	31	30
$B\bar{C}$	24	25	1 27	1 26

1

$\Sigma m(0, 2, 3, 10, 11, 12, 13, 16, 17, 18, 19, 20, 21, 26, 27)$

A B C D E
0 0000
0 0001

15 → 01111
16 → 10000
31 → 11111

quad 1 :- $\bar{C}D\bar{A}$
quad 2 :- $\bar{C}D A$
quad 3 :- $\bar{B}\bar{D}A$
pair :- $BCD\bar{A}$
quad 4 :- $\bar{B}\bar{C}E$

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05 $\Sigma m(0,1,2,4,7,8,12,14,15,16,17,18,20,24,28,30,31)$

$\bar{A}$

BC \ DE	$\bar{D}\bar{E}$	$\bar{D}E$	DE	$D\bar{E}$
$\bar{B}\bar{C}$	1 (0)	1 (1)	(3)	1 (2)
$\bar{B}C$	1 (4)	(5)	1 (7)	(6)
BC	1 (12)	(13)	1 (15)	1 (14)
$B\bar{C}$	1 (8)	(9)	(11)	(10)

A

BC \ DE	$\bar{D}\bar{E}$	$\bar{D}E$	DE	$D\bar{E}$
$\bar{B}\bar{C}$	1 (16)	1 (17)	(19)	1 (18)
$\bar{B}C$	1 (20)	(21)	(23)	(22)
BC	1 (28)	(29)	1 (31)	1 (30)
$B\bar{C}$	1 (24)	(25)	(27)	(26)

Octat :- $\bar{D}\bar{E}$

quad 1 :- BCD

quad 2 :- $\bar{B}\bar{C}D$

quad 3 :- $\bar{B}\bar{C}\bar{E}$

pair :- $\bar{A}DEC$

* It is a manual process draw of K-map

Quine Mc-Cluskey :-

Or (Tabular Method)

Prime implicant = P

$PA + P\bar{A}$

$P(A+\bar{A})$

P

Convert into single if opposite bit are there.

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$\Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$

Index = no. of bit + 1

Index	Minterms	Binary representation	Minterm	Binary rep
Index 0	0	0 0 0 0	(0,1)	000 –
Index 1	1	0 0 0 1	(0,2)	00 – 0
	2	0 0 1 0	(0,8)	– 0 0 0
	8	1 0 0 0		
Index 2	3	0 0 1 1	(1,3)	00 – 1
	5	0 1 0 1	(1,5)	0 – 0 1
	9	1 0 0 1	(1,9)	– 001
Index 3	7	0 1 1 1	(2,3)	001 –
	11	1 0 1 1	(8,9)	100 –
	14	1 1 1 0		
			(3,7)	0 – 1 1
			(3,11)	– 0 1 1
			(5,7)	0 1 – 1
			(9,11)	10 – 1

PI = 14 ⇒ $ABC\overline{D}$

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$\bar{0}$ $\bar{1}$

April 2012

Saturday

07

Minterm	Binary repⁿ	
(0, 1, 2, 3)	0 0 — —	$\bar{A}\bar{B}$
(0, 1, 8, 9)	— 0 0 —	
(0, 2, 1, 3)	0 0 — —	
(0, 8, 1, 9)	— 0 0 —	
(1, 3, 5, 7)	0 — — 1	
(1, 3, 9, 11)	— 0 — 1	
(1, 5, 3, 7)	0 — — 1	
(1, 9, 3, 11)	— 0 — 1	

08 Sunday

$P(0, 1, 2, 3) \Rightarrow \bar{A}\bar{B}$

$Q(0, 1, 8, 9) \Rightarrow \bar{B}\bar{C}$

$R(1, 3, 5, 7) \Rightarrow \bar{A}D$

$t(1, 3, 9, 11) \Rightarrow \bar{B}D$

$S(1, 3) \Rightarrow \bar{A}\bar{B}\bar{C}D$

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Essential ❖ Follow-up

April 2012

Monday

09

Essential Prime Implicant

PI-Chart

PI \ Minterms	0	1	2	3	5	7	8	9	11	14
P(0,1,2,3)	X	X	X	X						
Q(0,1,8,9)	X	X					X	X		
R(1,3,5,7)		X		X	X	X				
S(1,3,9,11)		X		X				X	X	
T(14)										X

final = $\overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{A}D + \overline{B}D + ABC\overline{D} = Y$

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April 2012

Tuesday

10

Q. $\Sigma m(1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15)$

Index	Minterm	Binary Representation	Minterm	Binary Rep
Index 1	1	0001	(1, 3)	00_1
	2	0010	(1, 5)	0_01
	8	1000	(1, 9)	_001
Index 2	3	0011	(2, 3)	001_
	5	0101	(2, 6)	0_10
	6	0110	(8, 9)	100_
	9	1001	(8, 12)	1_00
	12	1100		
Index 3	7	0111	(3, 7)	0_11
	13	1101	(5, 7)	01_1
Index 4	15	1111	(5, 13)	_101
			(6, 7)	011_
			(9, 13)	1_01
			(12, 13)	110_
			(7, 15)	_111
			(13, 15)	11_1

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Binary Ra

Minterm	
(1,3,5,7)	0 _ _ 1
(1,5,3,7)	0 _ _ 1
(1,5,9,13)	_ _ 0 1
(1,9,5,13)	_ _ 0 1
(2,3,6,7)	0 _ 1 _
~~(2,6,3,7)~~	_
(2,6,3,7)	0 _ 1 _
~~(2,6,9,13)~~	~~_ _ 1 _~~
(8,9,12,13)	1 _ 0 _
(8,12,9,13)	1 _ 0 _
(5,7,13,15)	_ 1 _ 1
(5,13,7,15)	_ 1 _ 1

16	0	0	0	0	0 — 0
17	0	0	0	0	1 — 1
18	0	1	0	1	0 — 2
19	0	1	0	1	1 — 3
20	0	0	1	0	0 — 4
21	0	0	1	0	1 — 5
22	0	1	1	1	0 — 6
23	0	1	1	1	1 — 7
24	1	0	0	0	0 — 8
25	1	0	0	0	1 — 9
26	1	1	0	1	0 — 10
27	1	1	0	1	1 — 11
28	1	0	1	0	0 — 12
29	1	0	1	0	1 — 13
30	1	1	1	1	0 — 14
31	1	1	1	1	1 — 15

$PI = P(1,3,5,7) = \bar{A}D$

$Q(1,5,9,13) = \bar{C}D$

$R(2,3,6,7) = \bar{A}C$

$S(8,9,12,13) = A\bar{C}$

$T(5,7,13,15) = BD$

$\bar{A}D + \bar{C}D + \bar{A}C$

$D(\bar{A} + \bar{C}) + \bar{A}C$

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April 2012

Thursday

12

Essential Prime Implicant:

This is not ticked so used as ~~ESPI~~

PI Chart

PI \ Minterm	1	2	3	5	6	7	8	9	12	13	15
P(1,3,5,7)	X		X	X		X					
Q(1,5,9,13)	X			X				X		X	
R(2,3,6,7)		X	X		X	X					
S(8,9,12,13)							X	X	X	X	
T(5,7,13,15)				X		X				X	X

$$Y_1 = \bar{A}\bar{C} + A\bar{C} + BD + \bar{A}D$$

$$Y_2 = \bar{A}C + A\bar{C} + BD + \bar{C}D$$

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$\cancel{f. \Sigma m(6,7,8,9) + \Sigma d(10,11,12,13,15)}$

Tutorial

Show that

$A + \bar{A} = 1$
$1 + A = 1$

$A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B + C$

$\cancel{A\bar{B}C + B + \bar{D}(B + AB) + \bar{A}C}$

$\cancel{= AC(\bar{B} + \bar{A}) + B + \bar{D}(B + AB)}$.

$= A\bar{B}C + B(1 + \bar{D}) + AB\bar{D} + \bar{A}C$

$= A\bar{B}C + B + AB\bar{D} + \bar{A}C$.

$\cancel{A(\bar{B} + \bar{A}) + B(1 + A\bar{D})}$

$1 + 0 \cdot \bar{T}$
$1 + 0 \cdot 0$.

Distributive
$A + BC$
$(A+B)(A+C)$

$= A\bar{B}C + B(1 + A\bar{D}) + \bar{A}C$

$= A\bar{B}C + B + \bar{A}C$

$= C(A\bar{B} + \bar{A}) + B$

$= C(A + \bar{A})(\bar{B} + \bar{A}) + B$

$= \cancel{C(\bar{B} + \bar{A}) + B}$ $C(\bar{B} + \bar{A}) + B$

$= \bar{A}C + \bar{B}C + B$

$= \bar{A}C + (B + \bar{B})(B + C)$

$= \bar{A}C + B + C$

$C(A + 1) + B$

$\boxed{C(1) + B}$

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$A + BC$
$(A+B)(A+C)$

14 Q. Simplify

$(A+B)(A+\overline{C}) + \overline{A}\,\overline{B} + \overline{A}\,\overline{C}$

$(A \cdot A + A\overline{C}) + BA + B\overline{C} + \overline{A}\,\overline{B} + \overline{A}\,\overline{C}$

$A + \overline{C}(A+\overline{A}) + BA + B\overline{C} + \overline{A}\,\overline{B}$

$A + \overline{C} + BA + B\overline{C} + \overline{A}\,\overline{B}$

$A(1+B) + \overline{C}(1+B) + \overline{A}\,\overline{B}$

$A + \overline{C} + \overline{A}\,\overline{B}$

$(A+\overline{A})(A+\overline{B}) + \overline{C}$

$\boxed{A + \overline{B} + \overline{C}}$

Q. $A + B.[AC + (B+\overline{C})D]$

$= A + B[AC + BD + D\overline{C}]$

$= A + BAC + BD + BD\overline{C}$

~~$A + BD + B(AC$~~

$= A + BAC + BD(1+\overline{C})$

$= A + BAC + BD$ $= \boxed{A + BD}$

$A(1+BC) + BD$

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$A + BC$

$(A+B)(A+C)$

Q $\Sigma m(0,1,2,3,6,7,13,5)$

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1 (0)	1 (1)	1 (3)	1 (2)
$\bar{A}B$	(4)	1 (5)	1 (7)	1 (6)
AB	(12) (8)	1 (13) (9)	1 (15) (14)	(10)
$A\bar{B}$	(8)	1 (9)	(10)	(11)

1 quad $= \bar{A}\bar{B}$

2 quad $= \bar{A}C$

~~Pair 1 = $\bar{A}\bar{B}D$~~ Pair $= ABD$

~~Single = $\bar{C}\bar{D}A\bar{B}$~~ $ABCD$

Q $\Sigma m(0,1,2,3,4,5) + \Sigma d(10,11,12,13,14,15)$

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1 (0)	1 (1)	1 (3)	1 (2)
$\bar{A}B$	1 (4)	1 (5)	(7)	(6)
AB	X (12)	X (13)	X (15)	X (14)
$A\bar{B}$	(8)	(9)	X (11)	X (10)

$\bar{A}\bar{B} +$

$\bar{A}\bar{C}$

Scanned by CamScanner

17 Q Simplify

$\bar{A} + AB + AB\bar{D} + A\bar{B}\bar{D} + C$

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1 (0)	1 (1)	1 (3)	1 (2)
$\bar{A}B$	1 (4)	1 (5)	1 (7)	1 (6)
AB	1 (12)	1 (13)	1 (15)	1 (14)
$A\bar{B}$	1 (8)	0 (9)	1 (11)	1 (10)

$\cancel{\bar{A} + B + \bar{C}A + \bar{C}\bar{D}A}$

$\bar{A} + B + C + \bar{D}$

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Q (6, 9, 13, 18, 19, 25, 27, 29, 31) using k-map

	$\bar{D}\bar{E}$	$\bar{D}E$	DE	$D\bar{E}$
$\bar{B}\bar{C}$	0	1	3	2
$\bar{B}C$	4	5	7	6
BC	12	13	15	14
$B\bar{C}$	8	9	11	10

	$\bar{D}\bar{E}$	$\bar{D}E$	DE	$D\bar{E}$
$\bar{B}\bar{C}$	16	17	19	18
$\bar{B}C$	20	21	23	22
BC	28	29	31	30
$B\bar{C}$	24	25	27	26

quad 1 – $\bar{A}BE$

Quad 2 – $B\bar{D}E$

Pair 1 – $\bar{A}\bar{B}\bar{C}D$

Single – $\bar{A}\bar{B}CD\bar{E}$

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$\Sigma m(6, 7, 8, 9) + \Sigma d(10, 11, 12, 13, 15)$

Index	Minter	Binary Represe
Index 1	8	1000
Index 2	6	0110
	9	1001
	10	1010
	12	1100
Index 3	7	0111
	11	1011
	13	1101
Index 4	15	1111

Minter	Binary
(8, 9)	100_
(8, 10)	10_0
(8, 12)	1_00
(6, 7)	011_
(9, 11)	10_1
(9, 13)	1_01
(10, 11)	101_
(12, 13)	110_
(7, 15)	_111
(11, 15)	1_11
(13, 15)	11_1

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Minter	Binary
(8, 9, 10, 11)	1 0 — —
(8, 9, 12, 13)	1 — 0 —
(8, 10, 9, 11)	1 0 — —
(8, 12, 9, 13)	1 — 0 —
(9, 11, 13, 15)	1 — — 1
(9, 13, 11, 15)	1 — — 1

PI =

P (8, 9, 10, 11) = $A\bar{B}$

Q (8, 9, 12, 13) = $A\bar{C}$

R (9, 11, 13, 15) = AD

S (6, 7) = $\bar{A}BC$

T (7, 15) = BCD

PI	6 ✓	7 ✓	8	9
P(8, 9, 10, 11)			×	×
Q(8, 9, 12, 13)			×	×
R(9, 11, 13, 15)				×
S (6, 7)	×	×		
T(7, 15)		×		

P, Q.

$\boxed{\bar{A}BC} + A\bar{B}$, Or $\bar{A}BC + A\bar{C}$

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Q E (0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)

~~Minterm~~ Index	Minterm	Binary	Min	Binary
Index 0	0	00000	(0,1)	0000_
Index 1	1	00001	(0,2)	000_0
	2	00010	(0,8)	0_000
	8	01000		
Index 2	9	01001	(1,9)	0_001
	17	10001	(1,17)	_0001
	24	11000	(8,9)	0100_
			(8,24)	_1000
Index 3	21	10101	(9,25)	_1001
	25	11001	(17,21)	10_01
			(17,25)	1_001
Index 4	15	11111	(24,25)	110_0
PI	27	11011	(25,27)	110_1
Index 5	31	11111	(27,31)	11_11

22 Sunday

APR 2012 Su Mo Tu We Th Fr Sa Su Mo Tu We Th Fr Sa Su Mo Tu We Th Fr Sa Su Mo Tu We Th Fr Sa Su Mo Tu
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

Scanned by CamScanner

1 0 0 00 — 16

01

10

11

$\boxed{PI}$ P = (0,2) = $A\bar{B}\bar{C}\bar{E}$

Q = (8,24) = $B\bar{C}\bar{D}\bar{E}$

R = (17,21) = $A\bar{B}\bar{D}E$

S = (25,27) = $AB\bar{C}\bar{D}E$

T = (27,31) = $ABD\bar{E}$

U = (0,1,8,9) = $\bar{A}\bar{C}\bar{D}$

V = (1,9,17,25) = $\bar{C}\bar{D}E$

W = (8,9,24,25) = $B\bar{C}\bar{D}$

X = (15) = ABCDE

Minter	Binin
(0,1,8,9)	0 _ 00 _
(0,8,19)	0 _ 00 _
(8,9,24,25)	_ 1 00 _
(1,9,17,25)	_ _ 001
(1,17,9,25)	_ _ 001

PI	0	1	2	8	9	15	17	21	24	25	27	31
(0,2)	X		X									
(8,24)				X					X			
(17,21)							X	X				
(25,27)										X	X	
(27,31)											X	X
(0,1,8,9)	X	X		X	X							
(1,9,17,25)		X			X		X			X		
(8,9,24,25)				X	X				X	X		
(15)						X						

Tu We Th Fr Sa Su Mo Tu We Th Fr Sa Su Mo Tu We Th Fr Sa Su Mo Tu We Th Fr Sa Su Mo Tu We Th MAY
01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 2012

A B C E + A B D E + AB D + A C D + B C D

+ ABCDE

Scanned by CamScanner

NOR

$\overline{\bar{A}\cdot B + A\cdot \bar{B}}$

$\bar{A}\cdot B + A\cdot \bar{B}$

Unit - 2.

Logic Gates :-

$\overline{A+B} = \bar{A}\cdot\bar{B}$

$\bar{A}\cdot\bar{B}$

$A+B$

Basic Gates :- NOT
AND *
OR +

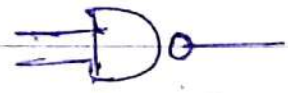
NAND
NOR
EXOR
EX-NOR

$\overline{A+B} = \bar{A}\cdot\bar{B}$

$\overline{A\cdot B} = \overline{A+B}$

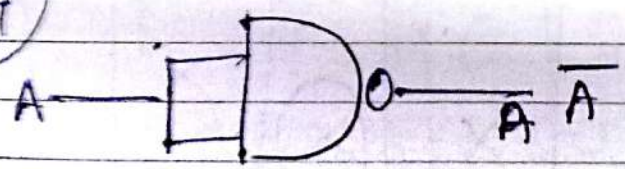
$\bar{A}+\bar{B}$

Universal gate



⇒ NAND → NOT
⇒ NOR, AND
OR
EX-OR
EX-NOR
NOR

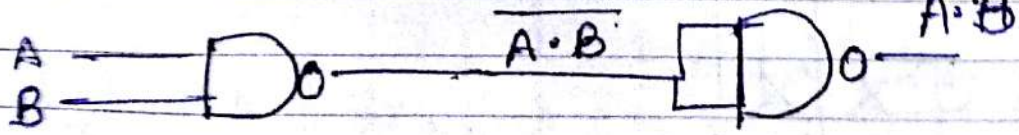
NOT



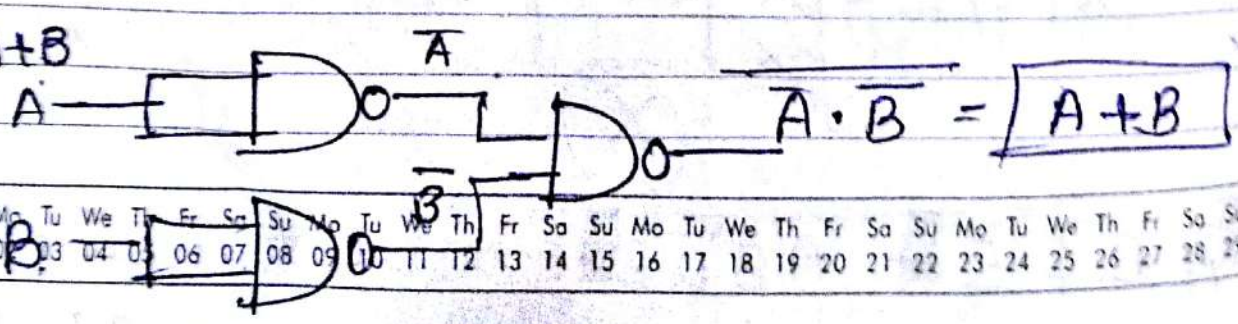
$\bar{A\cdot B}$

$\bar{A}\cdot B$

AND $A\cdot B$



Or $A+B$



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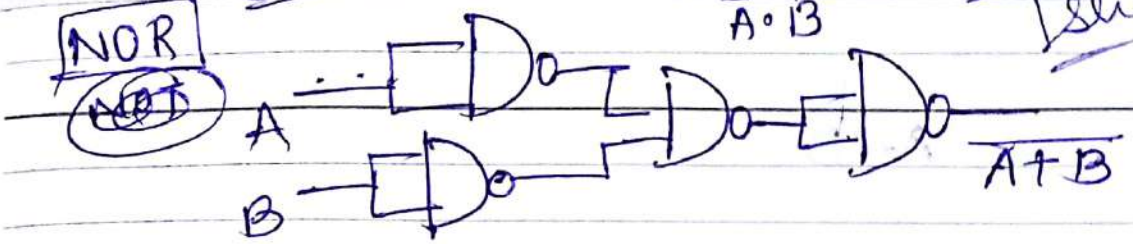
[RGIAC]

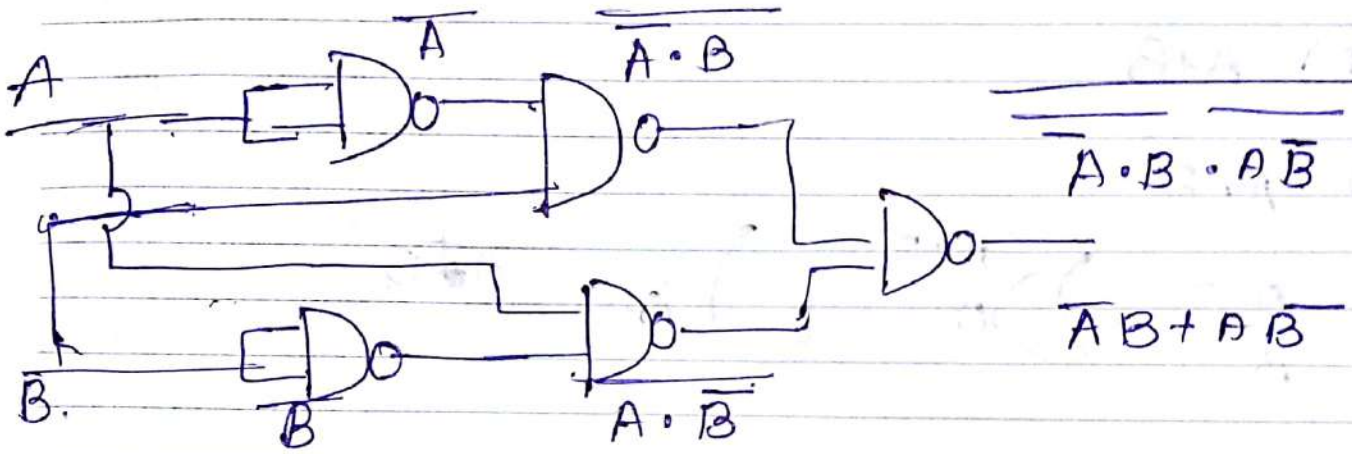
Bansal [Shahpura] [Jaipur]

NOR

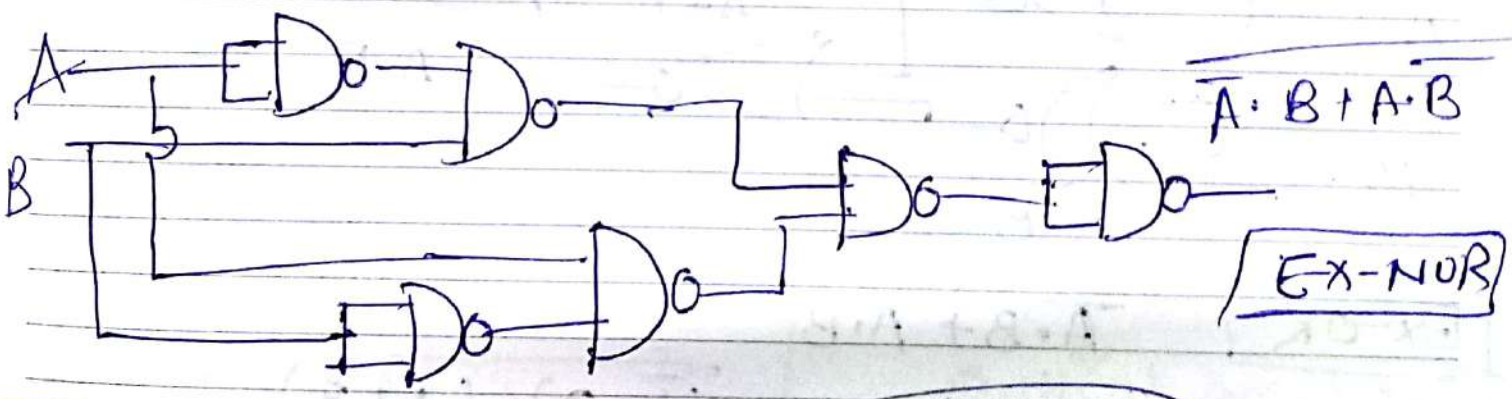


Ex-OR

$\overline{A} \cdot B + A \cdot \overline{B}$



EX-NOR



$(\overline{A} \cdot B) + (A + \overline{B})$

EXOR

$\overline{A} \cdot B + A \cdot \overline{B}$

$\overline{(\overline{A} \cdot B) \cdot (A \cdot \overline{B})}$

$(\overline{A} + \overline{B}) \cdot (\overline{A} + \overline{\overline{B}})$

$(A + B) \cdot (\overline{A} + B)$

$(A + \overline{B}) + (\overline{A} + B)$

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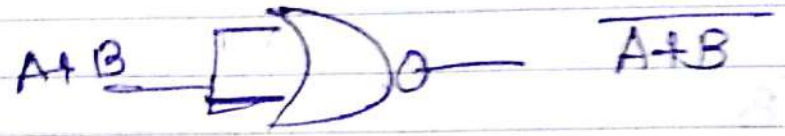
NOR. $\overline{A+B}$

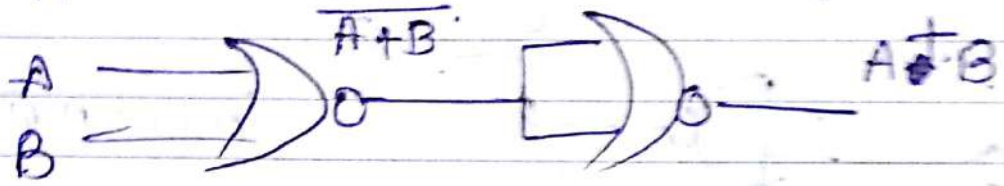
NOT



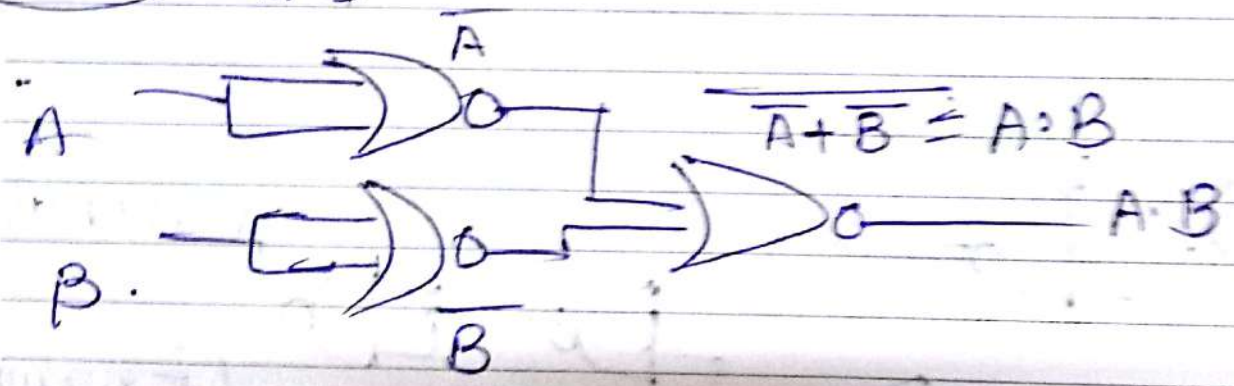
OR

~~NOR~~ $A+B$

$\overline{\overline{A+B}}$ $\overline{\overline{A}}\cdot\overline{\overline{B}}$



AND $A\cdot B$



Ex-OR $\overline{A}\cdot B + A\cdot\overline{B}$

~~$\overline{A\cdot B} + \overline{A\cdot B}$~~

~~$\overline{A+B}$~~

$$= \overline{(\overline{A}+B)\cdot(A+\overline{B})}$$

$$= \overline{\overline{\overline{A}+B} + \overline{(A+\overline{B})}}$$

$$= \overline{(\overline{\overline{A}}\cdot\overline{B}) + (\overline{\overline{A}}\cdot\overline{\overline{B}})}$$

$$= \overline{(A\cdot\overline{B}) + (\overline{A}\cdot B)}$$

$$(\overline{A}\cdot\overline{B})\cdot(\overline{A}\cdot B)$$

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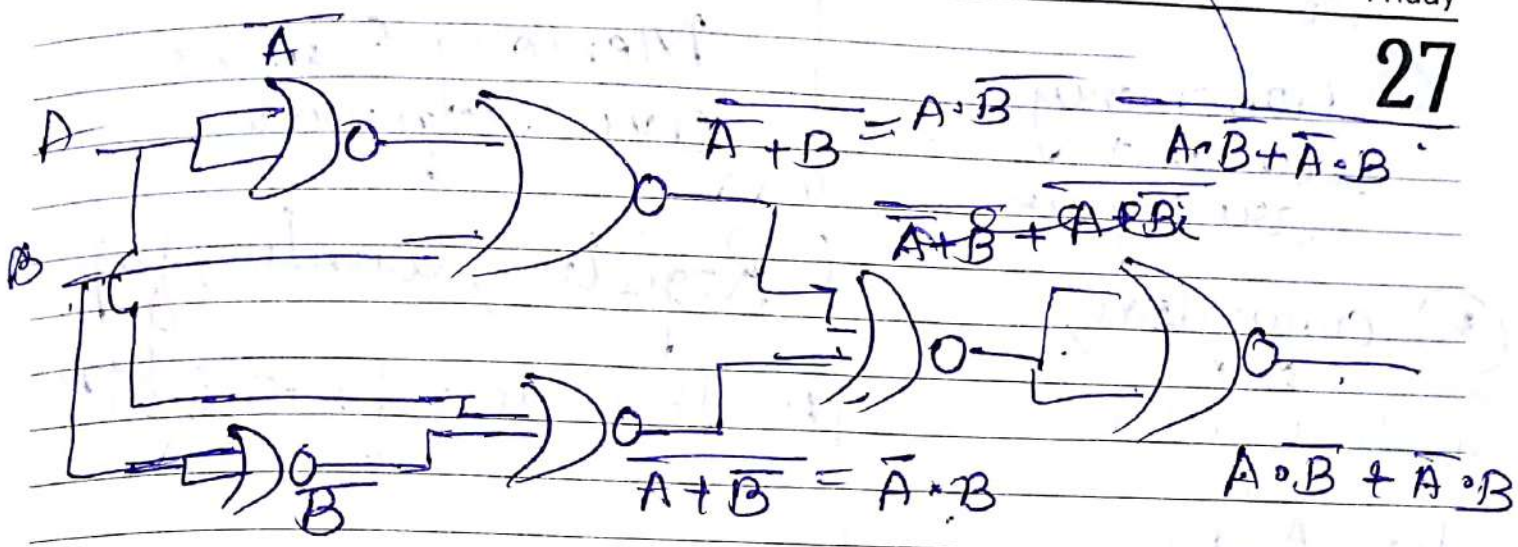
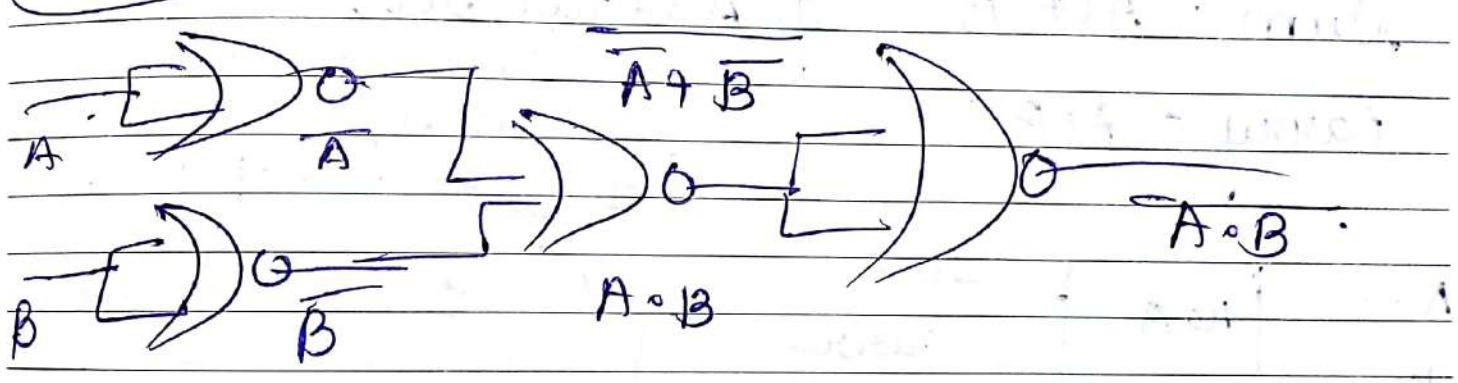
Ex-NOR

$= (\bar{A}+B) \cdot (A+\bar{B})$



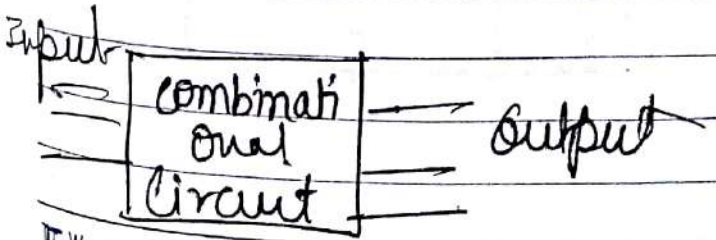
NAND



Combinational Circuit

↓

output depend on the present state of Input

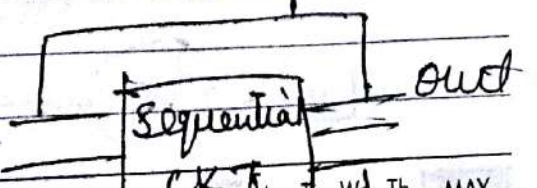


Ex:- half adder

Vs Sequencbel. Circuit

↓

Output not only depend on the present state previous state of the Output



Ex:- flip flop

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April 2012

Saturday

28 (2) Nomemory element are requir

(3) convertors, BCD.

(4) It is faster

(2) Memory Element are required

(1) Register, Counter, flip-flop

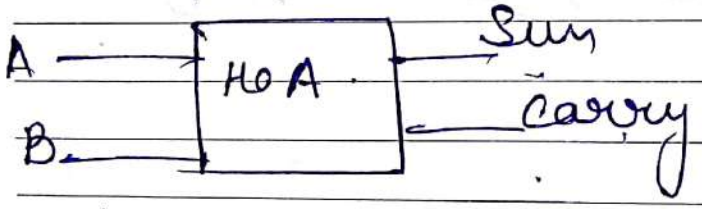
(4) It is less faster (slower)

Half Adder

$Sum = A \oplus B$

$Carry = A \cdot B$

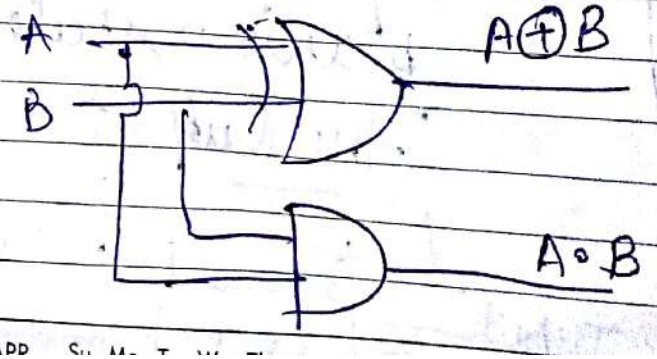
It Add two bit.
It is a Combinational circuit.



Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

29 Sunday $Sum = \bar{A}B + A\bar{B} = A \oplus B$

$Carry = A \cdot B$



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Full Adder

→ Used to Add two or more than two binary bit.

			Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Sum

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0 (0)	1 (1)	0 (3)	1 (2)
A	1 (4)	0 (5)	1 (7)	0 (6)

$$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$

EXOR EXNOR

$B \oplus C = X$

$$\bar{A}(B \oplus C) + A\overline{(B \oplus C)}$$

$$\bar{A}(B \oplus C) + A(B \odot C)$$

$$= A \oplus B \oplus C$$

$$A + X$$

$$A \oplus X$$

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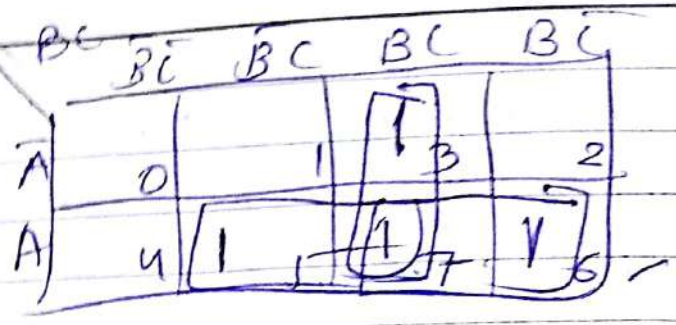
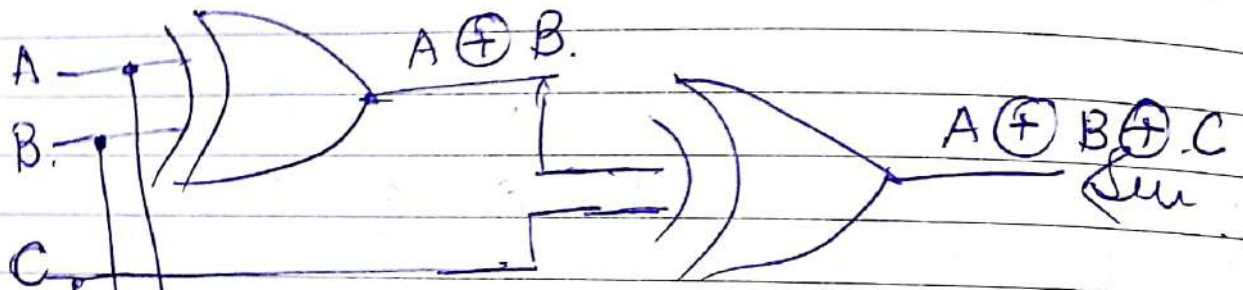
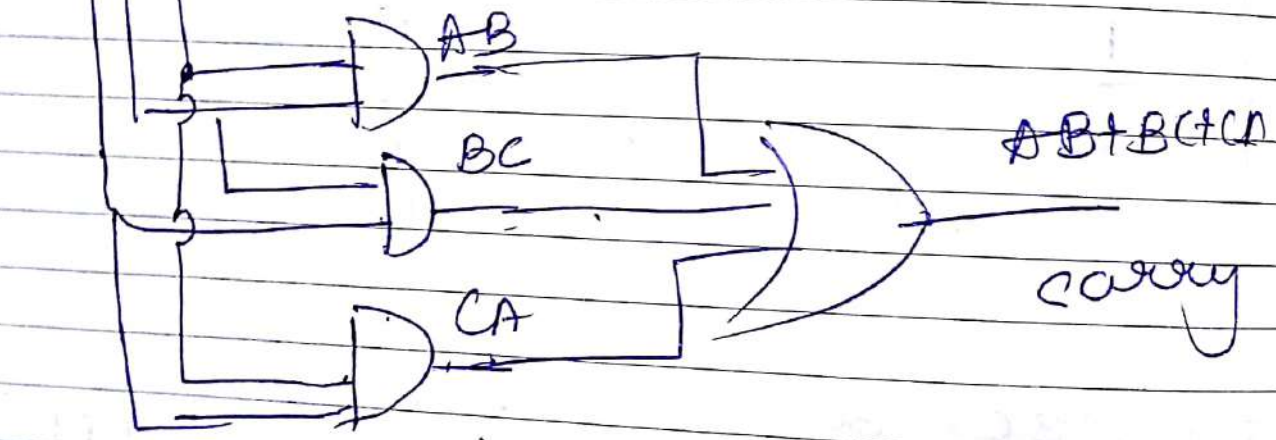
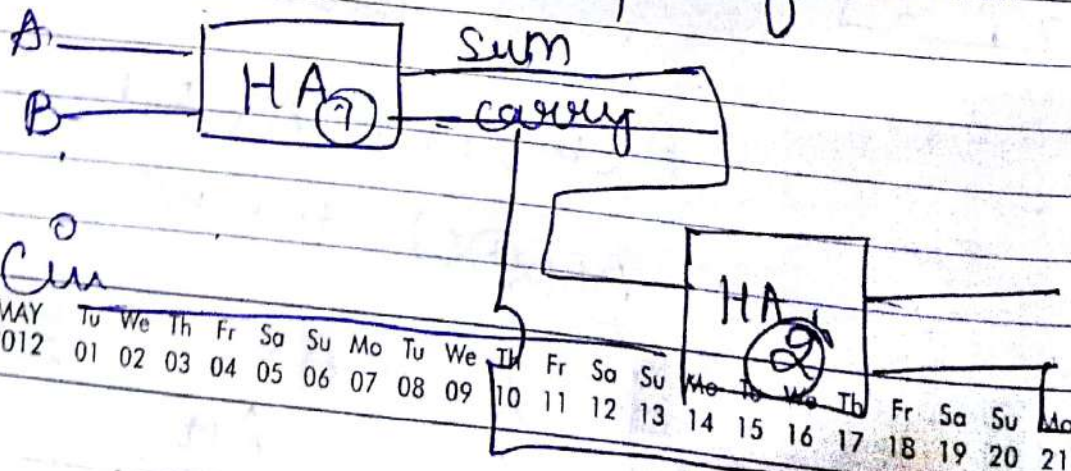


$$Carry = AC + \bar{A}B + BC$$





* Full Adder using Half Adder



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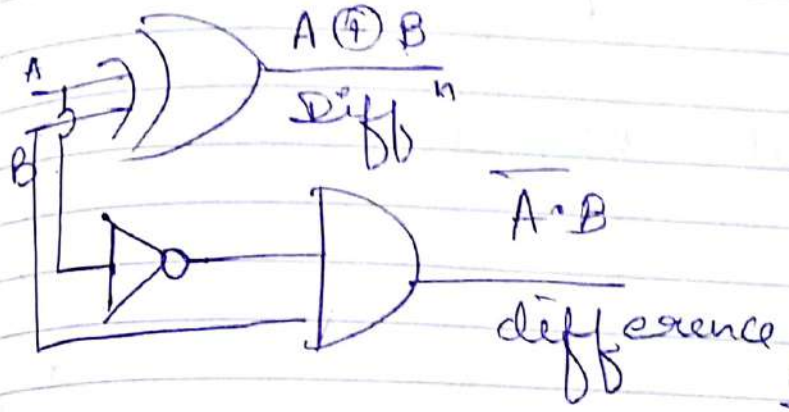
Half Subtractor

A	B	D (Differen)	B (Borrow)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Difference $= \bar{A}B + A\bar{B} = A \oplus B$

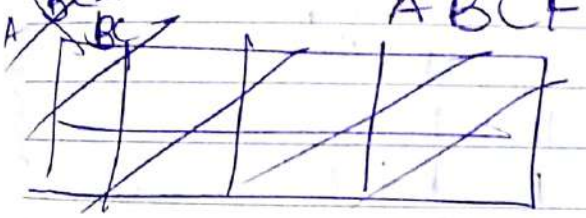
Borrow $= \bar{A}B$



Full Subtractor

I/P			output	
A	B	C	Diff^n	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Diff^n $= \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C}$



$= A \oplus B \oplus C$

Borrow :-

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	B	$B\bar{C}$
$\bar{A}$	0	1	1	1
A	0	0	1	0

Borrow :- $\bar{A}C + \bar{A}B + BC$

$= \bar{A}(B + C) + BC$

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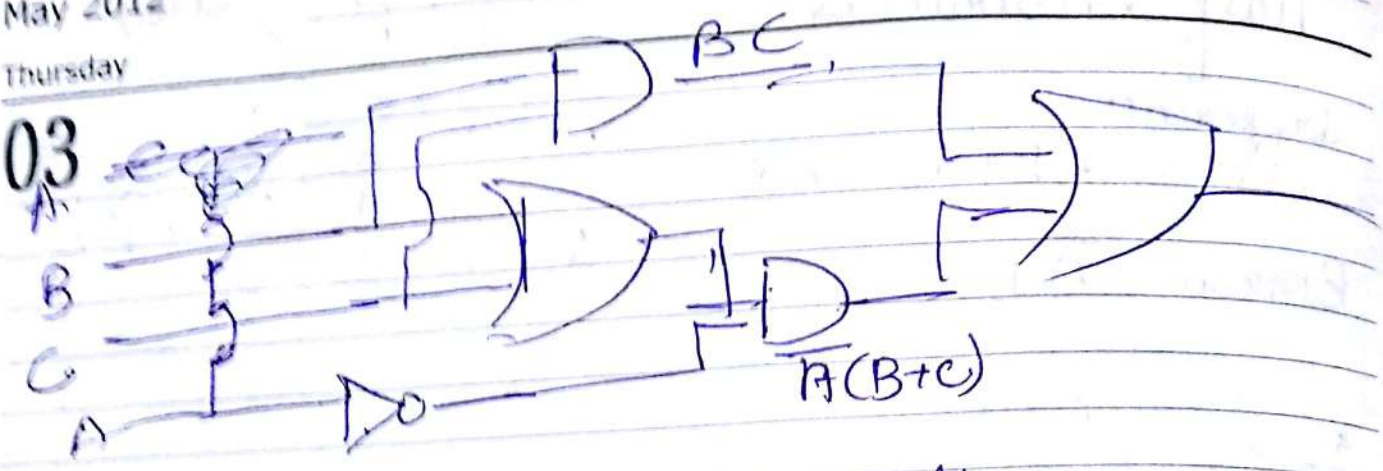

using half subtract make full subtract

Code Converter

A	B	C	D	W	X	Y	Z			
				gray						
0	0	0	0	0	0	0	0	—	0	0
0	0	0	1	0	0	0	1	—	1	1
0	0	1	0	0	0	1	1	—	3	3
0	0	1	1	0	0	1	0	—	3	2
0	1	0	0	0	1	1	0	—	4	6
0	1	0	1	0	1	1	1	—	8	7
0	1	1	0	0	1	0	1	—	6	5
0	1	1	1	0	1	0	0	—	7	4
1	0	0	0	1	1	0	0	—	8	12
1	0	0	1	1	1	0	1	—	9	13
1	0	1	0	1	1	1	1	—	10	15
1	0	1	1	1	1	1	0	—	11	14
1	1	0	0	1	0	1	0	—	12	10
1	1	0	1	1	0	1	1	—	13	11
1	1	1	0	1	0	0	1	—	14	9
1	1	1	1	1	0	0	0	—	15	8

Km map

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$2^1 + 2^0$

gray to bin

0 0 1 1

0 0 1 0

(W)

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	0 (1)	0 (3)	0 (2)
$\bar{A}B$	0 (4)	0 (5)	0 (7)	0 (6)
AB	1 (12)	1 (13)	1 (15)	1 (14)
$A\bar{B}$	1 (8)	1 (9)	1 (11)	1 (10)

$\boxed{W = A}$

(X)

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	0 (1)	0 (3)	0 (2)
$\bar{A}B$	1 (4)	1 (5)	1 (7)	1 (6)
AB	0 (12)	0 (13)	0 (15)	0 (14)
$A\bar{B}$	1 (8)	1 (9)	1 (11)	1 (10)

$X = \bar{A}B + A\bar{B} = A \oplus B$

(Y)

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	0 (1)	1 (3)	1 (2)
$\bar{A}B$	1 (4)	1 (5)	0 (7)	0 (6)
AB	1 (12)	1 (13)	0 (15)	0 (14)
$A\bar{B}$	0 (8)	0 (9)	1 (11)	1 (10)

$Y = B\bar{C} + \bar{B}C = B \oplus C$

(Z)

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	1 (1)	(3)	(2)
$\bar{A}B$	0 (4)	1 (5)	(7)	1 (6)
AB	0 (12)	1 (13)	(15)	1 (14)
$A\bar{B}$	0 (8)	1 (9)	(11)	1 (10)

$Z = \bar{C}D + C\bar{D}B + A\bar{C}\bar{D}$

$C \oplus D$

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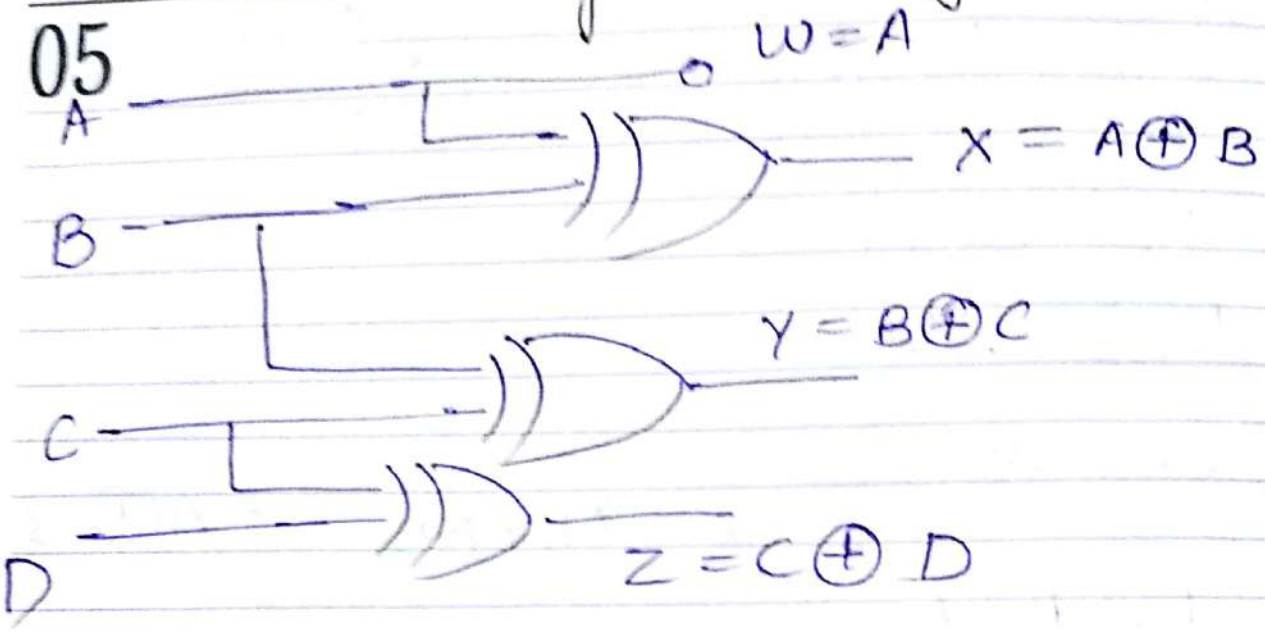
* Gray to binary Code.



* 4 bit Binary to excess 3 BCD

Input — 5 output bit

A	B	C	D	V	W	X	Y	Z
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1	0	1	0	0	1
1	0	1	0	1	0	0	0	0
1	0	1	1	1	0	0	0	1
1	1	0	0	1	0	0	1	0
1	1	0	1	1	0	1	0	0
1	1	1	0	1	0	1	0	1
1	1	1	1					

11 → 000100

10

15

00010101

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| 0 0 |

↓

| 1 0 0 1 |

* $\boxed{\text{BCD to excess 3}}$
* Excess 3 to BCD

Q Design an combinational circuit that except a 3 bit BCD no. and generate an output binary no. equal to the square of the input no.

Multiplexers (Data-Selector)

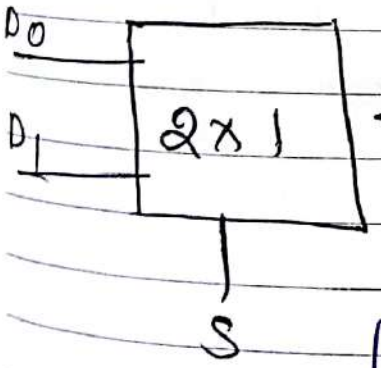
I/P	O/P	Selectline
2×1		1
4×1		2
8×1		3
16×1		4
32×1		5

general :- 2^m

$2^m = n$.

n no. of i/P

m no. of selecline



Output — Y

I/P	Select line S	Output Y
D_1	0	D_0
D_0	1	D_1

$$\boxed{Y = \bar{S} \cdot D_0 + S D_1}$$

$\bar{S}$

$D_0 \cdot 1$

$1 \cdot 1 \Rightarrow 0$

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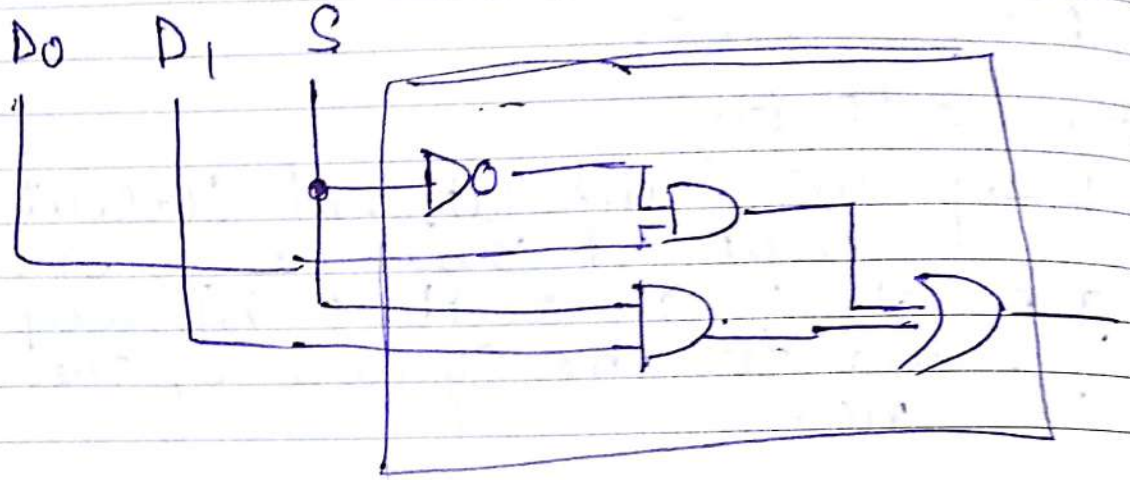
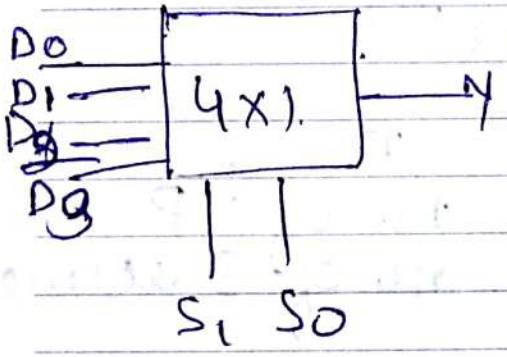
08 / circuit



4x1

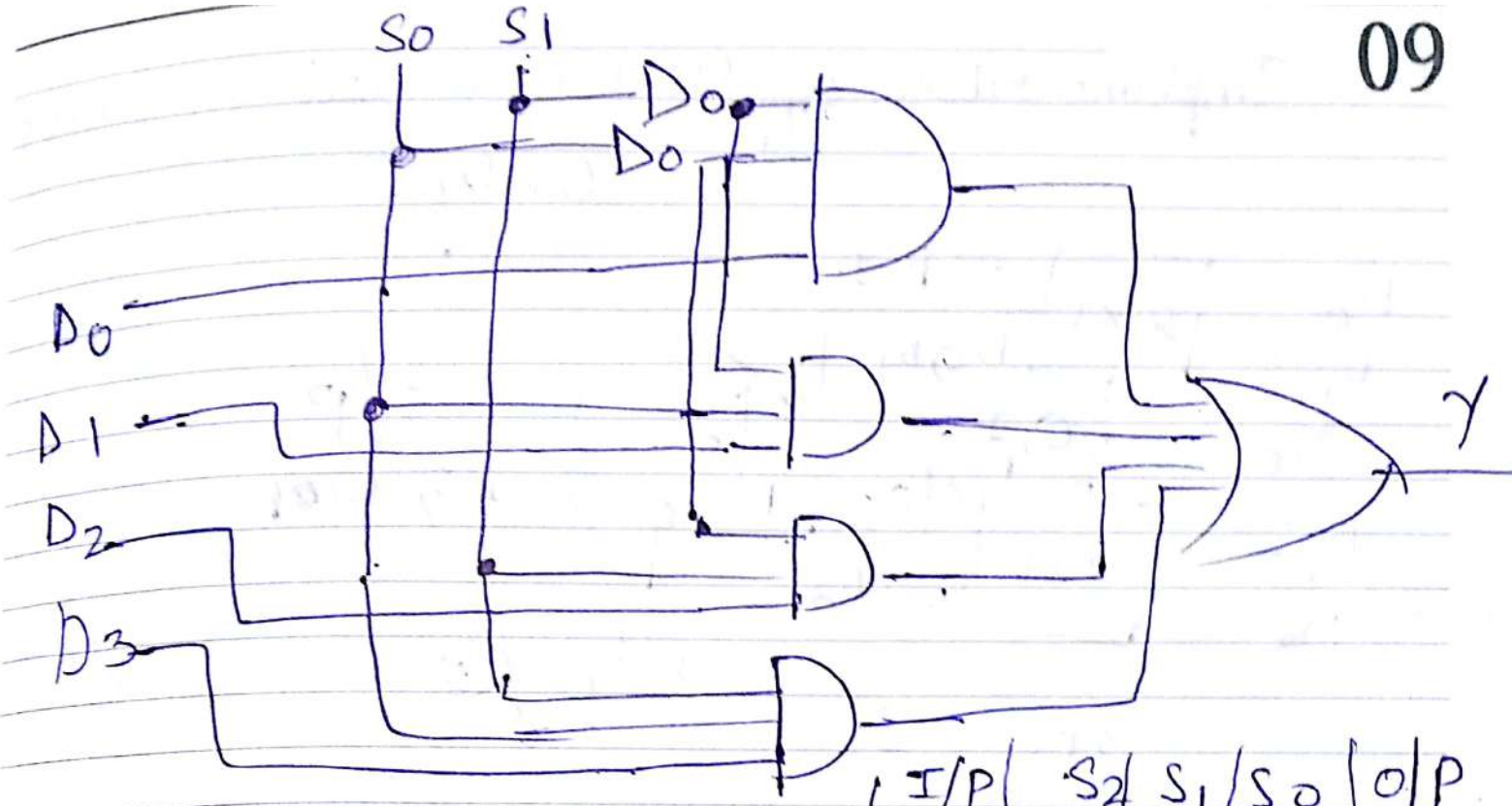


output

I/P	Select line S_0	S_1	Output Y
D0	0	0	D0
D1	0	1	D1
D2	1	0	D2
D3	1	1	D3

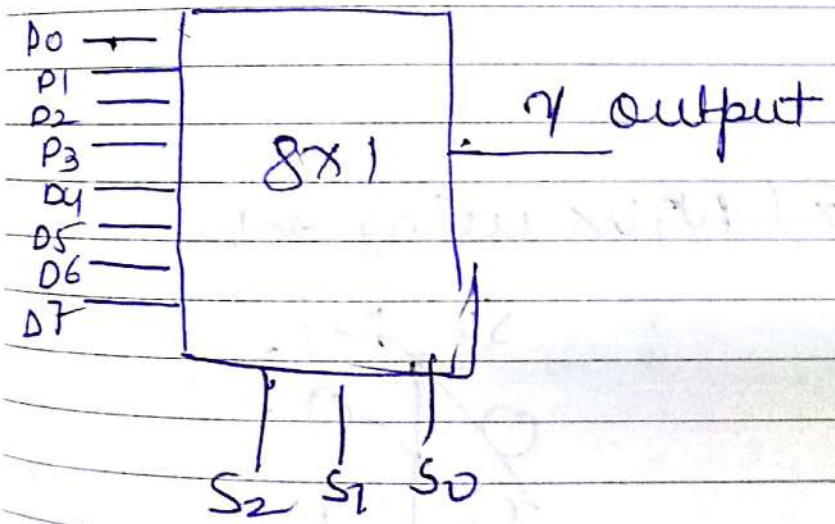
$$Y = \overline{S_0}\,\overline{S_1}\cdot D_0 + \overline{S_0}\,S_1\cdot D_1 + S_0\,\overline{S_1}\cdot D_2 + S_0 S_1\cdot D_3$$

Scanned by CamScanner



I/P	S_2	S_1	S_0	O/P Y
D0	0	0	0	D0
D1	0	0	1	D1
D2	0	1	0	D2
D3	0	1	1	D3
D4	1	0	0	D4
D5	1	0	1	D5
D6	1	1	0	D6
D7	1	1	1	D7

$\boxed{8\times1}$ - MUX



$$Y = \bar{S_2}\,\bar{S_1}\,\bar{S_0}\cdot D_0 + \bar{S_2}\,\bar{S_1}\,S_0\cdot D_1 + \bar{S_2}\,S_1\cdot\bar{S_0}\,D_2 + \bar{S_2}\,S_1\,S_0\,D_3 + S_2\,\bar{S_1}\,\bar{S_0}\,D_4 + S_2\,\bar{S_1}\,S_0\,D_5 +$$

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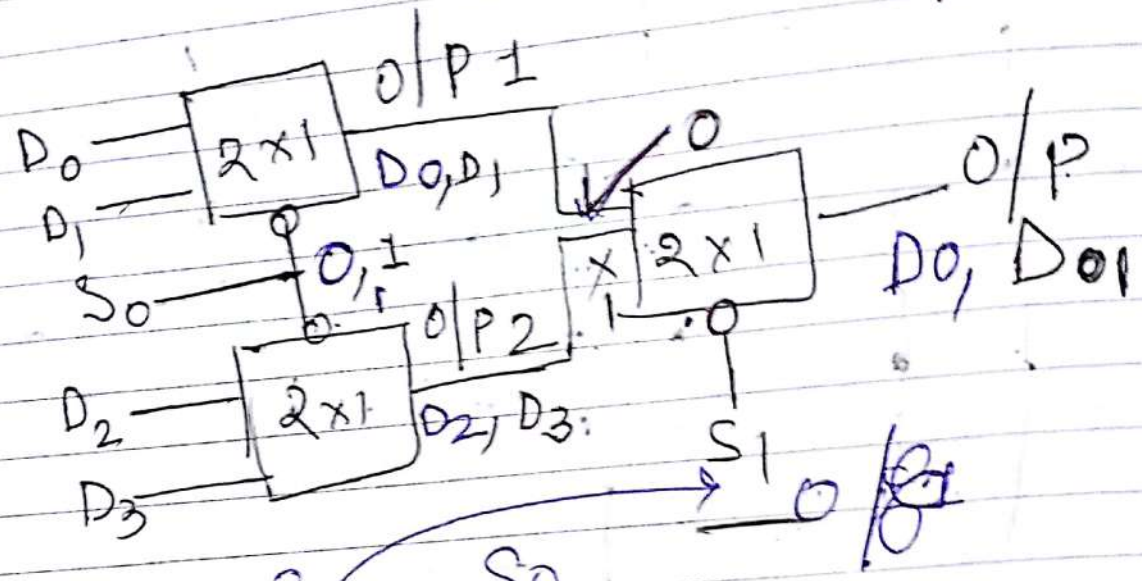
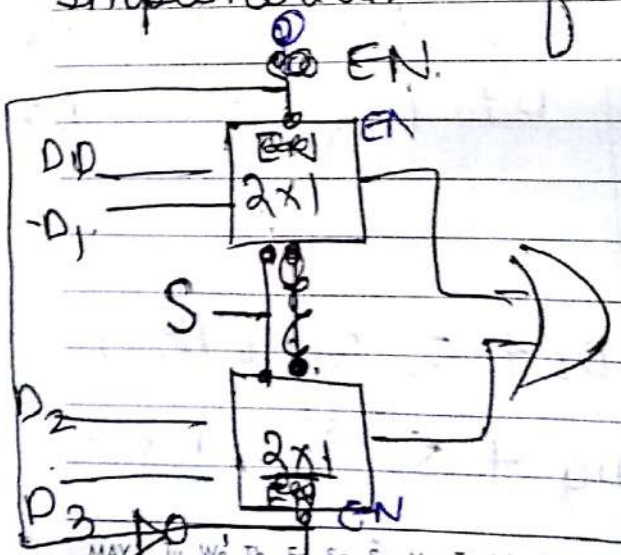
Implementation of 4x1 mux using 2x1 mux only.



	S_1	S_0
D_0	0	0
D_1	0	1
D_2	1	0
D_3	1	1

Implementation of 4x1 MUX using 2x1.



S_0	S_1
0	0
0	1
1	0
1	1

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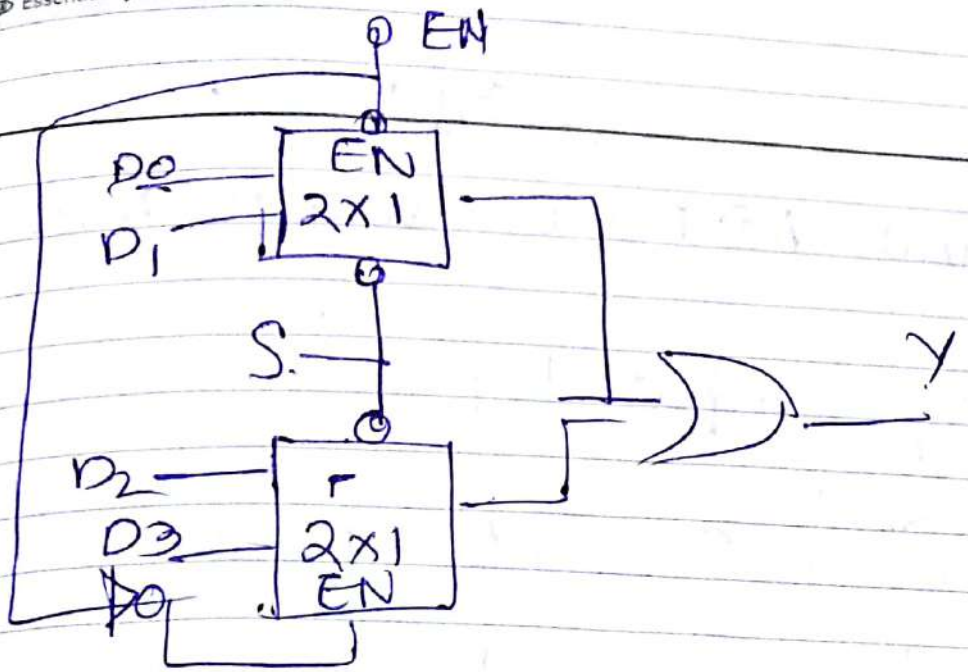
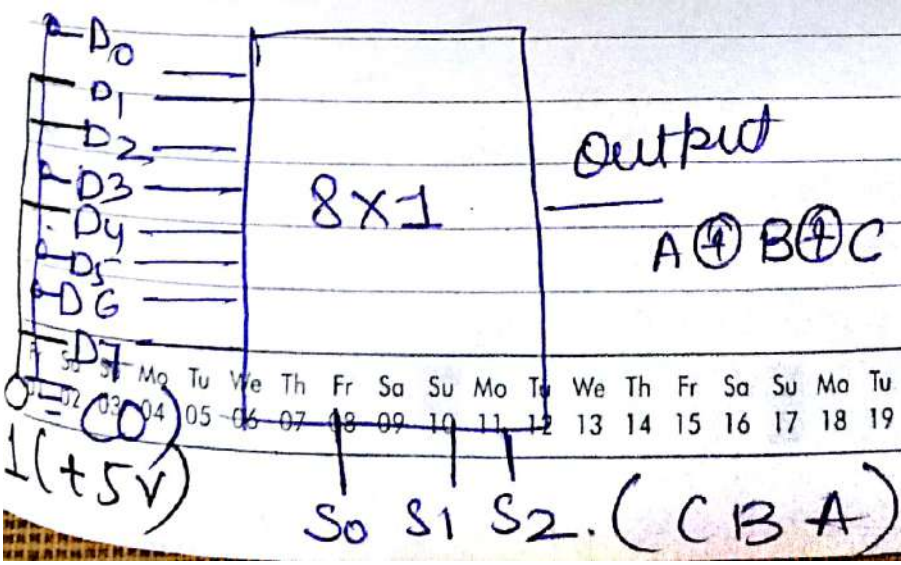


Throw Multiplexer, Implement the function

* Use a MUX to implement. $A \oplus B \oplus C$

S_0 A	S_1 B	S_0 C	F
D_0 0	0	0	0
D_1 0	0	1	1
D_2 0	1	0	1
D_3 0	1	1	0
D_4 1	0	0	1
D_5 1	0	1	0
D_6 1	1	0	0
D_7 1	1	1	1



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May 2012

Saturday

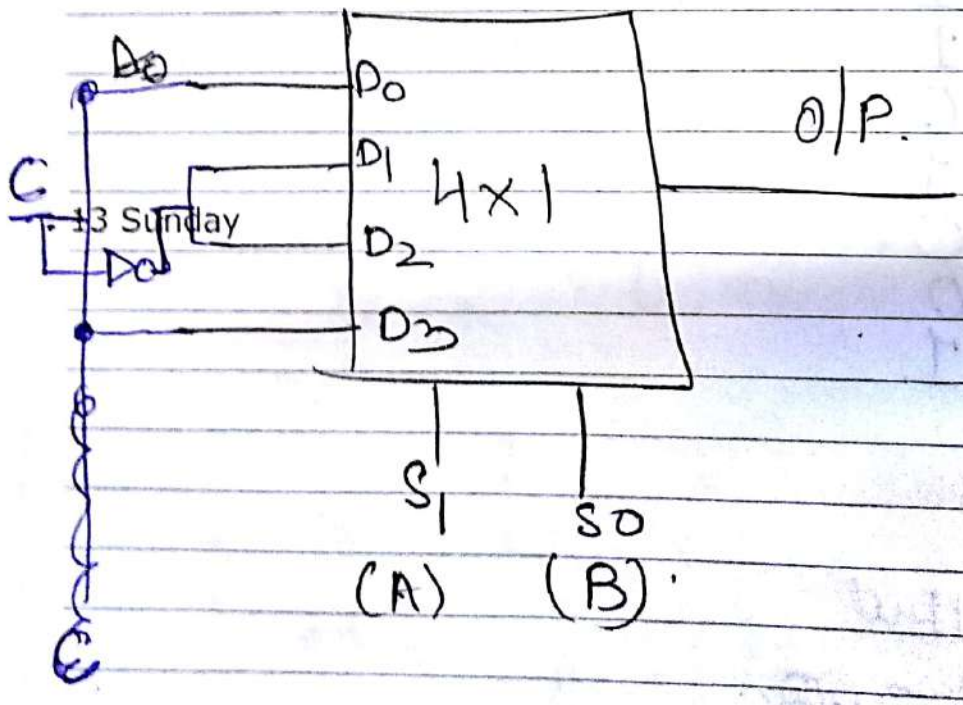
12

$Q = \Sigma_m(1,2,4,7)$

Implement $A \oplus B \oplus C$ using 4×1 mux.

	S_1 (A)	S_0 (B)	Input (C)	F	
D_0 0	0	0	0	0	$F = C$
1	0	0	1	1	
D_1 2	0	1	0	1	$F = \overline{C}$
3	0	1	1	0	
D_2 4	1	0	0	1	$F = \overline{C}$
5	1	0	1	0	
D_3 6	1	1	0	0	$F = C$
7	1	1	1	1	

LCB as a circuit variable / Input



13 Sunday

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Shortcut methode

$\Sigma_m(1,2,4,7)$

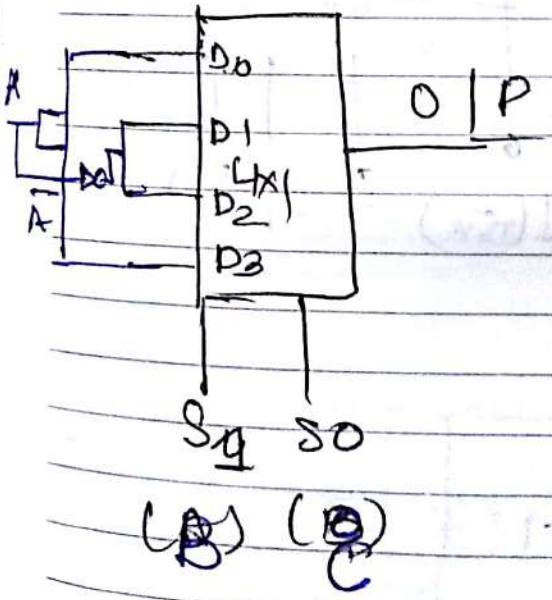
	D_0	D_1	D_2	D_3
$\bar{C}$	0	2	4	6
C	1	3	5	7
	C	$\bar{C}$	$\bar{C}$	C

(*) If two b. both mark 1
If both not mark 0
If one mark, so only variable

Or (If MCB as a input variable)

	D_0	D_1	D_2	D_3
$\bar{A}$	0	1	2	3
A	4	5	6	7
	A	$\bar{A}$	$\bar{A}$	A

$\Sigma_m(1,2,4,7)$



	Input Variable A	S_1 B	S_0 C	F
D_0 0	0	0	0	0
D_1 1	0	0	1	1
D_2 2	0	1	0	1
D_3 3	0	1	1	0
D_0 4	1	0	0	1
D_1 5	1	0	1	0
D_2 6	1	1	0	0
D_3 7	1	1	1	1

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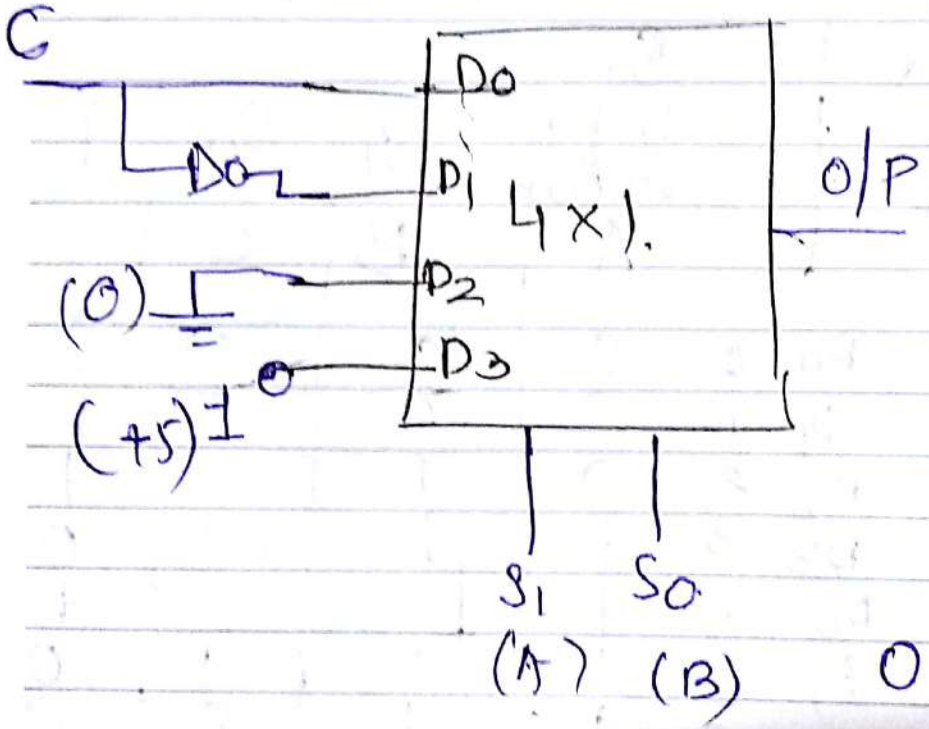
15 Em (1, 2, 6, 7)

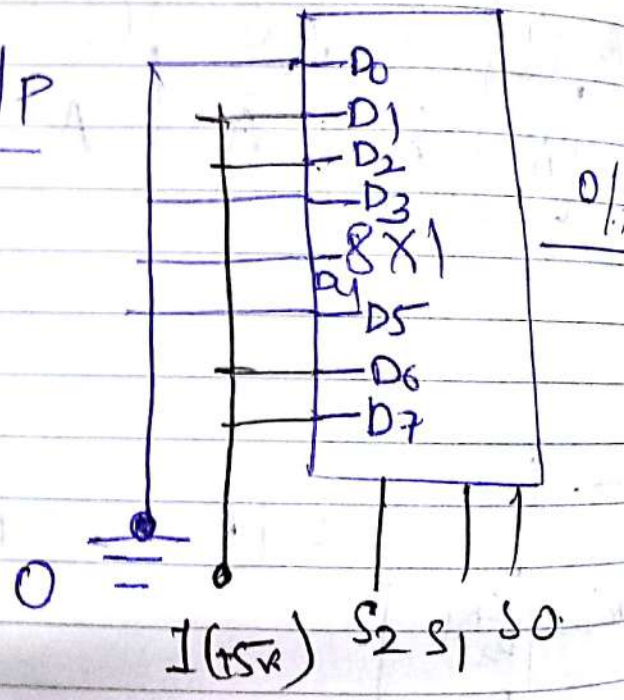
LSB

A	B	C	
D_0	D_1	D_2	D_3
$\bar{C}$	0	2	4	6
C	1	3	5	7
C	$\bar{C}$	0	1

4x1

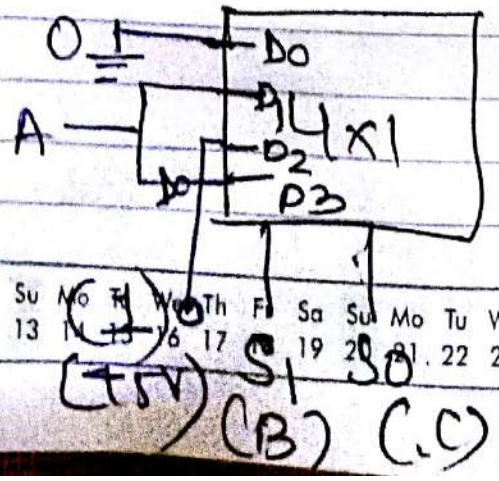
8x1





MSB

	D_0	D_1	D_2	D_3
$\bar{A}$	0	1	2	3
A	4	5	6	7
	0	$\bar{A}$	1	A



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Implement $ab + \bar{b}c$ using 4x1 mux.

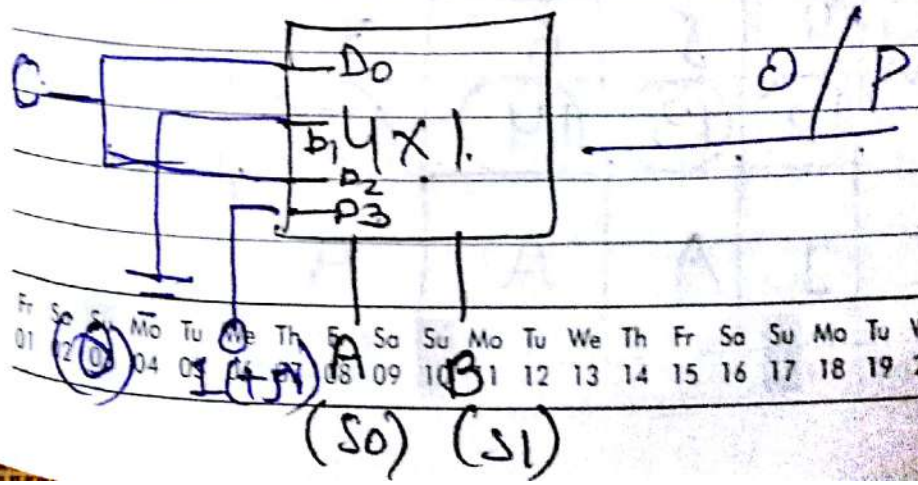
$f = ab + \bar{b}c$

	S0	S1	Input variable		
	A	B	C		
0	0	0	0	0	0·0 + 1·0
1	0	0	1	1	0 + 1·1
2	0	1	0	0	0·1 + 0·0
3	0	1	1	0	0·1 + 0·1
4	1	0	0	0	1·0 + 1·0
5	1	0	1	1	1·0 + 1·1
6	1	1	0	1	1·1 + 0·0
7	1	1	1	1	1·1 + 1·1

D_0 D_1 D_2 D_3

LSB

	D_0	D_1	D_2	D_3
$\bar{C}$	0	2	4	6
C	1	3	5	7
	C	0	C	1

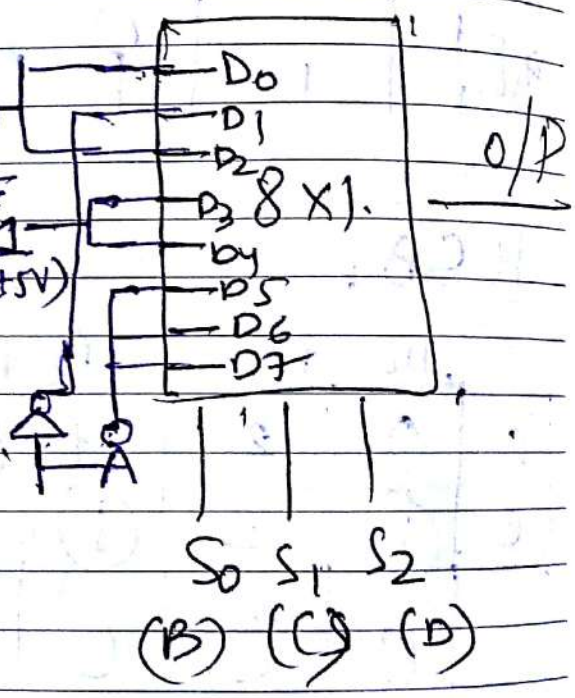


Scanned by CamScanner

Q $\Sigma_m(1, 3, 4, 11, 12, 13, 14, 15)$

Using 8×1.

Input Variable	S_0 A	S_1 B	S_2 C	D	F
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1



MSB

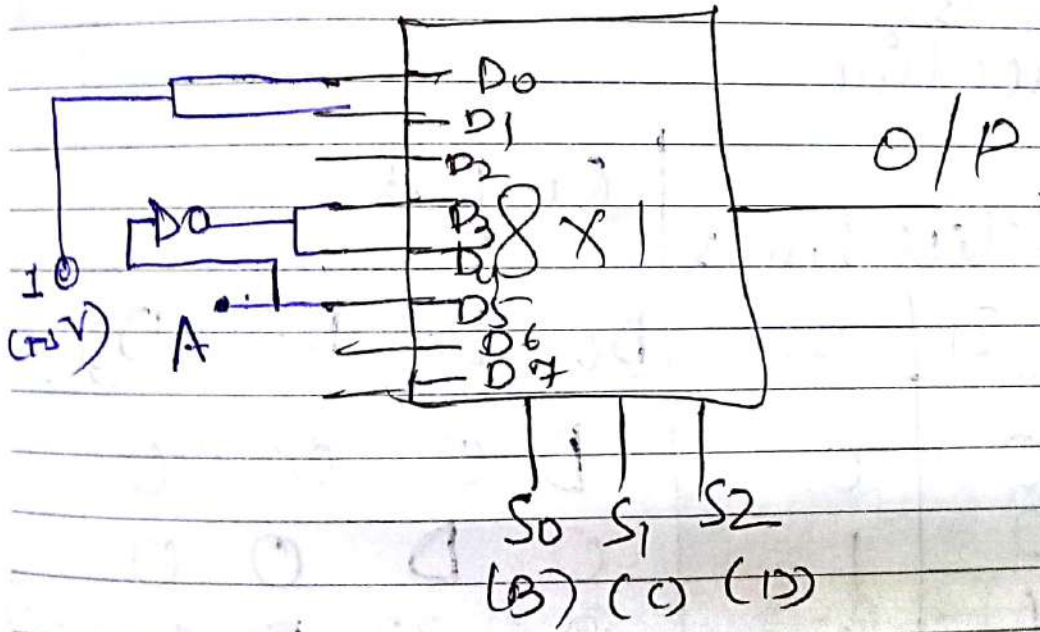
	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	0	$\bar{A}$	0	1	1	A	A	A

Scanned by CamScanner

LSB | MSB

Q. $\Sigma m(0, 1, 3, 4, 8, 9, 15)$

	D_0	D_1	D_2	D_3	D_4			
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	1	1		$\bar{A}$	$\bar{A}$			A



Scanned by CamScanner

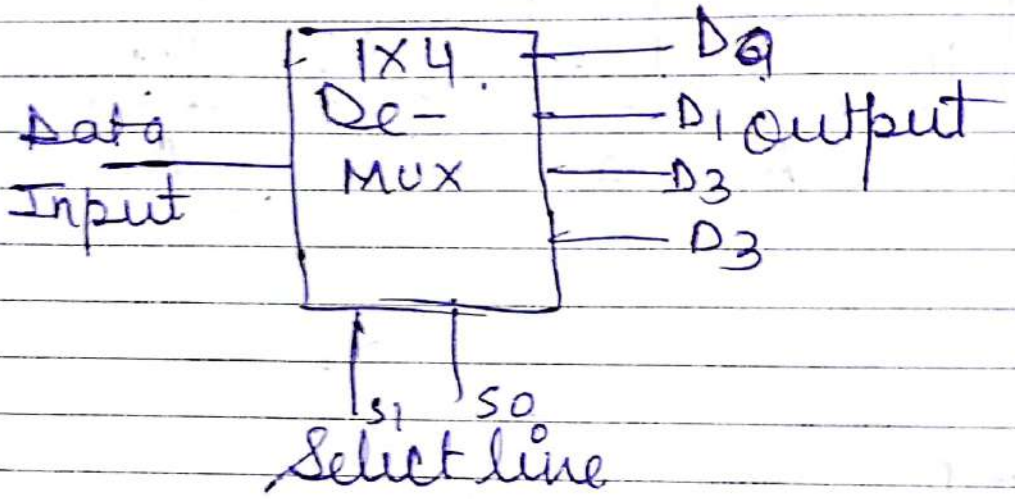
app.cloudeducationerp.com/mcu/

Password : student 1234

college info
↳ course registration
↳ student registrationship

* Demultiplexer

Data Distrubuter



Input D	Select lines S_1	S_0	Output D_0	D_1	D_2	D_3
D	0	0	D	0	0	0
D	0	1	0	D	0	0
D	1	0	0	0	D	0
D	1	1	0	0	0	D

$D_0 = \overline{S_0}\,\overline{S_1}\,D =$

$D_1 = S_0\,\overline{S_1}\,D$

$D_2 = \overline{S_0}\,S_1 D$

$D_3 = S_0\,S_1\,D$

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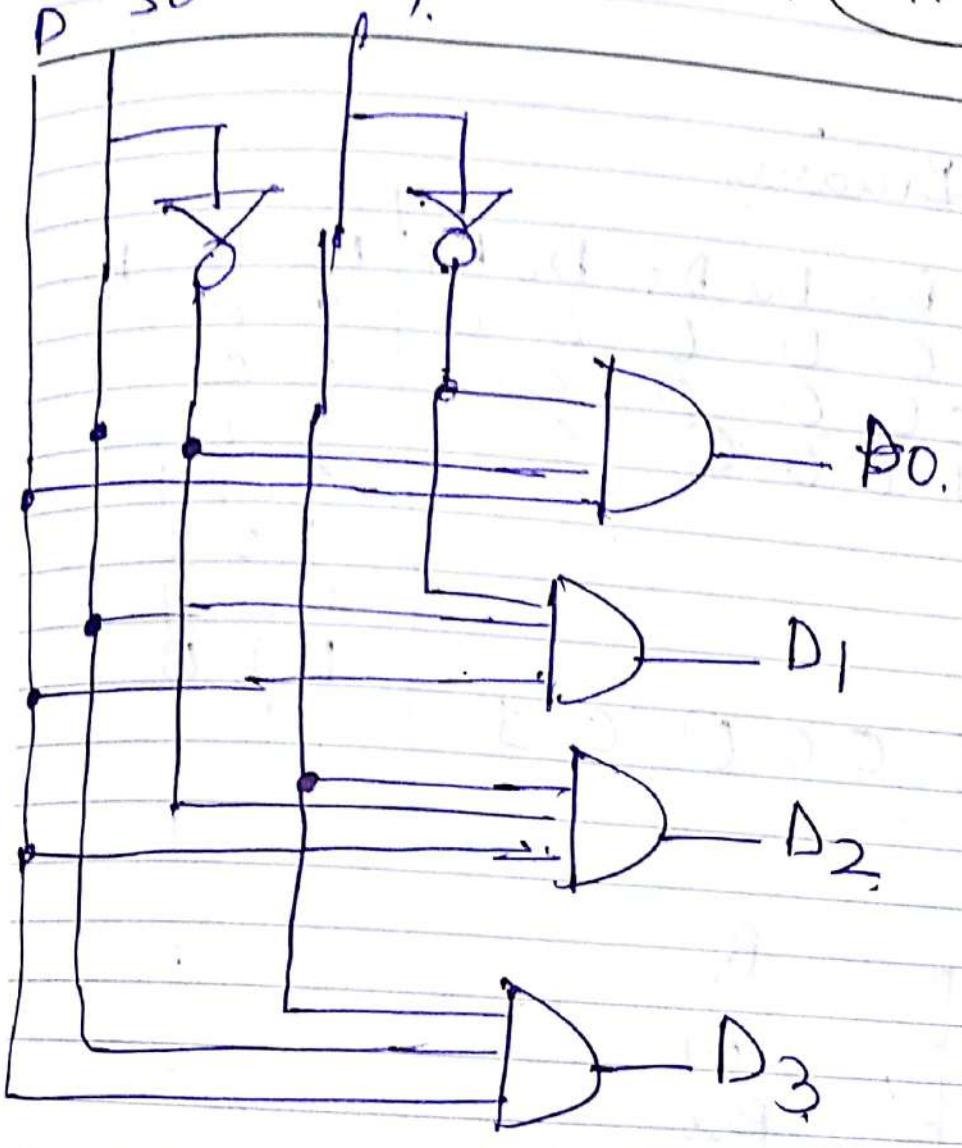
⇒ (1×8)



Encoder :- It encode the Known value into other code.

1) Decimal to BCD encoder (0-9 to BCD (4 bit output))

2) Octal to Binary encoder (0-7 to $B_0 B_1 B_2$)

3) Hexadecimal to Binary encoder (0-15 to Binary)

4) Priority Encoder.

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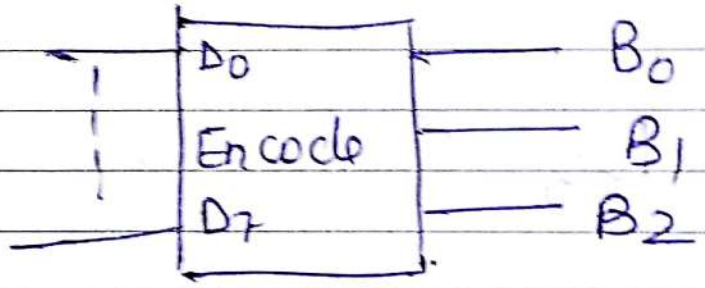
Octal to Binary

Octal	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	B_2	B_1	B_0
0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	1
2	0	0	1	0	0	0	0	0	0	1	0
3									0	1	1
4									1	0	0
5									1	0	1
6									1	1	0
7	0	0	0	0	0	0	0	1	1	1	1



B_0 $\Sigma_m(1, 3, 5, 7)$

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$				
A				

$B_0 = D_1 + D_3 + D_5 + D_7$

$B_1 = D_2 + D_3 + D_6 + D_7$

$B_2 = D_4 + D_5 + D_6 + D_7$

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4 Input Priority encoder

Highest Input — least Priority

D_3	D_2	D_1	D_0	B_1	B_0
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

$B_0 =$

D_3D_2 \ D_1D_0	$\bar{D}_1\bar{D}_0$	$\bar{D}_1D_0$	D_1D_0	$D_1\bar{D}_0$
$\bar{D}_3\bar{D}_2$	X	0	1	1
$\bar{D}_3D_2$	0	0	0	0
D_3D_2	1	1	1	1
$D_3\bar{D}_2$	1	1	1	1

$$B_0 = D_3 + \cancel{\bar{D}_3 D_2 D_1} \; D_1\bar{D}_2$$

00 1 X 1
0 — 0
1 — 1

01 X X
01 0 0 — 4
0 1 — 5
1 0 — 6
1 1 — 7

1 X X X
1 0 0 0
1 1 1 1

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$2^n \rightarrow$ output

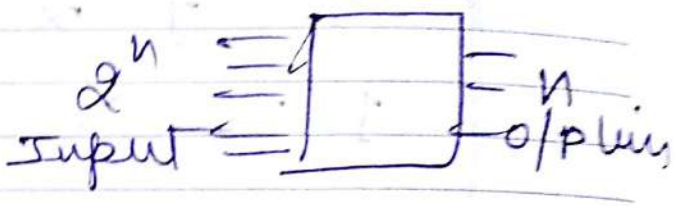
2 — output
4 — Input

B_1

	$\bar{D}_1\bar{D}_0$	$\bar{D}_1 D_0$	$D_1 D_0$	$D_1 \bar{D}_0$
$D_3 D_2$	X	0	0	0
$\bar{D}_3 D_2$	1	1	1	1
$D_3 D_2$	1	1	1	1
$D_3 \bar{D}_2$	1	1	1	1

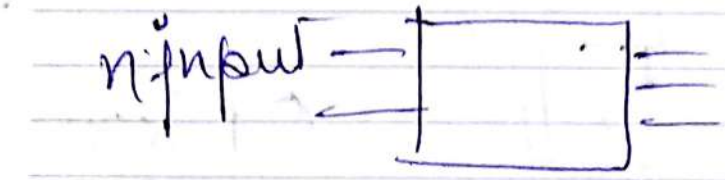
2^n output

$B_1 = D_2 + D_3$



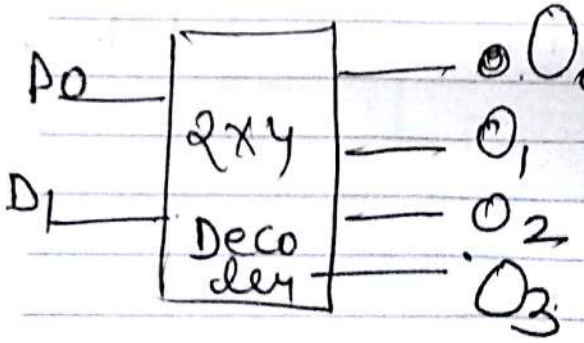
Decoder

2 → Input So 4 Output



(No select lines are required)

2×4 decoder.



D_0	D_1	O_0	O_1	O_2	O_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

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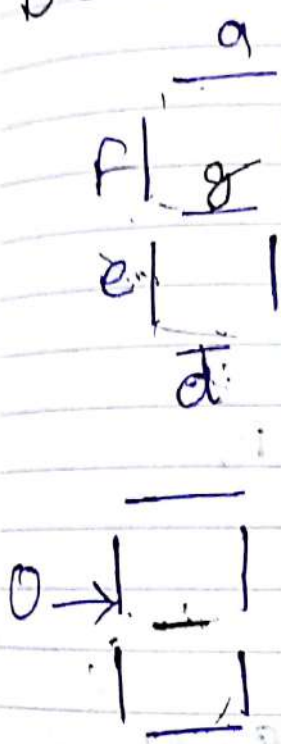
$O_0 = \overline{D_0}\,\overline{D_1}$ ③ 2^n

$O_1 = \overline{D_0}\,D_1$

$O_2 = D_0\,\overline{D_1}$

$O_3 = D_0\,D_1$.

BCD to 7 segment.



is on pie represent zero

2 ⇒

I/P BCD				a	b	c	d	e	f	g	
A	B	C	D								
0	0	0	0	1	1	1	1	1	1	0	— 0
				0	1	1	0	0	0	0	— 1
				1	1	0	1	1	0	1	— 2
				1	1	1	1	0	0	1	— 3
				0	1	1	0	0	1	1	— 4
				1	0	1	1	0	1	1	— 5
				1	0	1	1	1	1	1	— 6
				1	1	1	0	0	0	0	— 7
				1	1	1	1	1	1	1	— 8
				1	1	1	1	0	1	1	— 9

Scanned by CamScanner

7→	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	0	1	1	1

(a)

	$\bar{A}\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	1	1
$\bar{A}B$	0	1	1	1
AB	X	X	X	X
$A\bar{B}$	1	1	X	X

$$a = A + C + BD + \bar{B}\bar{D}$$

(f) $F(A, B, C, D) = A\bar{B} + BD + \bar{B}C\bar{D}$

Implement this fun using 8×1 MUX

A B C D

Scanned by CamScanner

$A\overline{B} + BD + \overline{B}C\overline{D}$

	A	B	C	D	Output
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	1

0+ ·
0·1 + 0·1 + 1·0
0 + 0 + 1·
0 + ·

~~0·1 + 0·0 + 1·1·1~~

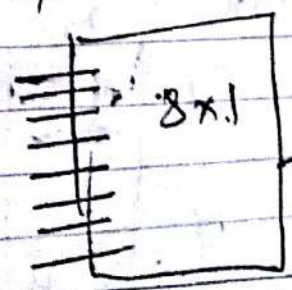
$A\overline{B} \Rightarrow$ 1 000 – 8
01 – 9
10 – 10
11 – 11

$BD \Rightarrow$ 0 1 0 1 – 5
0 1 – 7
1 0 – 13
1 1 – 15

$\overline{B}C\overline{D} \Rightarrow$ 0 0 1 0 ⇒ 2
1 0 1 0 ⇒ 10

MSB

	D0	D1	D2	D3	D4	D5	D6	D7
$\overline{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	A	A	1	A	0	1	0	1



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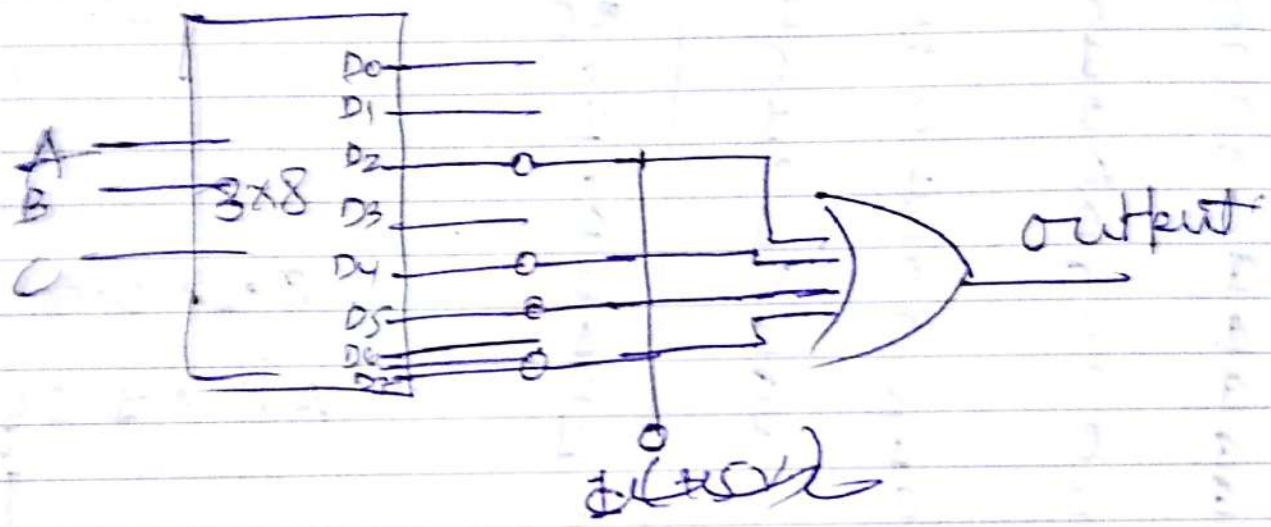
implement using:

Q. 3 : 8 Decoder & basic gates

Sol. $\Sigma m(2, 4, 5, 7)$



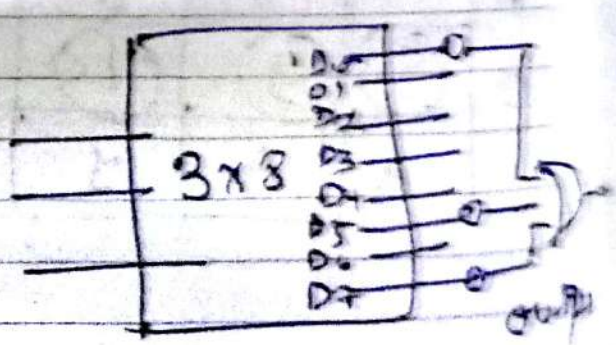
Q. $f(x, y, z) = \bar{x}\bar{y}\bar{z} + xz.$

Sol.

xy \ yz	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{x}\bar{y}$				
$\bar{x}y$				
xy				
$x\bar{y}$				

$\Sigma min \begin{pmatrix} 0 \\ 5 \\ 7 \end{pmatrix}$

x \ yz	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{x}$	1 (0)	1 (1)	(3)	(2)
x	(4)	1 (5)	1 (7)	(6)



Scanned by CamScanner

BCD Adder

BCD Addition :- BCD → 0-9

(1)
```
 +3      0011
  4      0100
         ----
         0111  = 7 valid BCD no carry
no carry
```

(2)
```
  6      0110
 +7      0111
         ----
         1101  — Invalid BCD no
no carry
```

Adding correction factor 6 — 0011.0

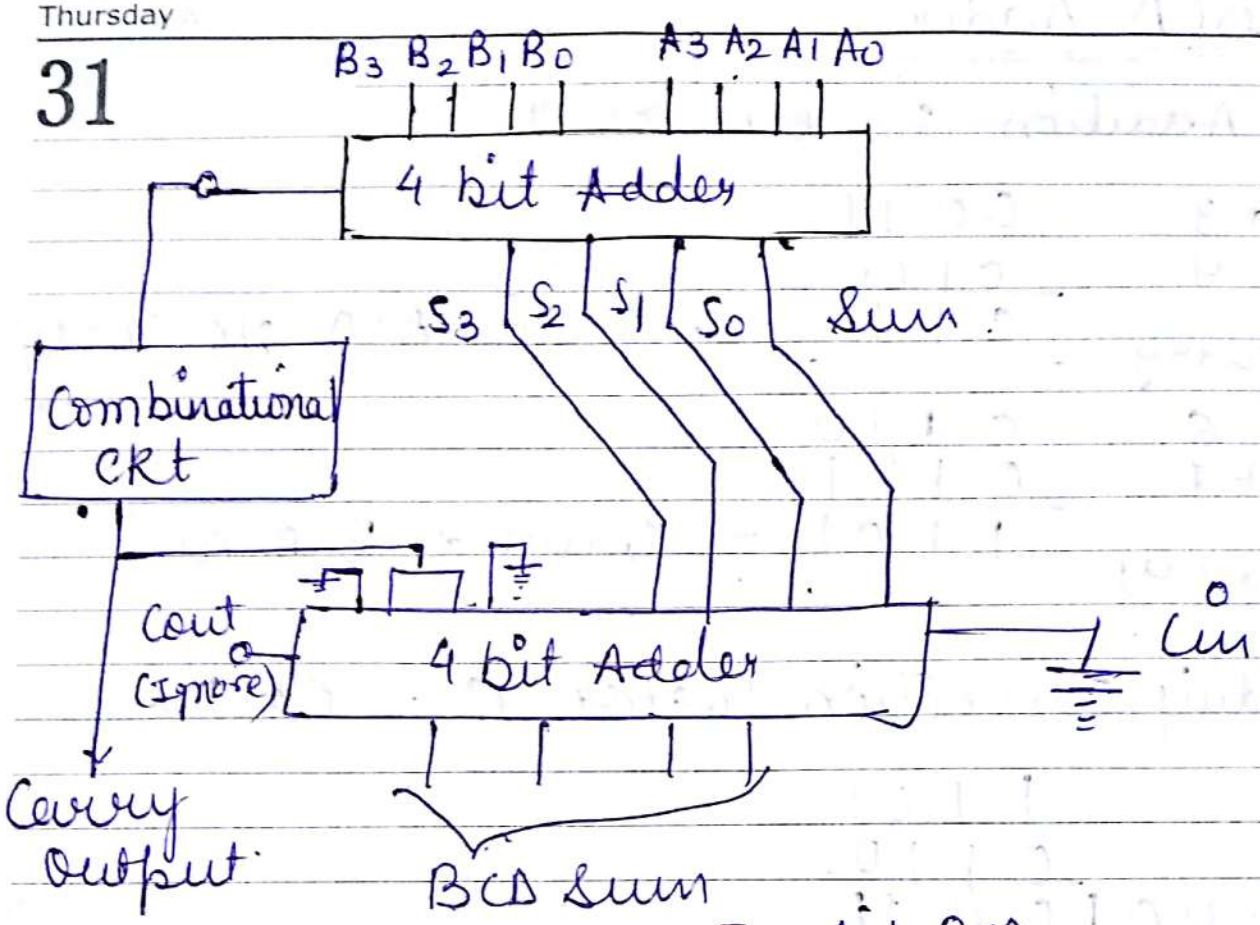
```
         1101
         0110
         ----
0001     0011
 ____    ____
          13
```

(3)
```
 8       1000        10001
+9       1001        00110
         ----        -----
carry ← [1]0001      0001 0111
                      ____ ____
                       1    7
```

If carry generate add correction factor directly

If no carry — (1) valid no.
(2) Invalid no.

Scanned by CamScanner



Invalid BCD

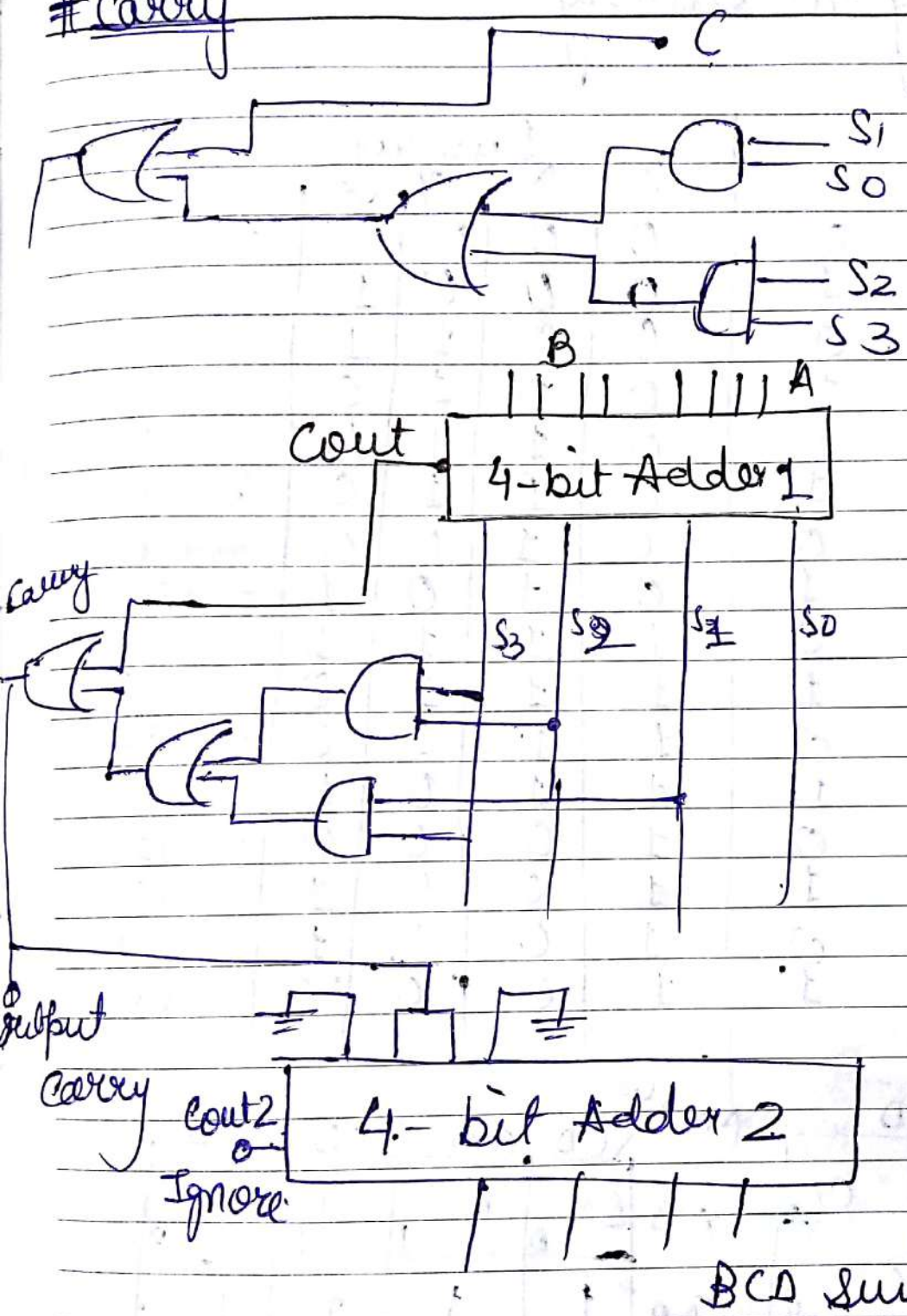
	S_3	S_2	S_1	S_0	O/P (Y)
0					0
1					0
2					0
3					0
9	1	0	0	1	
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

	$\bar{S}_1\bar{S}_0$	$\bar{S}_1 S_0$	$S_1 S_0$	$S_1\bar{S}_0$
$\bar{S}_2\bar{S}_3$	0	0	0	0
$\bar{S}_2 S_3$	0	0	0	0
$S_2 S_3$	1	1	1	1
$S_2\bar{S}_3$	0	0	1	1

$$Y = S_3 S_2 + S_1 S_3$$

Scanned by CamScanner

Carry



Scanned by CamScanner

Gray to Binary

Gray A	B	C	D	Binary W	X	Y	Z	
0	0	0	0	0	0	0	0	— 0
0	0	0	1	0	0	0	1	— 1
0	0	1	0	0	0	1	1	— 2
0	0	1	1	0	0	1	0	— 3
0	1	0	0	0	1	1	1	— 4
0	1	0	1	0	1	1	0	— 5
0	1	1	0	0	1	0	0	— 6
0	1	1	1	0	1	0	1	— 7
1	0	0	0	1	1	1	1	— 8
1	0	0	1	1	1	1	0	— 9
1	0	1	0	1	1	0	0	— 10
1	0	1	1	1	1	0	1	— 11
1	1	0	0	1	0	0	0	— 12
1	1	0	1	1	0	0	1	— 13
1	1	1	0	1	0	1	1	— 14
1	1	1	1	1	0	0	0	— 15

08 Sunday

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	0 (1)	0 (3)	0 (2)
$\bar{A}B$	0 (4)	0 (5)	0 (7)	0 (6)
AB	1 (12)	1 (13)	1 (15)	1 (14)
$A\bar{B}$	1 (8)	1 (9)	1 (11)	1 (10)

$W = A$

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	0 (1)	0 (3)	0 (2)
$\bar{A}B$	1 (4)	1 (5)	1 (7)	1 (6)
AB	0 (12)	0 (13)	0 (15)	0 (14)
$A\bar{B}$	1 (8)	1 (9)	1 (11)	1 (10)

$A\bar{B} + \bar{A}B$

$A \oplus B$

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Y

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	0 (1)	1 (3)	1 (2)
$\bar{A}B$	1 (4)	1 (5)	0 (7)	0 (6)
AB	0 (12)	0 (13)	0 (15)	1 (14)
$A\bar{B}$	1 (8)	1 (9)	0 (11)	0 (10)

$$Y = \bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + AB\bar{C}\bar{D}$$

Z

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0 (0)	1 (1)	1 (3)	0 (2)
$\bar{A}B$	1 (4)	0 (5)	1 (7)	0 (6)
AB	0 (12)	1 (13)	0 (15)	1 (14)
$A\bar{B}$	1 (8)	0 (9)	1 (11)	0 (10)

$$Z = \bar{A}\bar{B}D + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD +$$

X X

3 bit Gray to Binary

Gray A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Binary W	X	Y	
0	0	0	0
0	0	1	1
0	1	1	2
0	1	0	3
1	1	1	4
1	1	0	5
1	0	0	6
1	0	1	7

Scanned by CamScanner

W

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	0	0	0
A	1	1	1	1

$W = A$

X

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	0	1	1
A	1	1	0	0

$X = \bar{A}B + A\bar{B}$

$A \oplus B$

Y

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	1	0	1
A	1	0	1	0

$Y = A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C}$

$\bar{B}C + B\bar{C} = X$

$\bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$

$\bar{A}(X) + A(\bar{X})$

$= \bar{A} \oplus X$

$A \oplus B \oplus C$

Binary to Gray

Binary A	B	C	Gray W	X	Y	
0	0	0	0	0	0	0
0	0	1	0	0	1	1
0	1	0	0	1	1	3
0	1	1	0	1	0	2
1	0	0	1	1	0	
1	0	1	1	1	1	
1	1	0	1	0	1	
1	1	1	1	0	0	

Scanned by CamScanner

W

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0_0	0_1	0_3	0_2
A	1_4	1_5	1_7	1_6

$NV = A$

X

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0_0	0_1	1_3	1_2
A	1_4	1_5	0_7	0_6

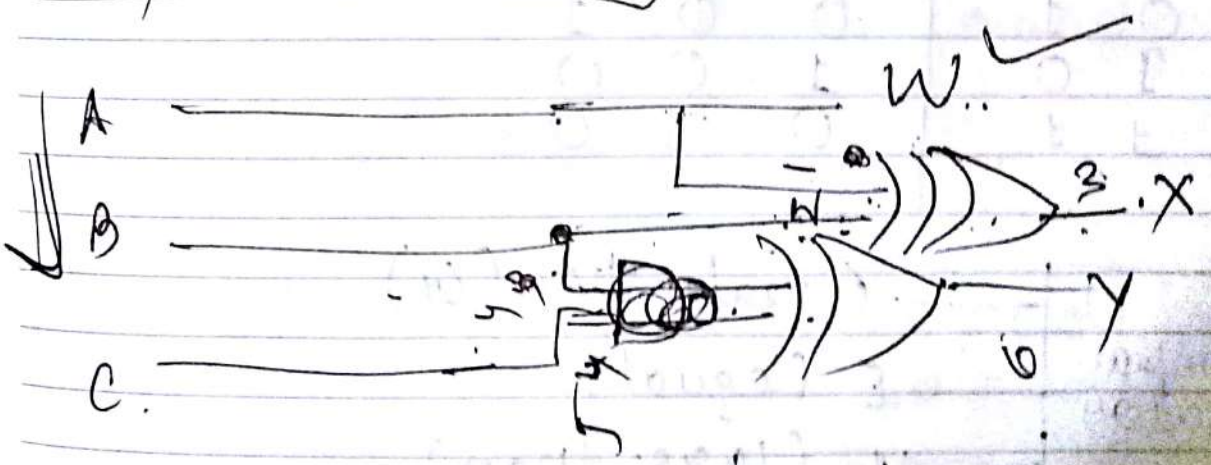
$A\bar{B} + \bar{A}B = A \oplus B = X$

Y

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	1	0	1
A	0	1	0	1

$Y = \bar{B}C + B\bar{C}$

$\boxed{Y = B \oplus BC}$



$\overline{A \cdot B}$

Scanned by CamScanner

07 Comparator :-

To compare the two bits

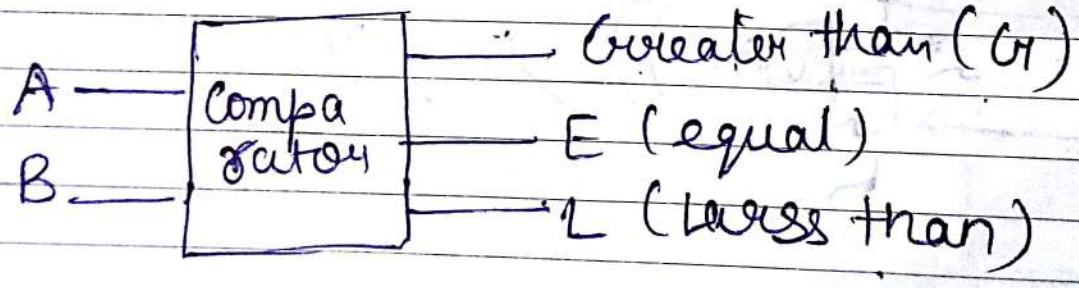
1. 1 bit Comparator
2. 2 bit Comparator
3. 3 bit Comparator
4. 4 bit Comparator

X NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(1) 1 bit Comparator

	Input		Output		
	A	B	G	E	L
Compare A & B.	0	0	0	1	0
	0	1	0	0	1
	1	0	1	0	0
	1	1	0	1	0

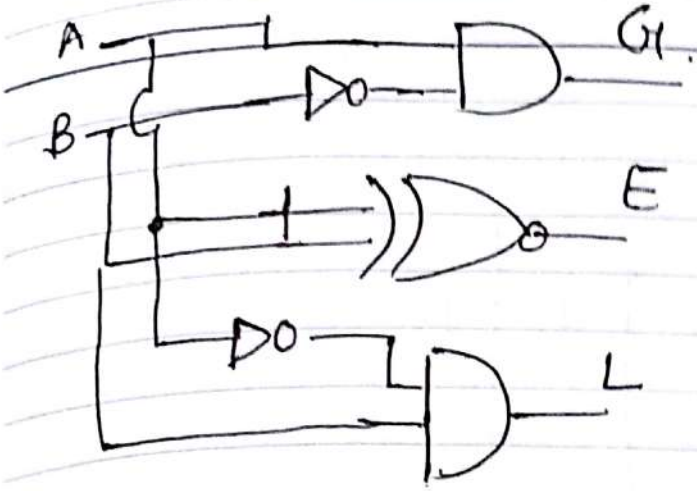


$E \Rightarrow \overline{A}\,\overline{B} + AB \Rightarrow A \odot B$

$G \Rightarrow A\overline{B}$

$L \Rightarrow \overline{A}B$

Scanned by CamScanner



Two bit Comparator

$\overline{A}\,\overline{B} + A\,B$

00 11

① $A > B$ (G) $\Rightarrow$ If $A_1 = 1$, $B_1 = 0$ or
A_1 & B_1 Coincide $A_0 = 1$, $B_0 = 0$

$$G = A_1 \overline{B_1} + (A_1 \odot B_1) A_0 \overline{B_0}$$

② Equal $\Rightarrow$ If A_1 & B_1 coincide and
A_0 & B_0 Coincide

$$E = (A_1 \odot B_1)(A_0 \odot B_0)$$

③ less than $\Rightarrow$ If $A_1 = 0$, $B_1 = 1$ or
A_1 & B_1 coincide $A_0 = 0$, $B_0 = 1$

$$L = \overline{A_1} B_1 + (A_1 \odot B_1) \overline{A_0} B_0$$

Scanned by CamScanner

Truth Table

A Input

A		B		G	E	L	
A_1	A_0	B_1	B_0				
0	0	0	0	0	1	0	— 0
0	0	0	1	0	0	1	— 1
0	0	1	0	0	0	1	— 2
0	0	1	1	0	0	1	— 3
0	1	0	0	1	0	0	— 4
0	1	0	1	0	1	0	— 5
0	1	1	0	0	0	1	— 6
0	1	1	1	0	0	1	— 7
1	0	0	0	1	0	0	— 8
1	0	0	1	1	0	0	— 9
1	0	1	0	0	1	0	— 10
1	0	1	1	0	0	1	— 11
1	1	0	0	1	0	0	— 12
1	1	0	1	1	0	0	— 13
1	1	1	0	1	0	0	— 14
1	1	1	1	0	1	0	— 15

G

A_1A_0 \ B_1B_0	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	$B_1\bar{B}_0$	B_1B_0
$\bar{A}_1\bar{A}_0$	0	0	0	0
$\bar{A}_1A_0$	1	0	0	0
$A_1\bar{A}_0$	1	1	0	1
A_1A_0	1	0	0	1

quad 1 = $A_1\bar{B}_1$

Pair 1 = $A_1A_0\bar{B}_0$

Pair 2 = $\bar{B}_1\bar{B}_0A_0$

$$G = A_1\bar{B}_1 + A_1A_0\bar{B}_0 + \bar{B}_1\bar{B}_0A_0$$

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$G = A_1\bar{B}_1 + A_0\bar{B}_0(\bar{B}_1 + A_1)$

E

	$\bar{B}_1\bar{B}_0$	$\bar{B}_1 B_0$	$B_1 B_0$	$B_1\bar{B}_0$
$\bar{A}_1\bar{A}_0$	1	0	0	0
$\bar{A}_1 A_0$	0	1	0	0
$A_1 A_0$	0	0	1	
$A_1\bar{A}_0$	0	0	0	1

$E = \bar{A}_1\bar{A}_0\bar{B}_1\bar{B}_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 A_0 B_1 B_0 + A_1\bar{A}_0 B_1\bar{B}_0$

$\bar{A}_1\bar{B}_1(\bar{A}_0\bar{B}_0 + A_0 B_0) + A_1 B_1(A_0 B_0 + \bar{A}_0\bar{B}_0)$

$\bar{A}_1\bar{B}_1(A_0 \odot B_0) + A_1 B_1(A_0 \odot B_0)$

$(A_0 \odot B_0)(\bar{A}_1 + \bar{B}_1 + A_1 B_1)$

$(A_0 \odot B_0)(A_1 \odot B_1)$

L

	$\bar{B}_1\bar{B}_0$	$\bar{B}_1 B_0$	$B_1 B_0$	$B_1\bar{B}_0$
$\bar{A}_1\bar{A}_0$	0	1	1	1
$\bar{A}_1 A_0$	0	0	1	1
$A_1 A_0$	0	0	0	0
$A_1\bar{A}_0$	0	0	1	0

$L = \bar{A}_1 B_1 + \bar{A}_1\bar{A}_0 B_0 + \bar{A}_0 B_1 B_0$

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3 bit comparator

A	B
$A_2\ A_1\ A_0$	$B_2\ B_1\ B_0$

$A > B$: (G) $\Rightarrow$ $A_2 = 1$, $B_2 = 0$ or

A_2 & B_2 coincide and $A_1 = 1, B_1 = 0$

or

A_2 & B_2 coincide ; A_1 & B_1 coincide

$A_0 = 1$, $B_0 = 0$

$$G = \overline{A_2}\,\overline{B_2} + A_2 \odot B_2 (A_1 \overline{B_1}) + (A_2 \odot B_2)(A_1 \odot B_1) A_0 \overline{B_0}$$

$A < B$:- (L) $\Rightarrow$ $A_2 = 0$, $B_2 = 1$ or A_2 & B_2 coincide

and $A_2 = 0$, $B_2 = 1$ or A_2 & B_2 coincide

A_1 & B_1 coincide $A_0 = 0$, $B_0 = 1$:

$$L = \overline{A_2} B_2 + A_2 \odot B_2 (\overline{A_2} B_2) + (A_2 \odot B_2)(A_1 \odot B_1) \overline{A_0} B_0$$

$E(A = B) \Rightarrow$ A_2 & B_2 coincide and A_1 & B_1 coincide and

A_0 & B_0 coincide

$$(A_2 \odot B_2)(A_1 \odot B_1)(A_0 \odot B_0)$$

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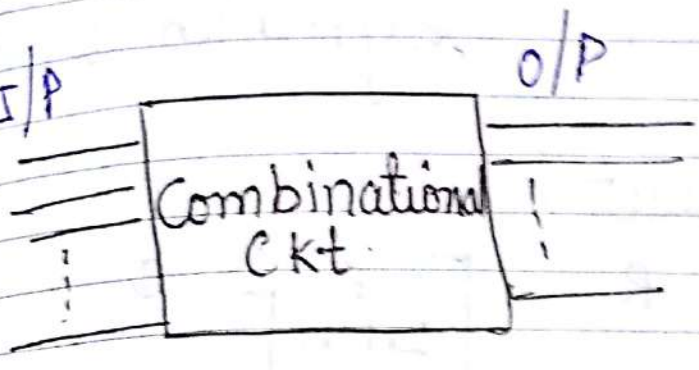
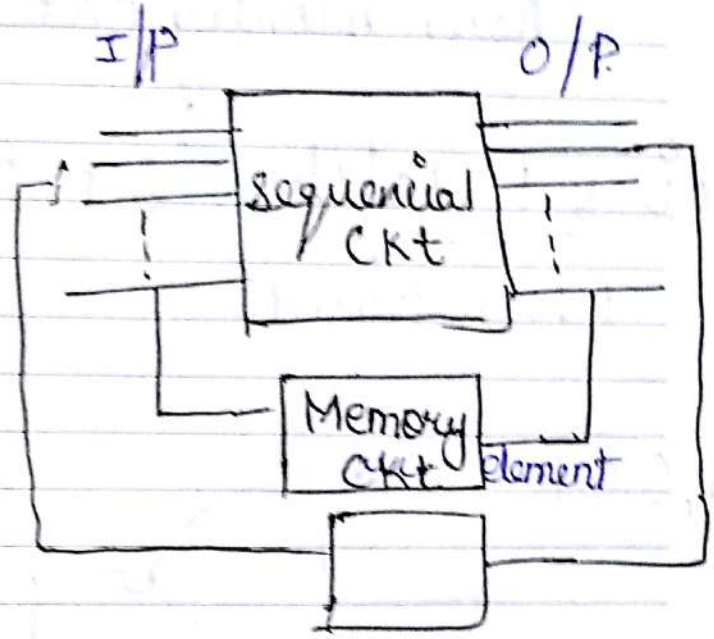
Unit :- 5

Sequential Circuits :-





Types of Sequential CKT

1. Synchronous SCKt
2. Asynchrous SCKt

(1) Are those CKt response to external signal ~~separate~~ by Clock CKT (pulse).
Simultaneously. (slowest device can perform task this much of clock pluse is present)

(2)

→ Are those CKt rupone to the external signal immediately with ~~using~~ dependency on the clock pluse.
(no external response signal)

→ It is ~~slower~~ faster than synchronous

→ Disadvantage
CKt may be unstable due to different propogation delay of input CKt.

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June 2012
Thursday

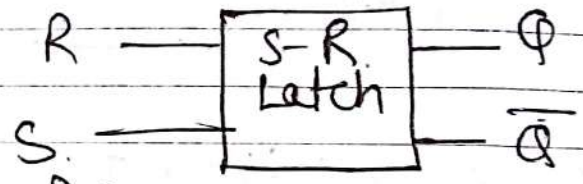
Memory element :-

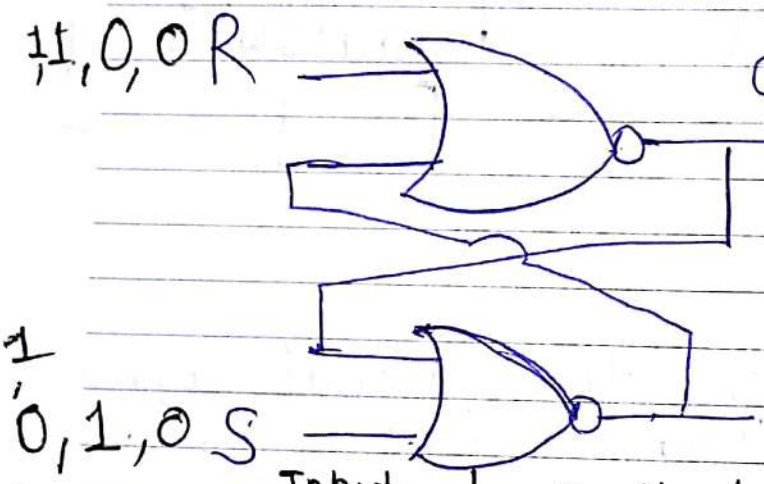
14 (1) Latch — Asynchronosly CKt

(2) Flip-flop (clock Latch) — Synchronous CKt

(i) S-R latch (Set-Reset)

(NOR Based)





P.S	N.S	
Q = 0, 1	0, 1	— ①
0, 1	0, 1, 1	— ②
0, 1	0, 0	— ③
1, 0	1, 0	— ③
1, 0	0, 0	— ②
$\overline{Q}$ = 1, 0	1, 0	— ①

1 0

0 0

Input R	Input S	Output Q_n	Output $\overline{Q}_{n+1}$	Remark (Action)
0	0	Q_n	Q_n	No Change
0	1	X	1	Set
1	0	X	0	Reset
1	1	Not allow	Not allow	Invalid or Forbidden or Prohibited

NOR Gate

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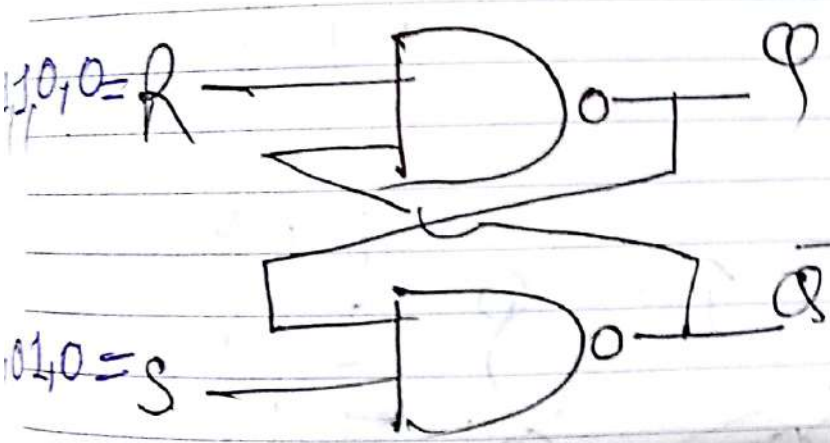
R	S	Qn	Qn+1	
0	0	0	0	No change
0	0	1	1	
0	1	0	1	Set
0	1	1	1	
1	0	0	0	Reset
1	0	1	0	
1	1	0	0	
1	1	1	0	

NAND

0	0	1
0	1	1
1	0	1
1	1	0

NAND Based S-R Latch



P.S	N.S	P.S	N.S	P.S	N.S
0	1	0	1	0	0
1	1	1	1	1	0
1	1	1	0	1	1
0	1	0	0	0	1

R	S	Qn	Qn+1	Action
0	0	Not allowed	Not allowed	Invalid
0	1	X	1	Set
1	0	X	0	Reset
1	1	Qn	Qn	No change

P.S	N.S
0	0
1	1
1	1
0	0

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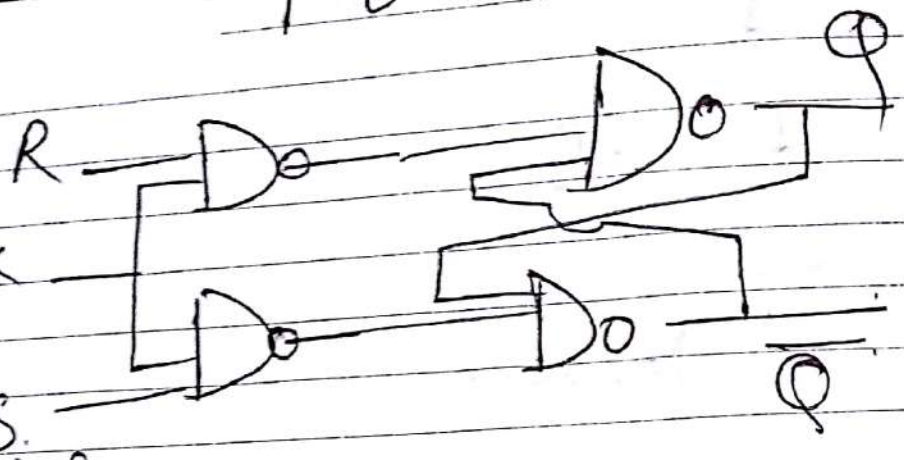
Flip flop



22/10/18

11

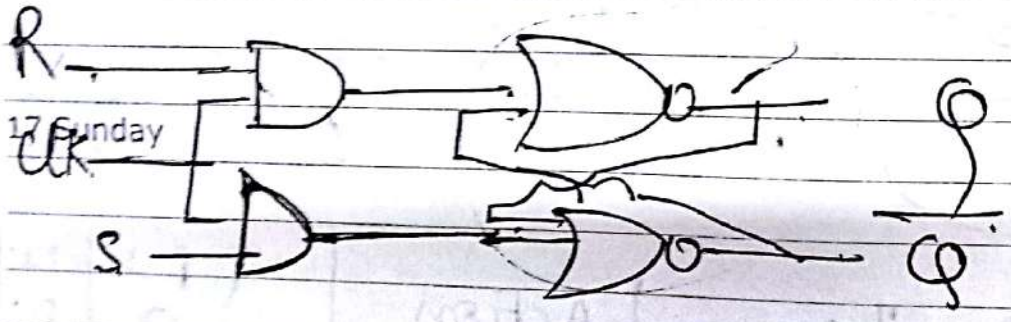
Flip-flop

(1) S-R flip flop

NOR Based

NOR		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

1
0



PS	NS
0	0
1	0
1	1
0	1

CLK	S	R	Q_n	Q_{n+1}	
0	x	x	Q_n	Q_n	No change
1	0	0	Q_n	Q_n	No Change
1	0	1	X	0	Reset
1	1	0	X	1	Set
1	1	1			Prohibited / Invalid

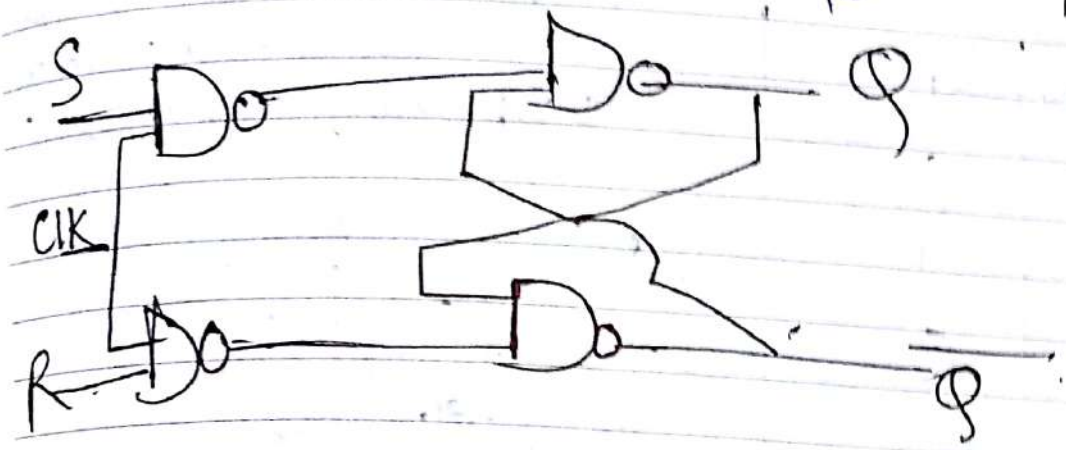
Scanned by CamScanner

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

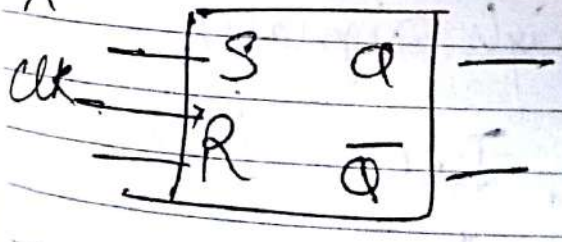
NAND Based

PS | NS



Clk	S	R	Q_n	Q_{n+1}	
0	X	X	Q_n	Q_n	No Chen
1	0	0	Q_n	Q_n	No Change
1	0	1	X	0	Reset
1	1	0	X	1	Set
1	1	1			Prohibitan

*



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Characteristic Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Invalid
1	1	1	

Excitation Table

(It tell what input should be taken so that particular ~~Qn~~ change can occur)

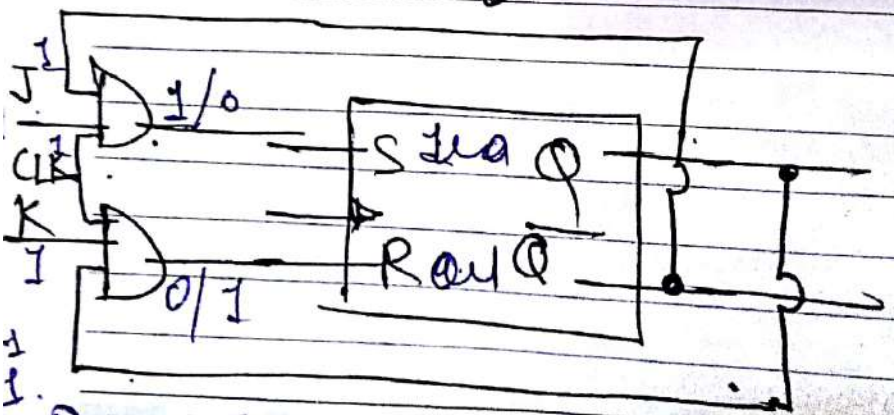
	$\bar{R}\bar{Q}$	$\bar{R}Q$	RQ	$R\bar{Q}$
$\bar{S}$	0 (0)	1 (1)	0 (3)	0 (2)
S	1 (4)	1 (5)	X (7)	X (6)

$$Q_{n+1} = S + \bar{R}Q$$

Excitation Table

Ps	Ns	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

* J-K flip-flop (Active high signals)



Jack / Kilbi

0	1
1	0
1	0
0	1

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* Forbidden State is removed by the JK flip-flop.

CLK	J	K	Q_n	Q_{n+1}	
0	X	X	Q_n	Q_{n+1}	No change
1	0	0	Q_n	Q_n	No Chan
1	0	1	X	0	Reset
1	1	0	X	1	Set
1	1	1	Q_n	$\overline{Q_n}$	Toggel cond^n

Excitation Table

Ps	NS	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

	$\overline{K}\overline{Q}$	$\overline{K}Q$	KQ	$K\overline{Q}$
$\overline{J}$	0	1	0	0
J	1	1	0	1

$Q_{n+1} = J\overline{Q} + \overline{K}Q$

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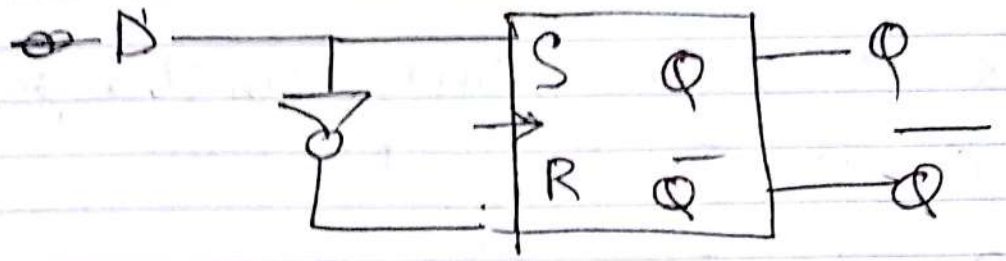
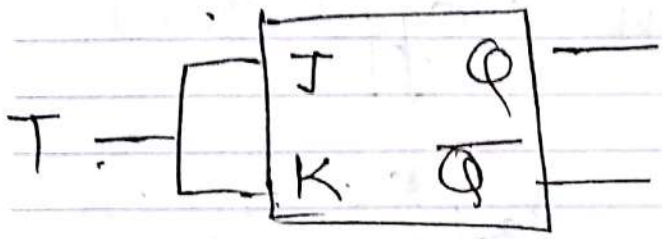
Delay flip-flop



Toggle flip flop



0 0
0 0 No change

1 1
1 1 Toggle

* Delay flip-flop

→ The Delay ff has only one input the Delay input and two Outputs Q & $\bar{Q}$

It can be constructed from SR flip-flop by inserting an inverter betn S & R and assigning the input as D as S

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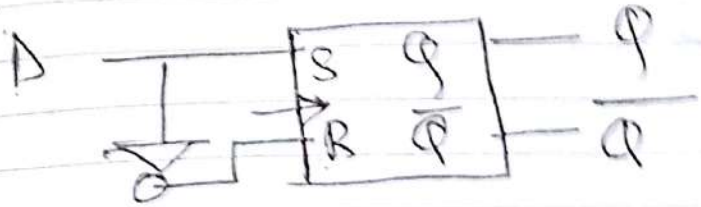
Latch :-

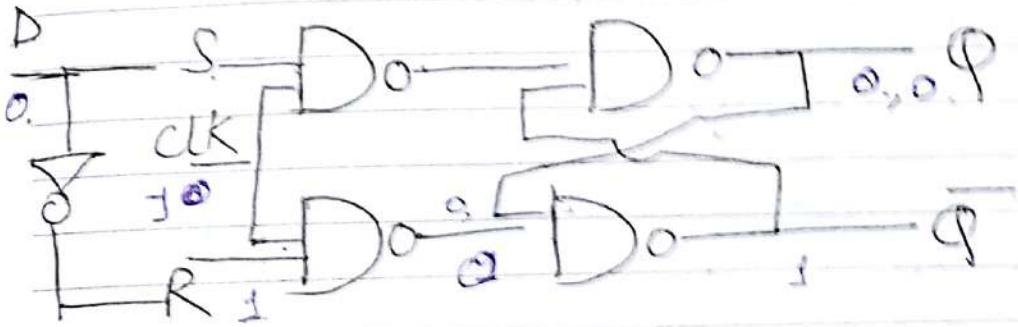
It is a storing unit.
It can store logical 1 & zero.

When we apply clk to latch it convert it into flip flop.

*



PS		NS
0	0	1
0	1	1
1	0	1
1	1	0



PS & NS Table

CLK	PS (Q_n)	Delay (D)	N.S (Q_{n+1})
0, 1	0	0	0
	0	1	1
	1	0	0
	1	1	1

Output follows the input only for the clock plus.

What input is taken so that we get the desired PS & NS.

June 2012

Saturday

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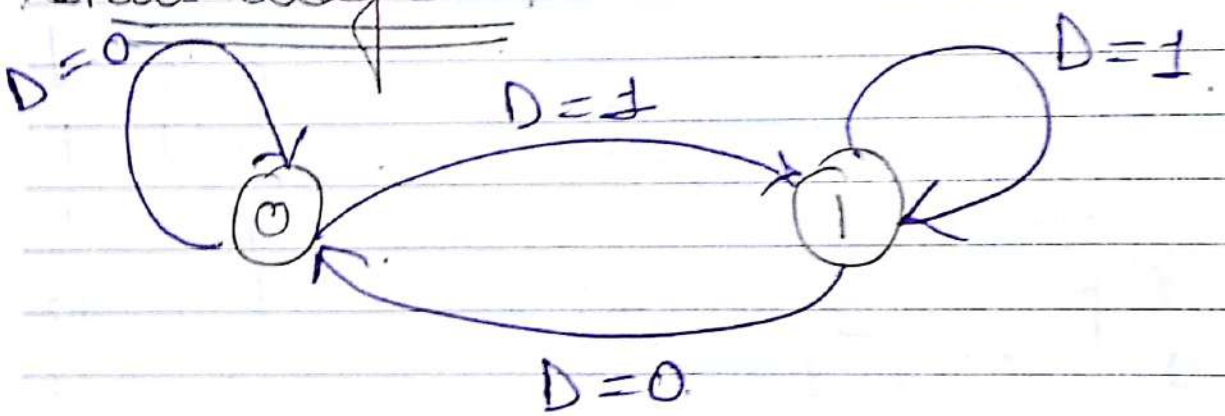
Excitation table for D flip flop

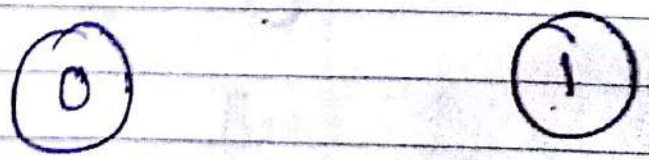
Q_n	Q_{n+1}	Excitation i/p
0	0	0
0	1	1
1	0	0
1	1	1

State diagram



State diagram of J-K flip flop

24 Sunday



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* Characteristic eqn for DFF.

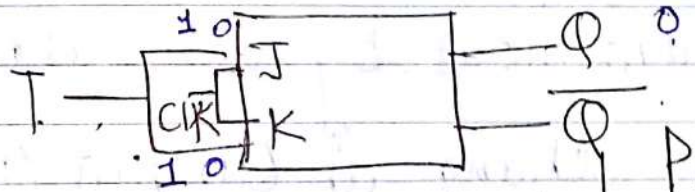
Q_n \ D	0	1
Q_n 0	0	1
Q_n 1	0	1

$\boxed{\text{Eqn} :- D}$

$\boxed{Q_{n+1} = D}$

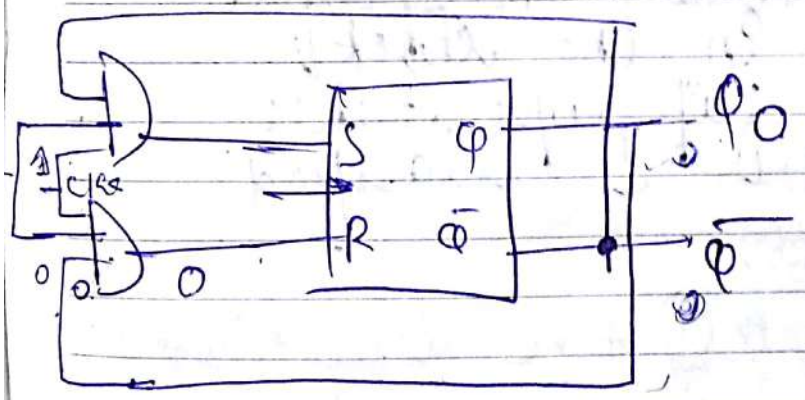
* Toggle flip flop

It has only one data input (T) & clk and two output Q & $\bar{Q}$. It can be obtained from JK flip flop by connecting its J & K inputs together.



PS NS Table

PS Q_n	i/p (T)	NS Q_{n+1}
0	0	No change 0
0	1	1
1	0	1
1	1	0



Excitation Table

Q_n	Q_{n+1}	Exc
0	0	0
1	0	1

The truth table shows that when T = 0 $Q_{n+1} = Q_n$. The next state is same as PS

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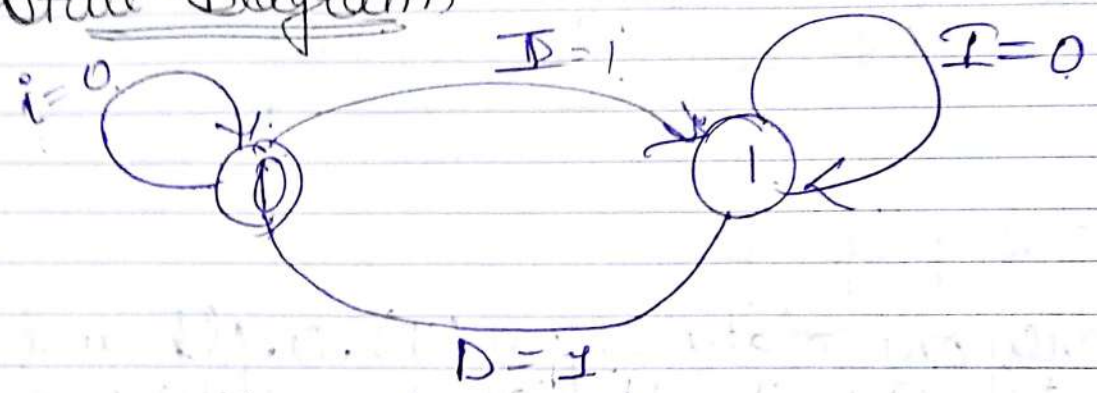
and no change occur.
When T = 1, $Q_{n+1} = \overline{Q_n}$ i.e
the state of flip flop is complement

State-Diagram



Triggering in flipflops

→ flipflops are synchronous by stable devices
→ Synchronous means change in Output occur at a specific point on a triggering input called clock based on specific internal or point in the clock at which triggering of flip flops takes place, It can be classified into types

→ level triggering → (1) +ve level trigged
→ edge triggering (2) −ve level triggered

(1) +ve edge triggered
−ve edge triggered

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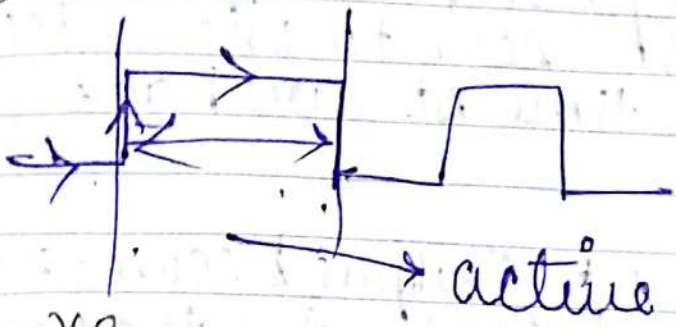
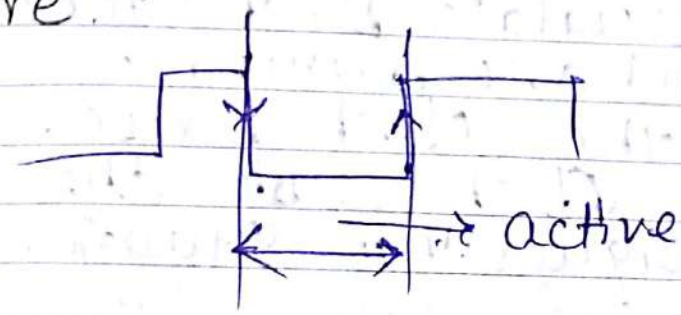
Level Trigger

① + ve



② -ve



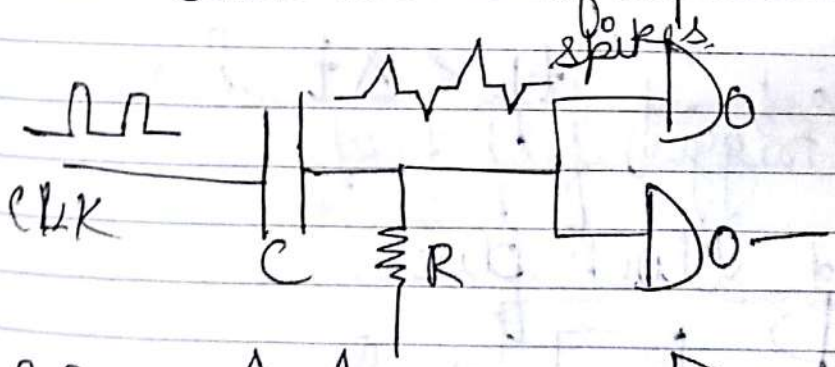
We can convert this by using inverter.

Edge Triggering

A level triggered flip flop can be converted to Edge triggered FF by inserting a differentiator circuit after the clock pulse.

↓

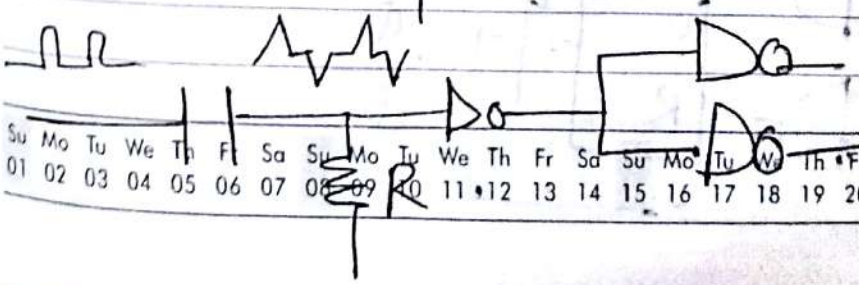
Combination of Capacitor & Resist.



Differentiator CKT

↓

Convert Square CLK to spikes



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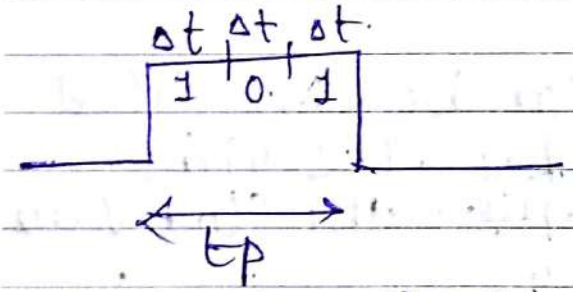
Forbidden problem of SR is rectified by JK.

Race around condition (Problem of JK)

When J=K=1 and q=0, when a clock pluse of width tp is applied, output will change from zero to one after a time Δt, Now after time Δt we have J=K=1 and Q=1.

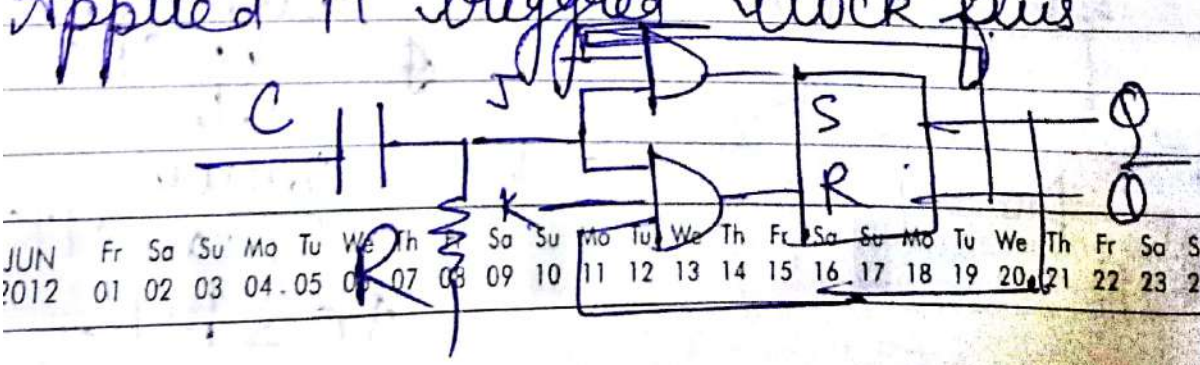
After another interval Δt Output become zero. Output will Osscialate back & forour between zero and one during duration tp of the clock pluse. at the end of the clock pluse the output is ambigues this situation is called Race around condition.



J=K=1, Q=0
1.

It can be avoided if tp < Δt here comes use of H trigger flip flop.

Applied H triggered clock plus



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Master Slave J-K flipflop

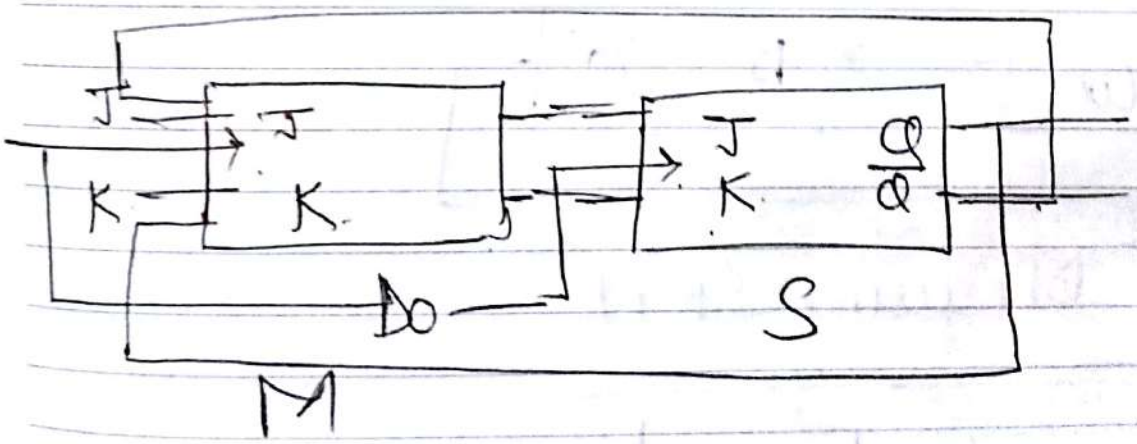
Master Slave JK flipflop
Can be Constructed using 2 JK flipflop

(1) Function as the master
(2) Function as the Slave

- First driven by the +ve edge of the CLK
- Second driven by the -ve edge.

→ When the clock plus has +ve edge the master ~~edge~~ acts as JK Input Slave doesnot respond.

→ At -ve edge Slave copies the master



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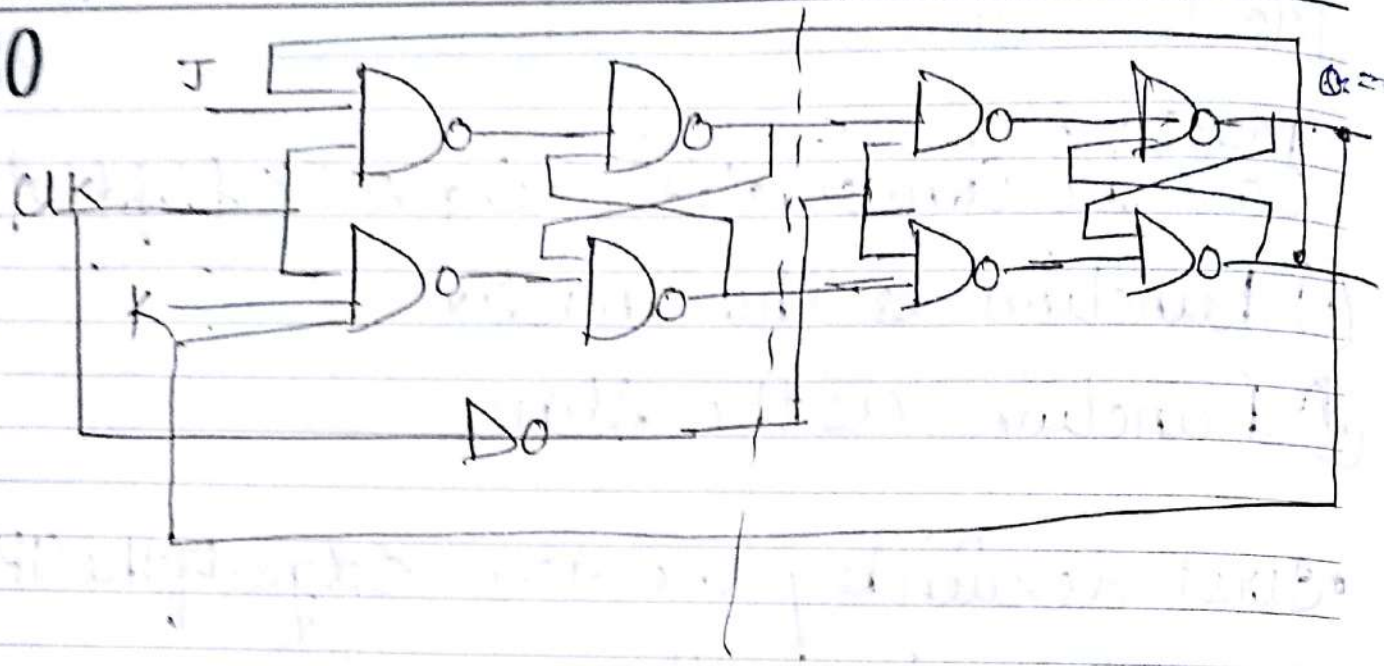
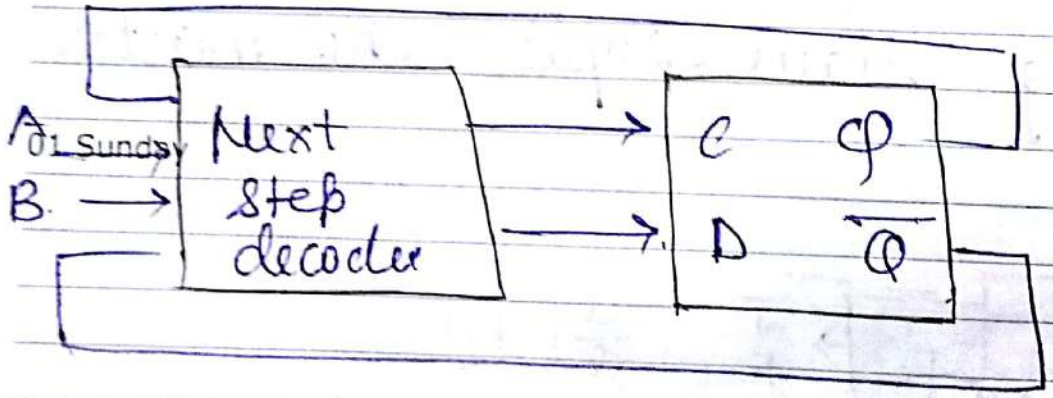
Master | Slave

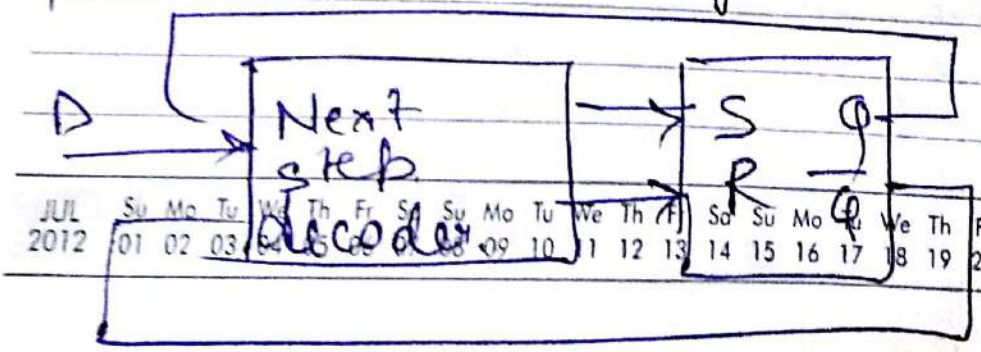


1 Realization of One flip flop using another FF

Block dia to realize FF (x) using FF (Y)



Q.1. Realize DFF using SRFF



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(1) Draw the ~~f~~ present state next state table of the flip flop to be design

(I)

PS	NS D	N.S
0	0	0
0	1	1
1	0	0
1	1	1

(2) Next we form an excitation for D flip flop using SR flip flop.

Q_n	D	Q_{n+1}	Excitation i/p S	R
0	0	0	0	X
0	1	1	1	0
1	0	0	0	1
1	1	1	X	0

(3) Design Next step decoder i.e simified expression for SR from excitation map.

Q_n \ D	D	D
Q_n	0 (0)	1 (1)
Q_n	0 (2)	X (3)

S

Q_n \ D	D	D
Q_n	X (0)	0 (1)
Q_n	1 (2)	0 (3)

R

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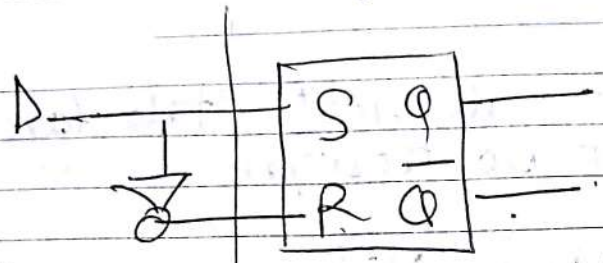
(4) Circuit for Delay flip flop using SR flip flop can be design.



Next State Decoder

Q Realize JKFF using SRFF

Ans (1) Draw the present & next state tabel of the FF to be design

(2)

PS	NS	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(3)

Q_n \ JK	$\bar{J}\bar{K}$	$\bar{J}K$	$J\bar{K}$	JK
$\bar{Q}_n$	0 (0)	0 (1)	1 (3)	1 (2)
Q_n	0 (4)	0 (5)	X (7)	X (6)

$$S = J\bar{Q}_n$$

Q_n \ JK	$\bar{J}\bar{K}$	$\bar{J}K$	JK	$J\bar{K}$
$\bar{Q}_n$	X (0)	X (1)	0 (3)	0 (2)
Q_n	1 (4)	1 (5)	0 (7)	0 (6)

$$R = J Q_n$$

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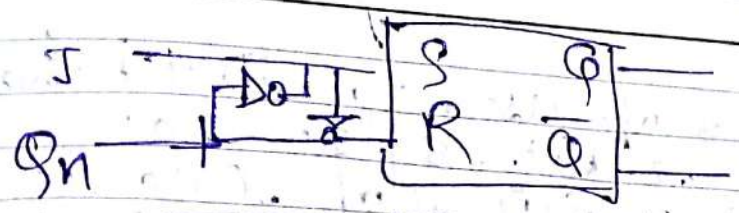

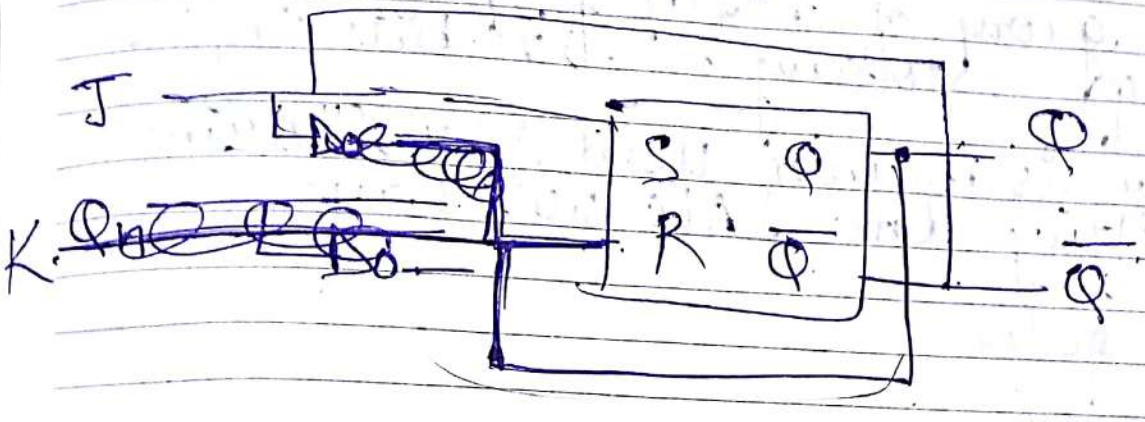

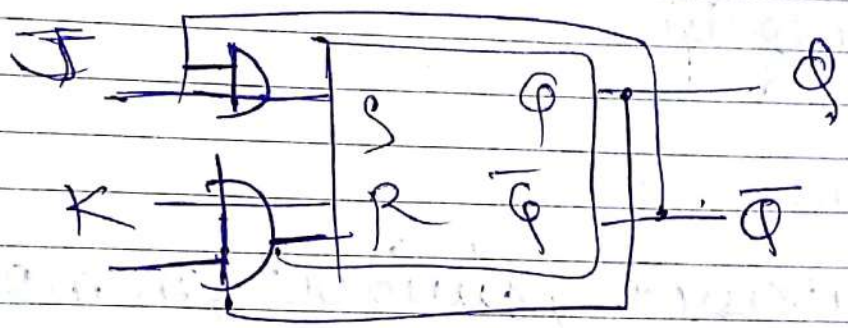

S	R
0	X
0	X
1	0
1	0
0	1
0	1
X	0
X	0

Qn	J	K	Qn+1
0	1	1	0

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Registers

* Group of flipflop used to store binary infⁿ. and n bit register has a group of n flip flop and is capable of storing n bits infⁿ.

The Register is mainly used for storing and shifting data A/c we have

1. Memory Register
2. Shift Register

Applications

1. Microprocessor, dividers, memories

Shift Registers

Shift Registers are classified into 4 type based on how binary infⁿ is entered or shifted out. A/c we have.

1. Serial In Serial Out SISO
2. Serial In parallel Out SIPO
3. parallel In serial Out PISO
4. parallel In parallel Out PIPO.

1. Serial in Serial Out :- It accept data serially i.e one bit at a time on a single input line. It produces the stored infⁿ on its

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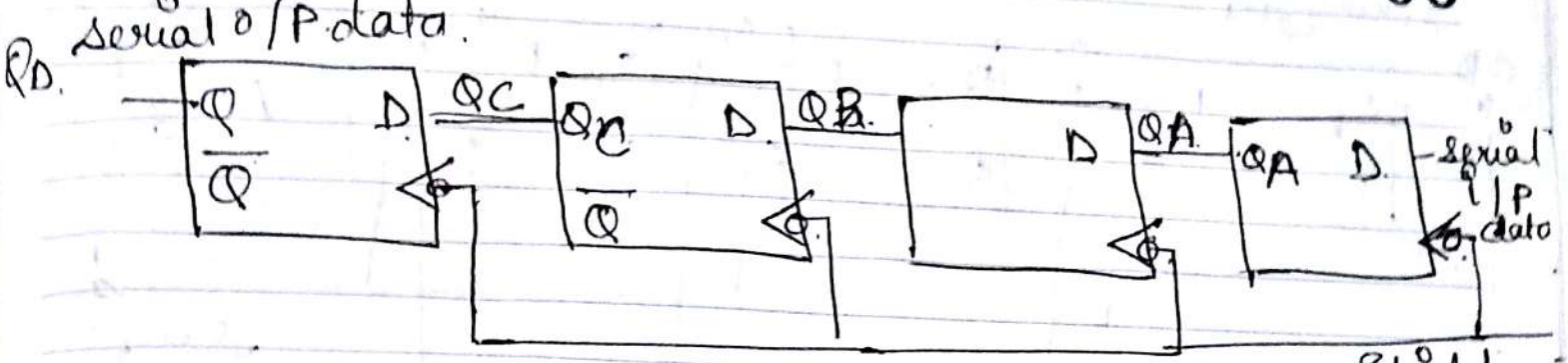
single output line in serial form.

(1) Shift left Reg:



Shift pulse	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1
0	1	1	1	0
1	1	1	0	0

→ 0 0 1 0

1 0 1 1 0

② Serial in parallel out

(i) Shift Reg: Data is shifted in serially but shifted out parallely. One the data is stored each bit appear on its respective output line and all of the bits are available simultaneously.

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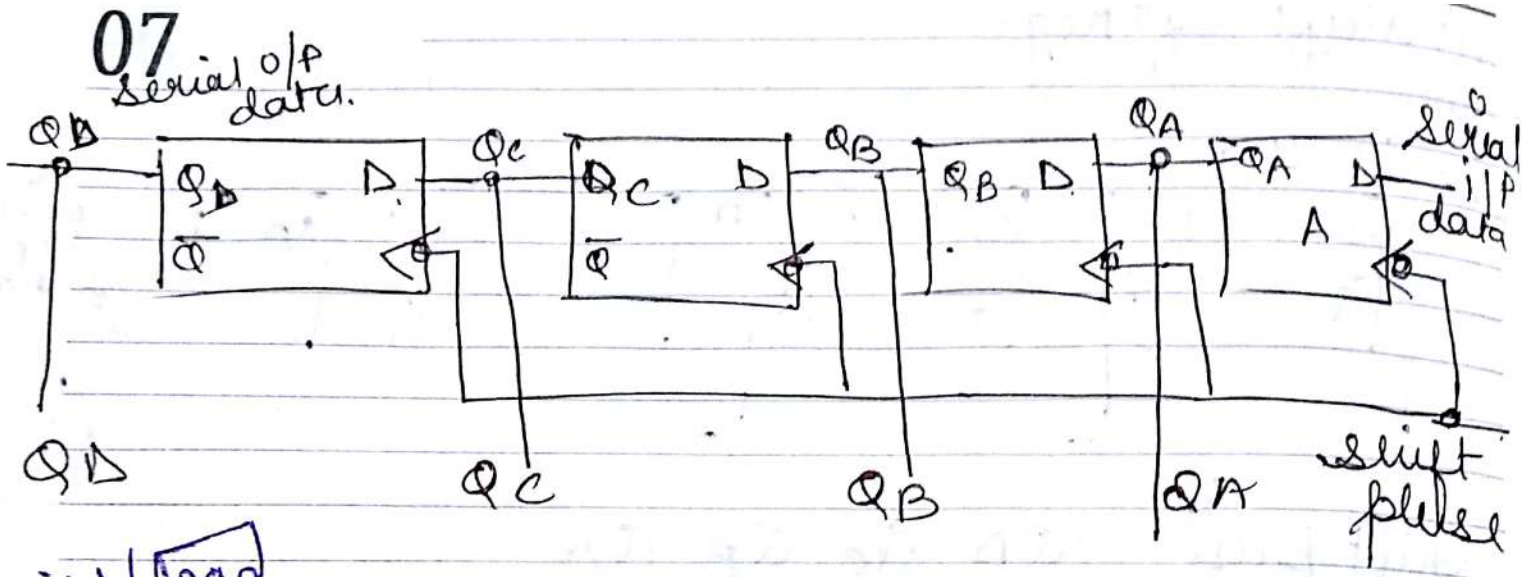
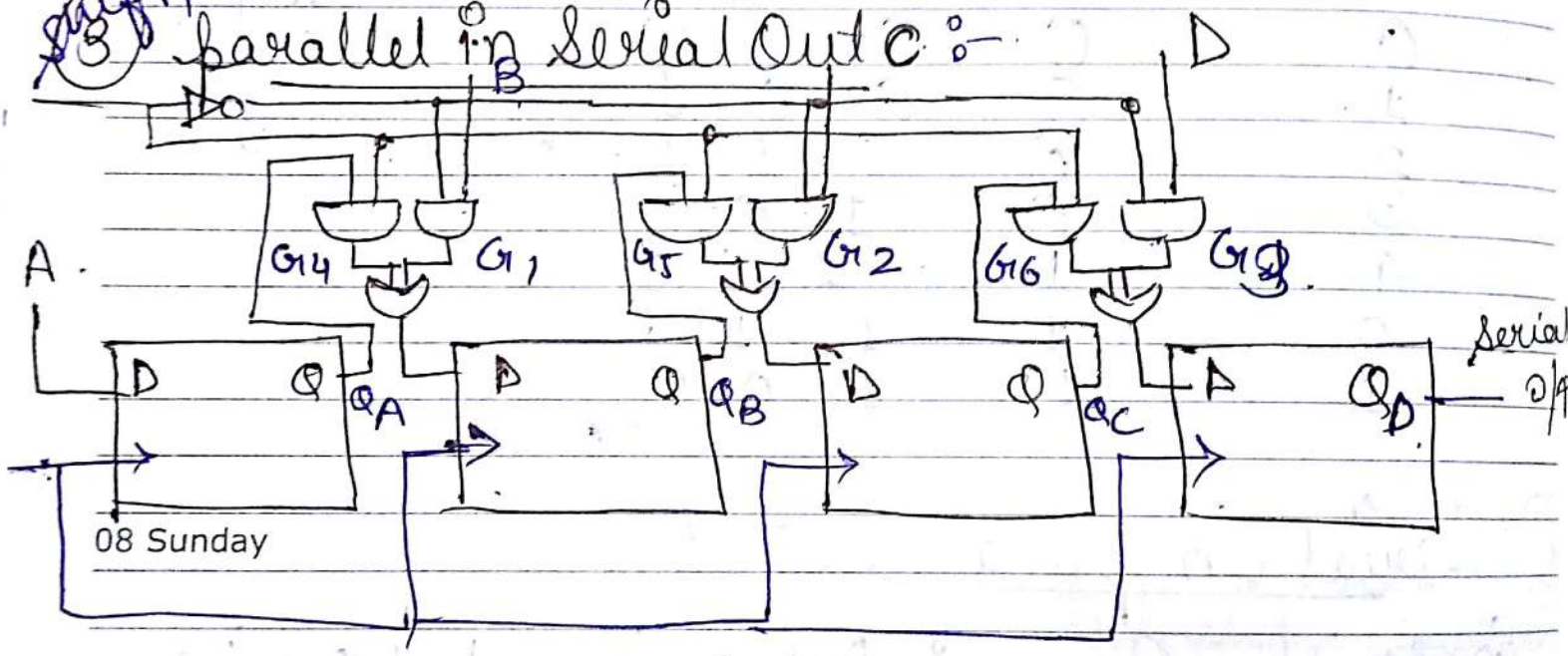


shift/load.

(3) parallel in Serial Out :-



08 Sunday

G1 G2 G3 → Parallel data in.

A, B, C, D are data input. Shift/load is control input that allows the 4 bits of data A, B, C, D to enter into the Registers in parallel or shift data in serial.

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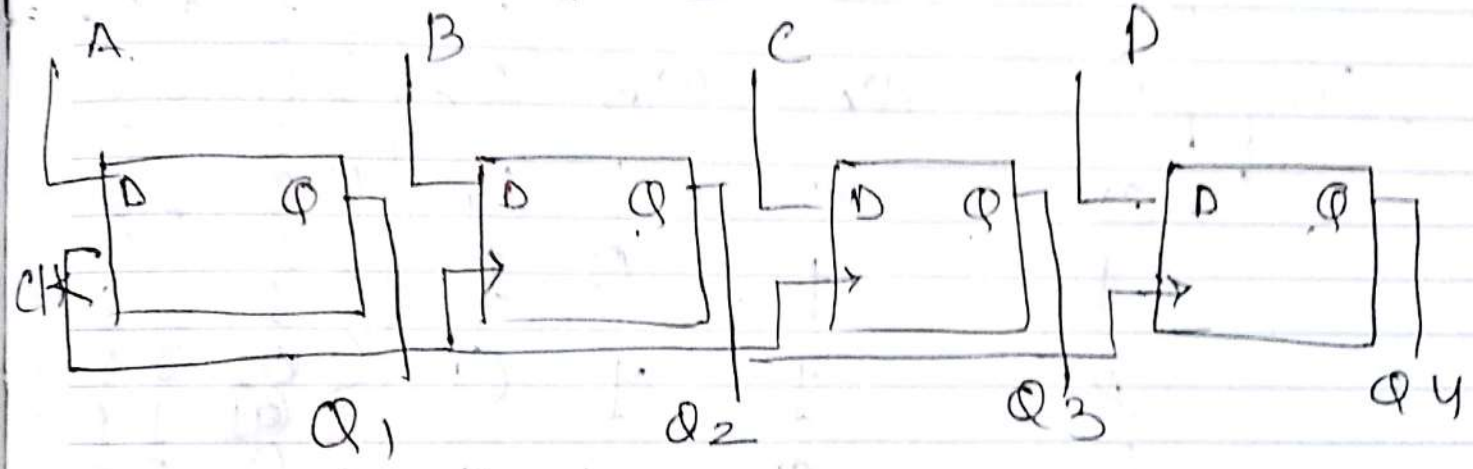
when Shift / Load is low, And gates G1, G2 & G3 are enabled and data is entered to B, C, D i/p. A is connected directly.

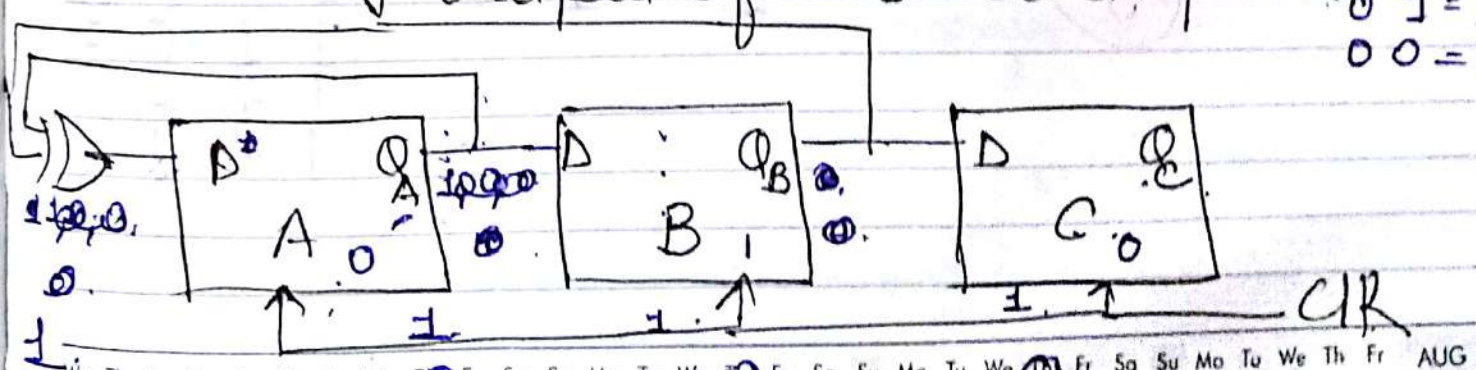
When the control is high, And gates G4, G5 & G6 are enabled allowing the data bits to shift right one stage to next.

(4) Parallel in parallel Out



Q. Intialy A, B, C = 0 1 0. What will be the Output after 5 clock pluse

0 1 = 1
0 0 = 0



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Shift pulse	QA	QB	QC
0	0	1	0
1	1	0	1
2	0	1	1
3	1	0	1
4	1	1	0
5	0	1	1

Shift pulse	QA	QB	QC
0	0	1	0
1	1	0	1
2	1	1	0
3	0	1	1
4	1	0	1
5	1	1	0

QD	QC	QB	QA	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

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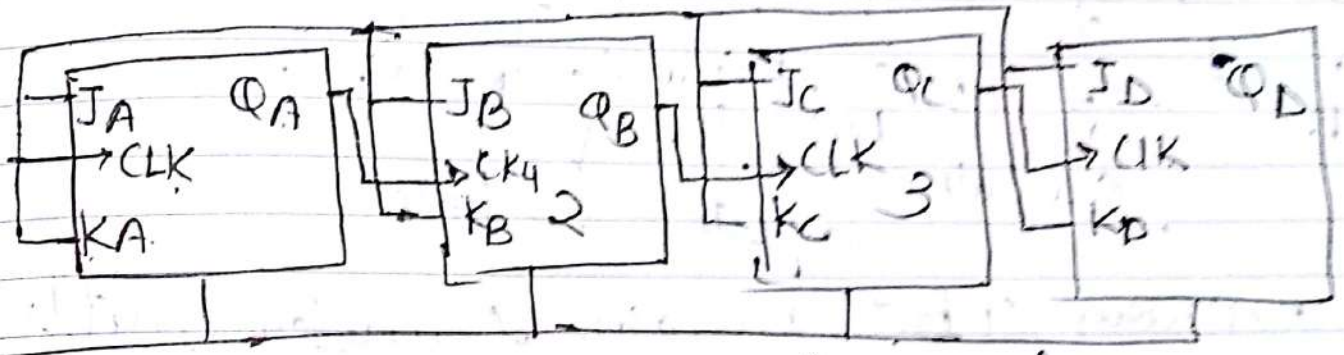
Counters :-

1. Asynchronous & Synchronous
2. Single mode & multimode
3. Modulus
4. 4 bit single mode upcounter
   4 bit serial upcounter
   4 bit asynchronous counter
   4 bit ripple counter

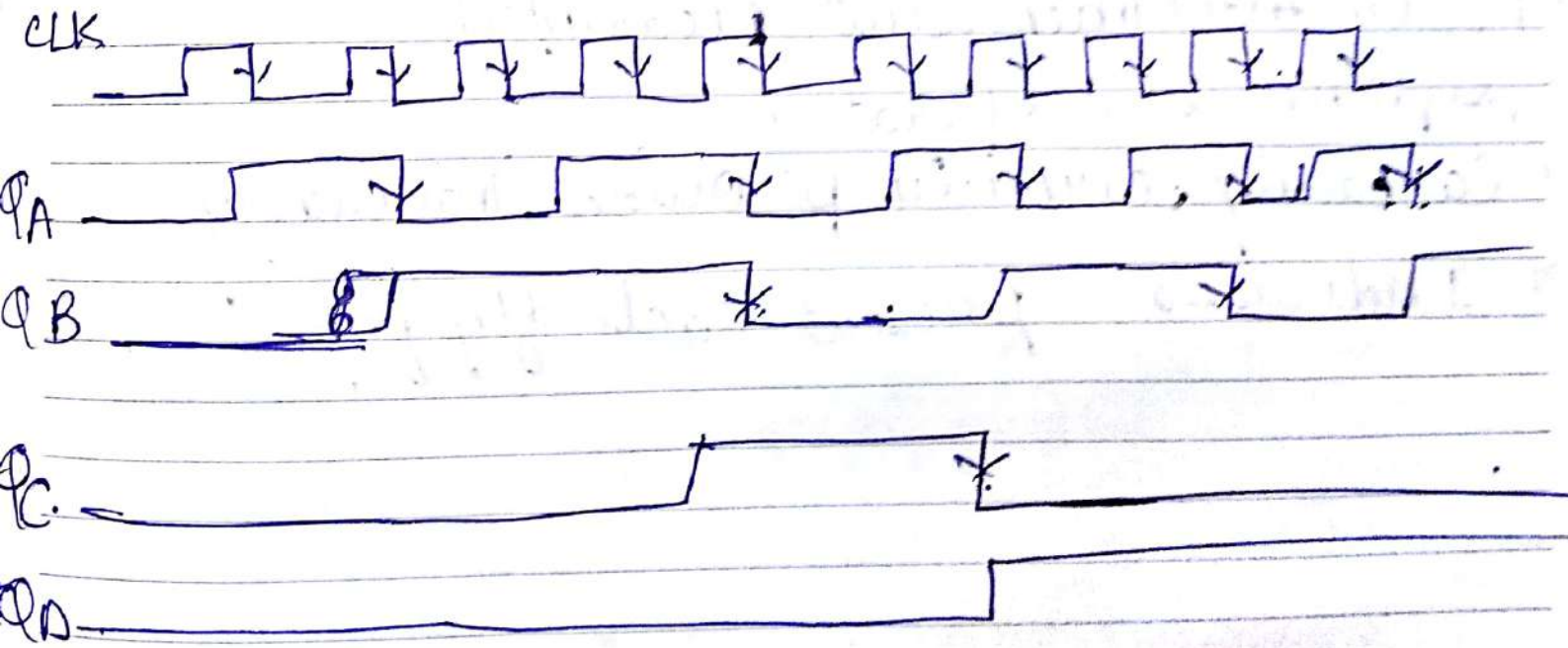
   } all are same.



$$2^n - 1 = 2^4 - 1 = 15 \text{ (states)}$$

0000 to 1111.

Q_D	Q_C	Q_B	Q_A
0	0	0	0



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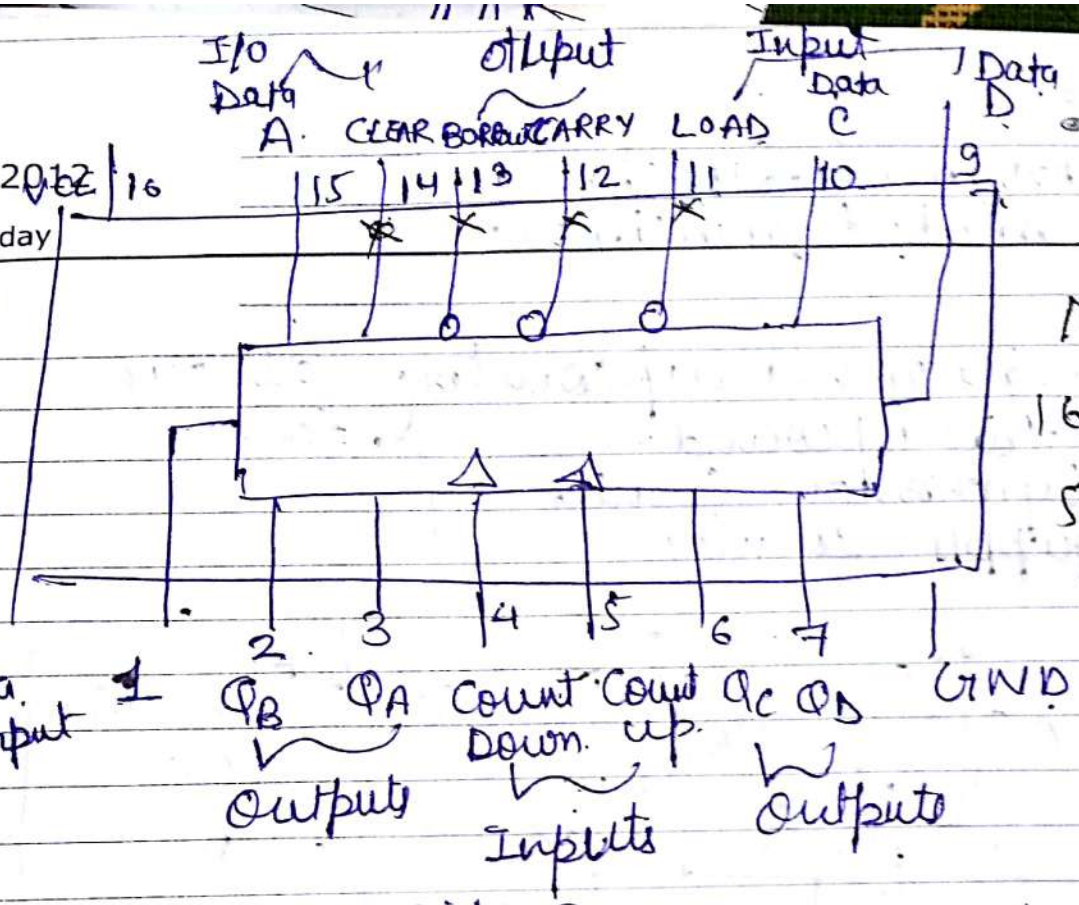

14+8 = G
16 = VCC
5 = U
4 = D

Synchronous 4 Bit Binary Counter with Dual Clock

Features :-

→ Fully ~~Inter~~ independent clear input
→ Synchronous operation
→ Cascading circuity provided internally
→ Individual present each flip flop.

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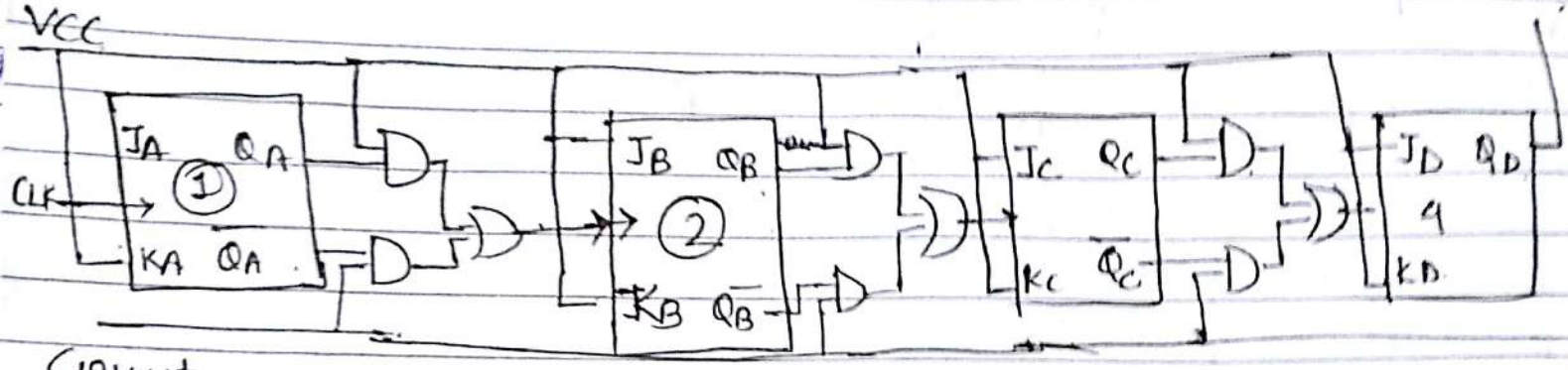
(Ripple Counter)

4 bit asynchronous up/down counter →

Counter

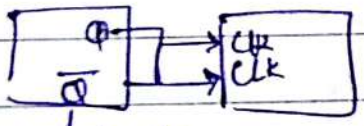


Count down

When counter down = 1
Counter up = 0

(down counter ki tarah work karega)
(dependent on complemented output i.e $\overline{Q_A}$)

→ Used to count the clock pluse
→ progation delay of each flipflop × total no of ff
$n \times t_p$
→ Drawback :- It take much time.
→ Upcounter



↳ downcount

Modulus → Stages

MOD-4 → 2 ff (2^n)

00	4 stage
01	
10	
11	

n is no of ff

Mod-6 → 3 ff

Mode-10 → 4 ff

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Design Mod-6 Rajesh asynchronous

* Design MOD-3 Synchronous counter

$a \rightarrow b \rightarrow c \rightarrow a$

Write the PS-NS Table $00 \rightarrow 01 \rightarrow 10 \rightarrow 00$

P.S	N.S
q_1 q_0	Q_1 Q_0
0 0	0 1
0 1	1 0
1 0	0 0
1 1	d d.

Excitation table for Mod-3 Counter

PS	NS	Excitation	t/PS
q_1 q_0	Q_1 Q_0	J_1 K_1	J_0 K_0
0 0	0 1	0 X	1 X
0 1	1 0	1 X	X 1
1 0	0 0	X 1	0 X
1 1	d d	d d	d d.

Exciation Map for K_1, J_0 K_0, J_1 of the Counter are drawn

$q_1 \backslash q_0$	$\bar{q}_0$	q_0
$\bar{q}_1$	0	1
q	X	X

$\boxed{J_1 = q_0}$

$q_1 \backslash q_0$	$\bar{q}_0$	q_0
$\bar{q}_1$	X	X
q_1	1	X

$\boxed{K_1 = 1.}$

$q_1 \backslash q_0$	$\bar{q}_0$	q_0
$\bar{q}_1$	1	X
q_1	0	X

$\boxed{J_0 = \bar{q}_1}$

$q_1 \backslash q_0$	$\bar{q}_0$	q_0
$\bar{q}_1$	X	1
q_1	X	X

$\boxed{K_0 = 1}$

*

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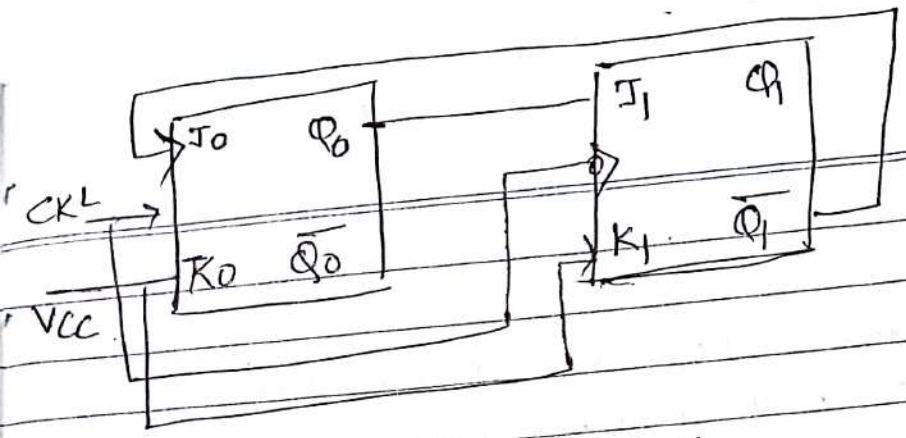

MOD-6 Synchronous Counter

P.S q_2	q_1	q_0	N.S Q_2	Q_1	Q_0		J_2	K_2	J_1	K_1	J_0	K_0
0 - 0	0	0	0	0	1	— 1						
1 - 0	0	1	0	1	0	— 2						
2 - 0	1	0	0	1	1	— 3						
3 - 0	1	1	1	0	0	— 4						
4 - 1	0	0	1	0	1	— 5						
5 - 1	0	1	1	1	0	— 6						
6 - 1	1	0	1	1	1	— 7						
7 - 1	1	1	0	0	0	— 8						

Excitation Input

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Johnson

This is similar to standard standard ring Counter but the inverted Output became as input for the signal

unit :- 4

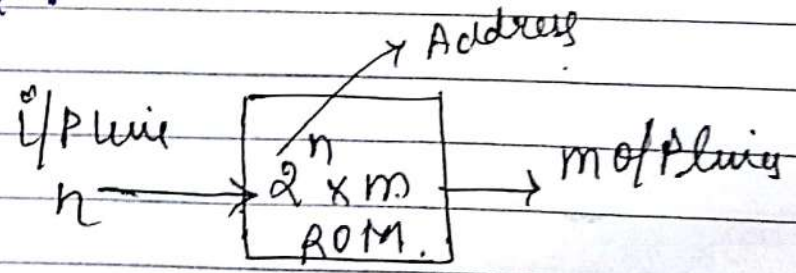
① RAM ② ROM ③ PND

PND

ROM (Read only memory)

→ Types of Rom.

→ A Rom is a memory device in which a fixed set of binary information is stored. It is device that include both decoders and OR gate within a single IC Package. Block Diag. shows that there are n input lines and m Output lines. Each with Combination of input variables is called an address. Each Bit Combination of Output line is called a word. The no. of bits per word is equal to the no. of Output lines m.
The no. of distinct address with n input variable is 2^n.



Consider a 32×8 block the unit Consists of 32 words of 8 bits. here there are 32 address line (2^5) and 5 input line. A ROM is specified by the total no. of bits it contents $= 2^n \times m$.

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Date : Page :

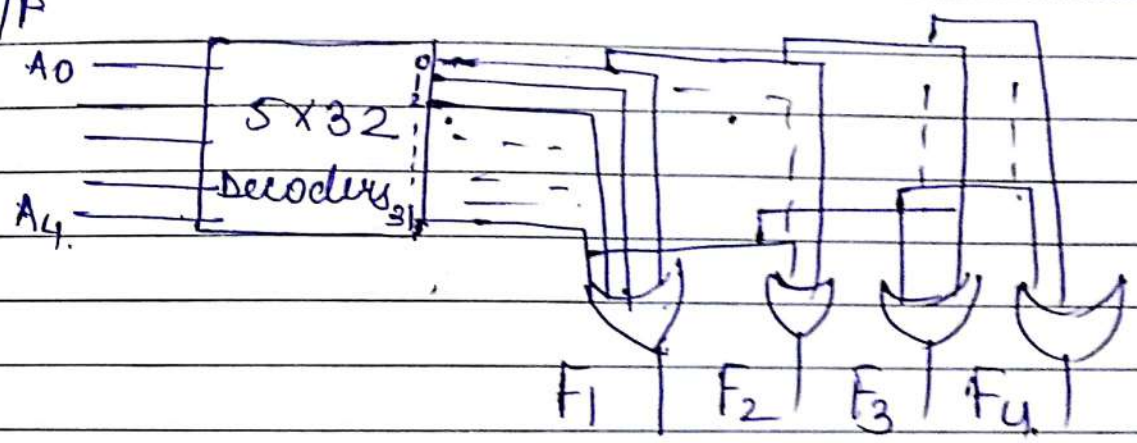
Ex:- 2048 bit ROM
is organised as $512 \times 4 = (2^9 \times 4)$ → Inputs

Address O/P.

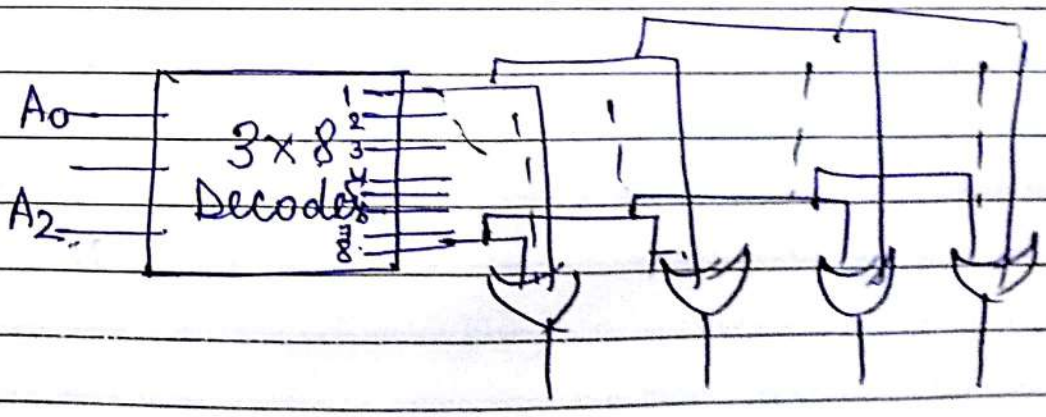
* logic or Internal Construction of 32x4 ROM

Given.. 32x4 $2^5 = 32$ → I/P.

Add. O/P



→ 32x8
→ 8x4 → O/P
2^3 I/P.



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