Explanation of ePWM1 Output Timing in Up-Down Counter Mode

Hotzenblitz Project – Motor Current Sensing

1 Overview

In this setup, the ePWM1 module of the TI C2000 F28003x microcontroller is configured in **up-down counting mode** to generate a 1 kHz timing signal. This signal is routed to GPIO0 and observed on an oscilloscope to visualize the exact timing of ADC sampling events.

A common point of confusion is why the observed pulse on the oscilloscope appears every 1 ms, even though the time-base period register (`TBPRD`) corresponds to 0.5 ms. This document explains this behavior clearly.

2 ePWM1 Time-Base Configuration

The relevant configuration parameters are:

- System clock: $f_{\text{SYSCLK}} = 120$ MHz
- Counting mode: Up-Down
- Time-base period register: `TBPRD = 60000`

In up-down mode, the counter behavior is:

$$0 \rightarrow \texttt{TBPRD} \rightarrow 0$$

This complete motion constitutes **one full PWM period**.

3 Time Calculation

Each time-base count corresponds to:

$$T_{\text{count}} = \frac{1}{120\,\text{MHz}} = 8.33 \text{ ns}$$

Up-count duration

$$60000 \times 8.33 \text{ ns} = 0.5 \text{ ms}$$

Full up-down period

$$2 \times 0.5 \text{ ms} = 1 \text{ ms}$$

Hence, the resulting PWM frequency is:

$$f_{\text{PWM}} = 1 \text{ kHz}$$

4 Meaning of TBPRD in Up-Down Mode

The counter reaches `TBPRD` exactly at the **midpoint** of the PWM period:

$$t = 0.5 \text{ ms}$$

Internally, this point corresponds to the **center-aligned position** of the PWM waveform. In this project, the ADC Start-of-Conversion (SOC) trigger is generated at this instant to achieve low-noise current sampling.

5 ePWM1 Output Pulse Generation

The Action Qualifier configuration is:

- Output set HIGH when counter equals CMPA during up-count
- Output set LOW when counter equals TBPRD

With:

$$\texttt{CMPA} = 59000$$

This produces a short pulse shortly before the counter reaches `TBPRD`. The falling edge of this pulse coincides exactly with the ADC trigger event at `TBCTR = TBPRD`.

6 Why the Oscilloscope Shows a 1 ms Interval

At system start:

- The time-base counter is reset to zero
- The PWM output starts in the LOW state
- No output transition occurs at time $t = 0$

An oscilloscope can only measure time between **observable signal edges**. Since the first visible transition occurs only when CMPA or TBPRD is reached, the oscilloscope measures the time between successive pulses.

Because the full up-down counting cycle takes 1 ms, the pulses repeat every 1 ms. Therefore, the oscilloscope displays a pulse spacing of 1 ms, even though each pulse internally corresponds to the midpoint (0.5 ms) of the PWM cycle.

7 Why the Oscilloscope Usually Shows "1 ms"

This behavior is a direct consequence of how oscilloscopes operate:

- Oscilloscopes measure **time between recurring signal edges**
- They do **not know the absolute start time** of the PWM counter

As a result, although the first PWM event occurs internally at 0.5 ms after startup, the oscilloscope primarily displays the interval between repeated pulses, which corresponds to the full PWM period of 1 ms.

8 Key Insight

> **TBPRD represents the midpoint of the PWM internally in up-down mode, but the oscilloscope displays the full PWM period because it measures the time between repeated output transitions, not absolute time from counter start.**

9 Conclusion

Although `TBPRD = 60000` is reached after 0.5 ms in up-down counting mode, the PWM output pulse appears every 1 ms on the oscilloscope. This is because the oscilloscope measures the interval between recurring output edges, which occur once per full PWM period. Internally, however, the ADC sampling remains perfectly synchronized to the center of the PWM cycle.