

## Design Specification

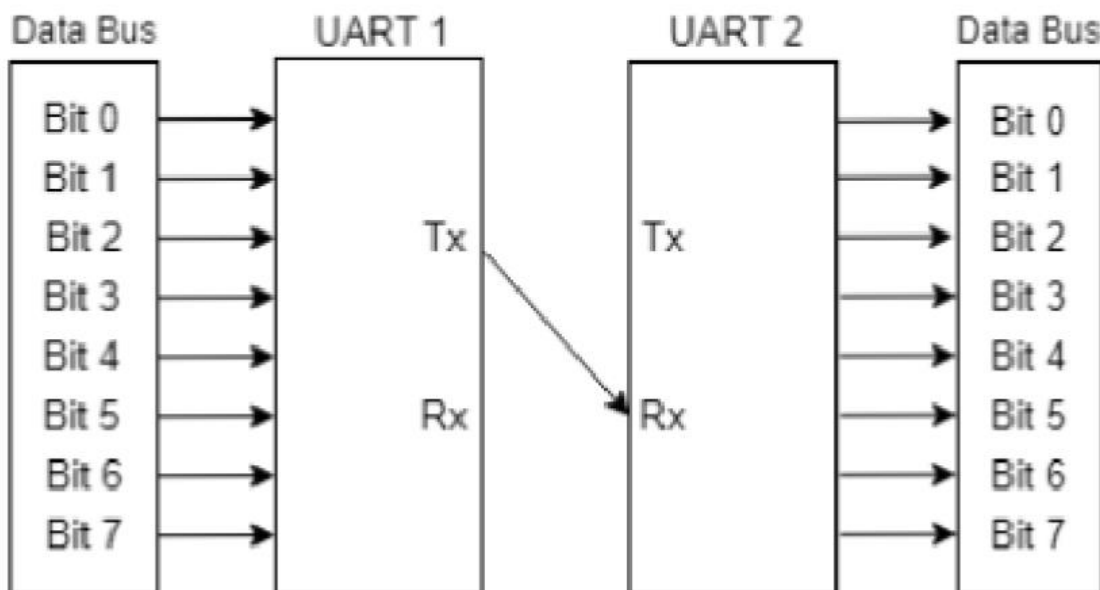
### Implementation and Verification of UART using Class and UVM based methodologies

#### 1.Features

UARTs (Universal Asynchronous Receiver/Transmitter facilitates serial communication between devices. Some features typically associated with UART design include:

1. Baud Rate Configuration: UART supports programmable baud rates, allowing communication at different speeds. Common baud rates include 1200,2400,4800,9600 and 115200 bps.
- 2.Enable signal: Enable signal will initiate the transmission.
- 3.Data Frame Configuration: UART supports configurable data frame formats, including the number of data bits per frame say 8 bits.
4. Dual UART Communication: The UART module supports bidirectional serial communication between two UART devices. This feature enables seamless data exchange between two independent systems or devices equipped with UART interfaces. Each UART can transmit and receive data, allowing for full-duplex communication between the connected devices.

#### 2.Implementation



### **3.Functional Description**

The UART that is going to transmit data receives the data from a data bus. The data bus is used to send data to the UART by another device like a CPU, memory, or microcontroller. Data is transferred from the data bus to the transmitting UART in parallel form. After the transmitting UART gets the parallel data from the data bus, it adds a start bit, a parity bit, and a stop bit, creating the data packet. Next, the data packet is output serially, bit by bit at the Tx pin. The receiving UART reads the data packet bit by bit at its Rx pin. The receiving UART then converts the data back into parallel form and removes the start bit, parity bit, and stop bits. Finally, the receiving UART transfers the data packet in parallel to the data bus on the receiving end.

### **4.Baud Rate Calculation**

$\text{clock\_count} = \text{clock\_frequency} / \text{baud rate}$

clock\_count is an internal variable declared and the ratio is assigned to it.

For Baud Rate=1200,

$1\text{MHz} / 1200 = 833.33$

For Baud Rate=2400,

$1\text{MHz} / 2400 = 416.66$

For Baud Rate=4800,

$1\text{MHz} / 4800 = 208.33$

For Baud Rate=9600,

$1\text{MHz} / 9600 = 104.16$

For Baud Rate=115200,

$1\text{MHz} / 115200 = 8.68$

### **5.Specifications**

**Module uarttx:**

- *clk\_tx*: transmitter clock in the uart with 50Mhz frequency.
- *rst* : reset signal.
- *tx\_data*: input data consists of 8 bits of data lines ,1 bit of start signal,1 bit of stop.
- *en\_tx*: when enabled, transmission of data to transmitter, 1 bit signal.
- *tx*: output data to be transmitted by the transmitter, it consists of input data streamed and it also consists of 8 bits of input data.
- *donetx*: flag to confirm the data is transmitted by the transmitter. Its one-bit signal.
- *newd* : Signal indicating the input of data

### Module uartrx:

- *clk\_rx*: receiver clock in the uart with 50Mhz frequency
- *rst* : reset signal.
- *rx\_data*: output data from receiver consists of 8 bits of data lines,1 bit of start signal, 1 bit of stop.
- *en\_rx*: enable receiving of data to receiver 1,1-bit signal.
- *rx*: input data to receiver from the transmitter, it consists of output data streamed and it also consists of 8 bits of output data.
- *donerx*: flag to confirm the data is received completely. It's a one-bit signal.

### Module uart\_single:

- Uart\_single consists of both transmitter and receiver.
- *clk* : Clock signal
- *rst* : Reset signal
- *dintx* : input, 8 bits data
- *newd* : Signal indicating the input of data
- *en\_tx*: when enabled, transmission of data to transmitter, 1 bit signal.
- *en\_rx*: enable receiving of data to receiver,1-bit signal.
- *tx*: output data to be transmitted by the transmitter, it consists of input data streamed and it also consists of 8 bits of input data.
- *doutrx* : output, 8 bits of data
- *donetx*: flag to confirm the data is transmitted by the transmitter. Its one-bit signal.
- *donerx*: flag to confirm the data is received completely. It's one-bit signal.

### Module uart\_top:

- *clk* : Clock signal
- *rst* : Reset signal
- *din* : input, 8 bits data
- *newd* : Signal indicating the input of data.
- *en\_tx1*: when enabled, transmission of data to transmitter 1, 1 bit signal.
- *en\_tx2*: when enabled, transmission of data to transmitter 2, 1 bit signal.
- *en\_rx1*: enable receiving of data to receiver 1,1-bit signal.
- *en\_rx2*: enable receiving of data to receiver 2,1-bit signal.
- *donetx1*: flag to confirm the data is transmitted by the transmitter 1. Its one-bit signal.
- *donerx1*: flag to confirm the data is received completely by the receiver. It's one-bit signal.
- *donetx2*: flag to confirm the data is transmitted by the transmitter 2. Its one-bit signal.
- *donerx2*: flag to confirm the data is received completely by the receiver 2. It's one-bit signal.

- *dout*: output, of 8 bits data.
- *tx1rx2*: Data transfer from transmitter 1 to Receiver 2.
- *tx2rx1*: Data transfer from transmitter 1 to Receiver 2.

## **6.References**

<https://www.theengineeringknowledge.com/introduction-to-uart/>

<https://www.ijeat.org/wp-content/uploads/papers/v9i5/E1135069520.pdf>

<https://scholarworks.calstate.edu/downloads/vq27zr66z>

[https://www.ti.com/lit/ug/sprugp1/sprugp1.pdf?ts=1713787655012&ref\\_url=https%253A%252F%252Fwww.google.com%252F](https://www.ti.com/lit/ug/sprugp1/sprugp1.pdf?ts=1713787655012&ref_url=https%253A%252F%252Fwww.google.com%252F)