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Semester Project – Bandgap Reference Voltage

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Sommaire

Abstract **ii**

1 Principle & Specifications **1**

2 Generate a CTAT Voltage **3**
2.1 Evolution of V_{BE} with respect to temperature 3
2.2 Bipolar Implementation in CMOS process 4

3 Generate a PTAT Voltage **5**
3.1 Using Base-emitter Voltage 5
3.2 Using Gate-source Voltage 6

4 Bandgap Voltage **8**
4.1 Current Source - Beta-Multiplier 8
4.2 Single Stage OTA 10
4.3 Overall circuits 11
4.3.1 Bandgap Voltage Reference 11
4.3.2 Sub-1V Bandgap Current and Voltage Reference 12

5 Results after Simulation **14**
5.1 Dependence to VDD 14
5.2 Temperature Dependence 14
5.3 Simulation Post route 14

Conclusion **15**

Annexes **16**

A Evolution of V_{BE} with respect to temperature **17**

B Output resistance of Beta Multiplier Current Source **18**

C ANNEXE C **19**

Abstract

ABSTRACT

Table des figures

1.1 CTAT Voltage Evolution 1
1.2 PTAT Voltage Evolution 1
1.3 General Bandgap Voltage Principle 2
2.1 Base-emitter Voltage Context 3
2.2 Layout of PNP Bipolar Transitor 4
3.1 Generate a PTAT Voltage 5
3.2 Generate a PTAT Current 6
3.3 Generate a PTAT Current with MOS transistor 7
4.1 Beta-Multiplier Current Source with Cascode 8
4.2 Beta-Multiplier Current Source with Cascode 9
4.3 OTA with PMOS differential pair 10
4.4 Bandgap Voltage Reference 11
4.5 Bandgap Voltage and Current Reference 12
B.1 Small Signal Analysis 18

Liste des tableaux

1.1 Voltage Reference Specifications 2
4.1 Beta-Multiplier transitor dimension 9
4.2 OTA transitor dimension 11
4.3 Bandgap Voltage Reference Dimensions 12

1 Principle & Specifications

Voltage references have always been an essential component of any system and consequently an important topic to explore. The last decades thrust toward higher and even total system integration has required all designers to be knowledgeable of this particular topic due to its mixed-signal implications (output impedance, temperature coefficient, etc...)

A general-use (ideal) voltage reference is a circuit used to generate a fixed voltage, V_{ref}, that is independent of the power supply voltage VDD (where $V_{ref} < VDD$), temperature, and process variations. In other words, the ideal reference voltage is independent of PVT. In some cases, we want to design a reference that varies with temperature. For example, if V_{ref} increases with temperature, Fig. 1.2, we say that the reference voltage is proportional to absolute temperature or **PTAT**. If the reference voltage decreases with increasing temperature, Fig. 1.1, the reference is said to be complementary to absolute temperature or **CTAT**.

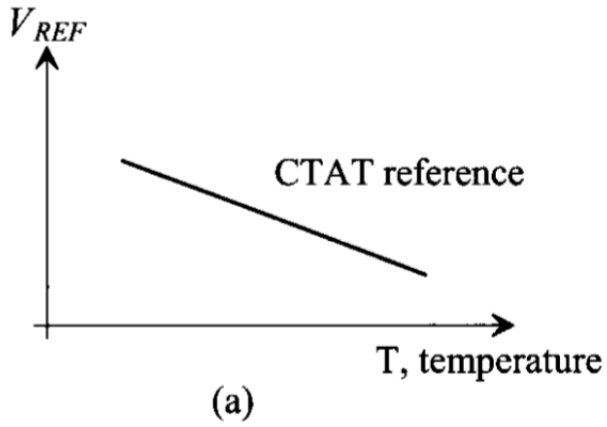

FIGURE 1.1 – CTAT Voltage Evolution

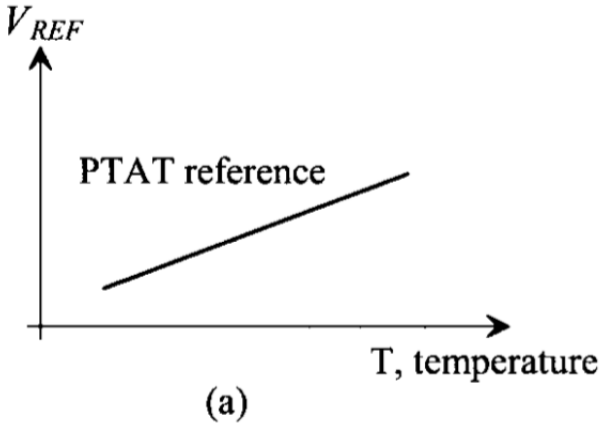

FIGURE 1.2 – PTAT Voltage Evolution

The **PTAT** and **CTAT** references can be used to design a voltage reference that changes very little with temperature called a bandgap reference. We only need to sum the two voltages with the correct coefficient K (Fig. 1.3).

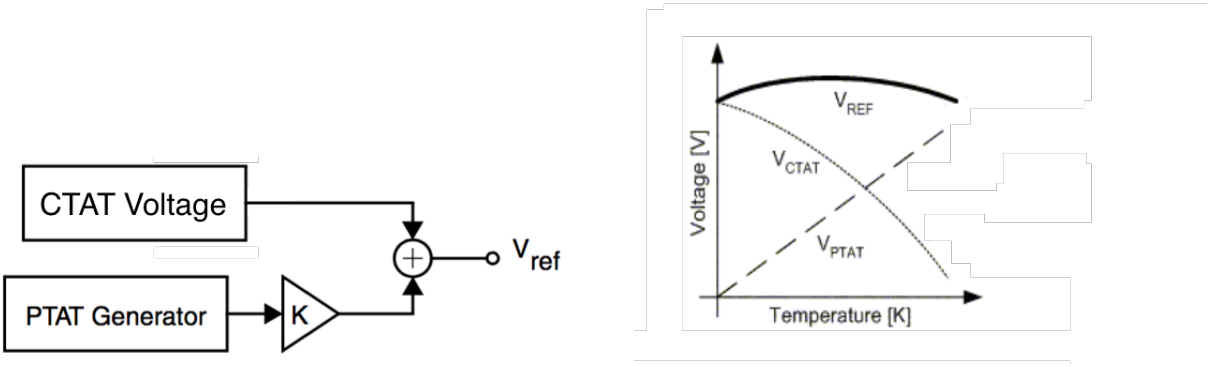

Figure 1.3 – General Bandgap Voltage Principle

Now, we need to find the component, or a characteristic that has a PTAT or CTAT behaviour. We are going to use the usual componenent, Bipolar and MOS transistor. In one hand, we can notice that the temperature coefficient of (evolution with respect to Temperature) V_{BE} is negative, as well as the V_{GS} of a MOS transitor. In the other hand, we can observe that two bipolar or MOS transistor working at a unequal current densities create a voltage that is proportionnal to $U_T = \frac{kT}{q}$ therefore PTAT voltage (Positive Temperature Coefficient - TC).

The bandgap voltage reference will be used in different block, and for applications with low power consumption. The design will then take into account some specifications related to these applications. We can resume the main specifications of this project in the next table :

	Typ	Maximum	Minimum
Current Consumption	1 μA	3 μA	—
Power Supply Voltage	1.8 V	2 V	1.5 V
Technology	UMC L180UMC L180		

Table 1.1 – Voltage Reference Specifications

2 Generate a CTAT Voltage

2.1 Evolution of V_{BE} with respect to temperature

The base-emmiter voltage of a bipolar transistors or, more generally, the forward voltage of a pn-junction diode show a negative TC. For a bipolar device such as represented in the Fig. 2.1

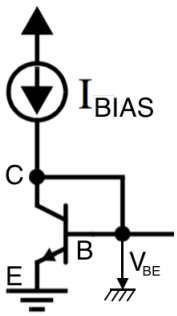

FIGURE 2.1 – Base-emitter Voltage Context

$$V_{BE} = \frac{k_B T}{q} \cdot ln\left(\frac{I_C}{I_S}\right) \tag{2.1}$$

With I_S, the saturation current which depend on the temperature through different characteristic (n_i, μ_0) that depend differently of temperature. In a first calculation, we suppose that the collector current I_C is independent of the temperature. After calculation (details on Appendix **??**) we obtain :

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)U_T - E_g/q}{T} \tag{2.2}$$

Where $m/approx - 3/2$ a process parameter, $E_g/approx 1.12eV$ the bandgap energy of silicon, $U_T = \frac{kT}{q}$ the thermal voltage. The equation 2.2, reveal the dependence of the TC of V_{BE} to the magnitude of V_{BE} itself. We then fix $V_B E \approx 700mV$, $T \approx 300K$ and we obtain $\frac{\partial V_{BE}}{\partial T} \approx -1.2mV/K$. In fact, in this part we limit our temperature analysis to the dependence to the first order of temperature which create a second order temperature dependence.

2.2 Bipolar Implementation in CMOS process

The implementation of a bipolar transitor in a CMOS process used here process a lateral bipolar transistor which can be better controled and processed with a much better accuracy than the vertical bipolar. In fact, during the process, the depth of oxydation in the silicon is controlled with much more difficulty whereas the oxydation of a specific area is much more controled and processed with a better accuracy. We then use a lateral transistor, processed and layouted as in the Fig 2.2 :

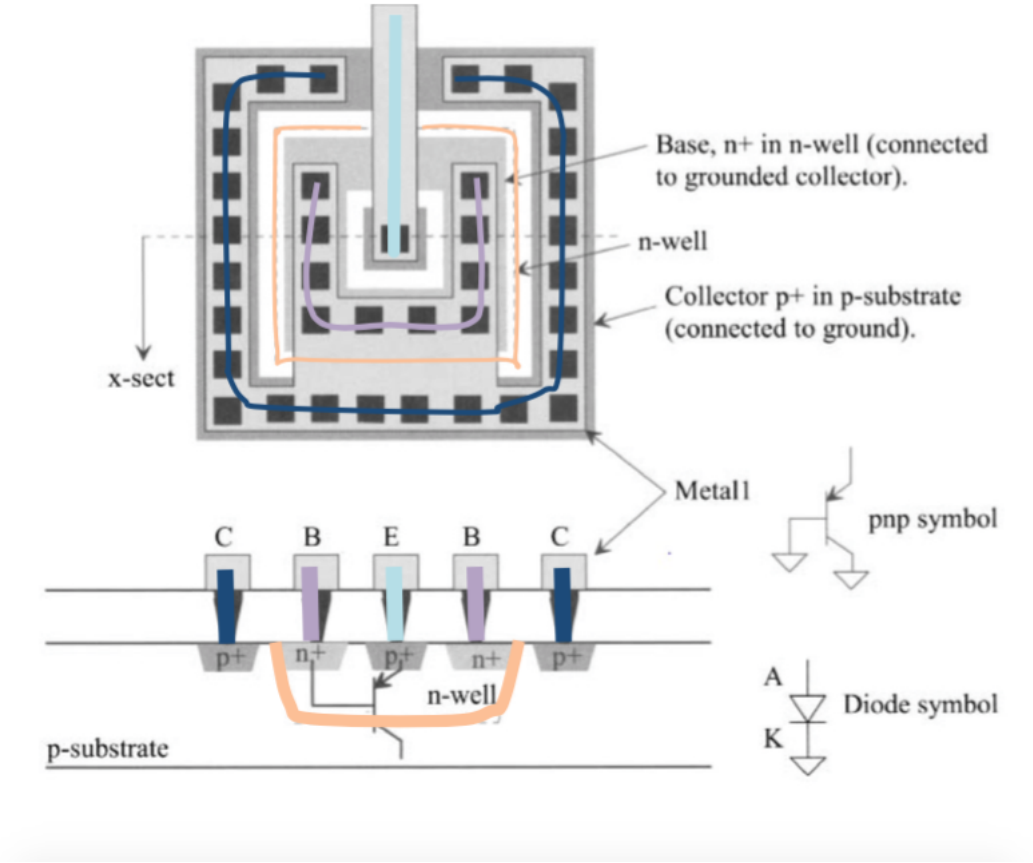

Figure 2.2 – Layout of PNP Bipolar Transitor

3 Generate a PTAT Voltage

3.1 Using Base-emitter Voltage

As said in the first chapter, we are going to use two bipolar transistor in two different current densities, and then the difference between their base-emitter voltage produce a voltage which is proportionnal to the thermal voltage, we then have a PTAT voltage.

We are going to use two branches with the same current I, and in one branch we are going to use n identical bipolar transitor and one bipolar transistor in the other branch ($I_{S2} = nI_S$ and $I_{S1} = I_S$).

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \tag{3.1}$$

$$= U_T ln\left(\frac{I_0}{I_{S1}}\right) - U_T ln\left(\frac{I_0}{I_{S2}}\right) \tag{3.2}$$

$$= \frac{kT}{q} \cdot ln(n) \tag{3.3}$$

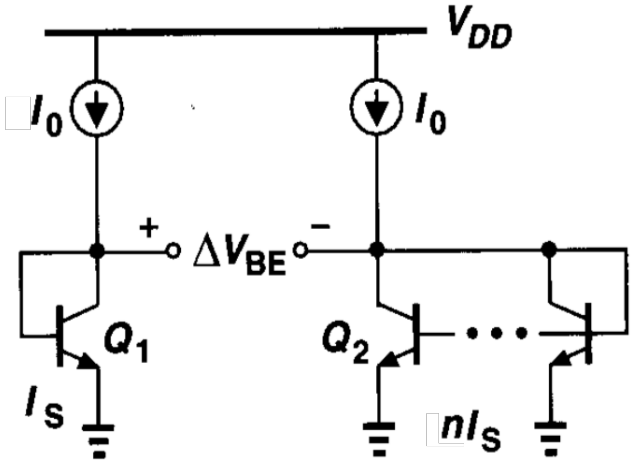

FIGURE 3.1 – Generate a PTAT Voltage

The precedent structure manipulate a differential voltage, the final idea is to add this voltage to a CTAT voltage which is not possible in a complete structure, so instead of generating a PTAT differential voltage, we generate a PTAT current which we can easily copy in another branch.

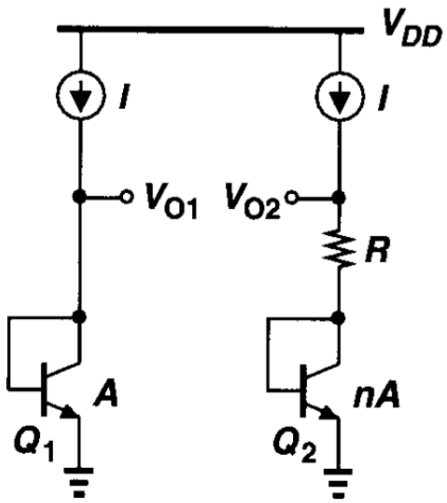

Figure 3.2 – Generate a PTAT Current

In this structure, we need also use a mechanism that will force $V_{O1} = V_{O2}$, we will use a operational amplifier with a high gain to force the two voltages to be equal.

$$V_{O1} = V_{O2} \tag{3.4}$$
$$V_{BE1} = RI + V_{BE2} \tag{3.5}$$
$$I = \frac{\Delta V_{BE}}{R} \tag{3.6}$$
$$= \frac{\frac{kT}{q} \cdot ln(n)}{R} \tag{3.7}$$

We obtain finally a PTAT current proportional to the thermal voltage that is easier to sum with a CTAT current or Voltage. Moreover we have two parameter n and R, that we can fix to cancel the negative temperature coefficient.

3.2 Using Gate-source Voltage

We use two transistor M1 and M2, which will operate in weak inversion with two different current densities. This region of operation have quasi the same way of variation than the bipolar transistor, whith a exponential dependence of the drain current with respect to the gate-source voltage.

$$I_{DS} = I_{SPECs} \cdot \frac{W}{L} \cdot exp\left(q\frac{V_{gs} - V_t}{nkT}\right) \tag{3.8}$$
$$I_{SPECs} = 2n\mu_n C_{ox} U_t^2 \tag{3.9}$$

In the same way, we use an Opamp to ensure that the two voltages V_A V_B are equal. We use the same current in the two branches, and we size the transistor M2 m times larger than M1, we then have :

$$V_{GS1} = nU_T \cdot ln\left(\frac{I_{DS1} \cdot L_1}{I_{SPECs} \cdot W_1} + V_{T0}\right) \tag{3.10}$$

$$V_{GS2} = nU_T \cdot ln\left(\frac{I_{DS2} \cdot L_2}{I_{SPECs} \cdot W_2} + V_{T0}\right) \tag{3.11}$$

$$\frac{W_2}{L_2} = m \cdot \frac{W_1}{L_1} \tag{3.12}$$

In the same logic we obtain a current I_{R1} which is proportional to ΔV_{GS}, in fact the final theoritical expression of $I_{R1} = \frac{\Delta V_{GS}}{R_1}$ with :

$$\Delta V_{GS} = \ n \ \frac{kT}{q} ln(m) \tag{3.13}$$

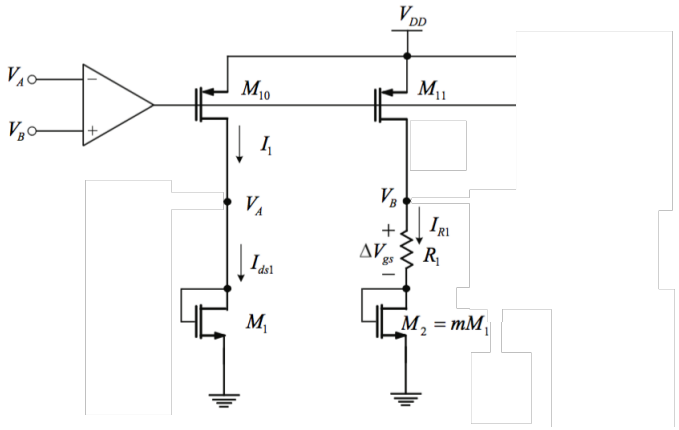

Figure 3.3 – Generate a PTAT Current with MOS transistor

The final result is very similar to the bipolar "version", except that for the MOS version, ΔV_{GS} is proportionnal to the slope factor, except that this parameter is dependent of the temperature, the variation can be neglected for the dependence of the first order of temperature.

4 Bandgap Voltage

4.1 Current Source - Beta-Multiplier

As we are limited to 3 μA in current consumption, we are going to limit the current consumption in the current source to the minimum. We decide then to produce a current of 100 nA that we are going to mirror in the different branches to generate a PTAT and a CTAT voltage. To generate this current, we are going to use the structure in the Fig 4.1 :

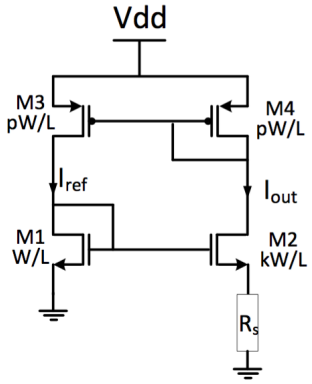

FIGURE 4.1 – Beta-Multiplier Current Source with Cascode

For such low current, we use the two transistor M1 and M2 in weak inversion, and to obtain a good current mirror with respect to mismatch and have then I_{ref} quasi equal to I_{out} we put the transistor M3 and M4 in strong inversion. We can then used the simplified equation of the drain current in weak inversion, given by the EKV model :

$$I_{out} = I_{spec} \cdot exp\left(\frac{V_G - nV_S - V_{T0}}{nU_T}\right) \tag{4.1}$$

If we apply this equation to the transitor M1 and M2, with M2 k times larger than M1, we have the final expression of I_{out} :

$$I_{out} = I_{ref} = \frac{U_T \cdot ln(k)}{R_S} \tag{4.2}$$

The main problem of this structure is the dependence of the current I_{out} to the absolute value of R_S, which make the current depend on process variation. In fact, the absolute value of R_S have a global precision of ± 20 %.

The other important dependence of I_{out} is to the varation of V_{DD} by ΔV_{DD}. Therefore, we have to do a small signal analysis of the varation ΔI_{out} of I_{out} with a varation of V_{DD} by ΔV_{DD}. The details of the calculation are shown in the Appendix B.1, but we have finally :

$$\frac{\Delta I_{out}}{\Delta V_{DD}} \approx \frac{1}{r_{on}} + \frac{2}{r_{op}} \tag{4.3}$$

With r_{on} and r_{op} respectively the output resistance of the NMOS and PMOS transistor, as shown in the Appendix B.1 . Therefore, to decrease the dependence of I_{out} to V_{DD}, we have to increase r_{on} and r_{op}, to do that we are going to use a cascode structure for the NMOS transistor and increase the length of the PMOS transistor to increase r_{op}. The final structure is shown on Fig 4.2 :

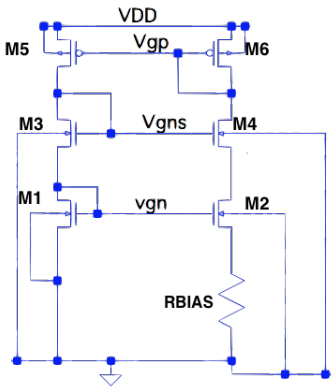

Figure 4.2 – Beta-Multiplier Current Source with Cascode

As the transistor M1 and M2 should work on weak inversion we choose an inversion coefficient $IC(M1)$ =????? and we choose k = 4, so $\frac{W_2}{L_2} = 4 \cdot \frac{W_1}{L_1}$ To maximize the swing we put the voltage V And finally, the transistor M5 and M6, should work on strong inversion, so we choose an inversion coefficient IC =????? so we can have a very large value of L_5 and L_6. We have finally :

$W_1 = 4\ \mu m$	$L_1 = 180\ nm$
$W_2 = 16\ \mu m$	$L_2 = 180\ nm$
$W_3 = W_4 = 5\ \mu m$	$L_3 = L_4 = 250\ nm$
$W_5 = W_6 = 250\ nm$	$L_5 = L_6 = 3.2\ \mu m$

Table 4.1 – Beta-Multiplier transitor dimension

4.2 Single Stage OTA

The specifications impose us a very low current consumption (max 3 μA), though the amplifier need to have a very high gain so we can have $V_{O1} = V_{O2}$, Fig. 3.2, and then we need enough current to have enough gain, we decide to fix a gain $A_0 = 500 \approx 50\ dB$.

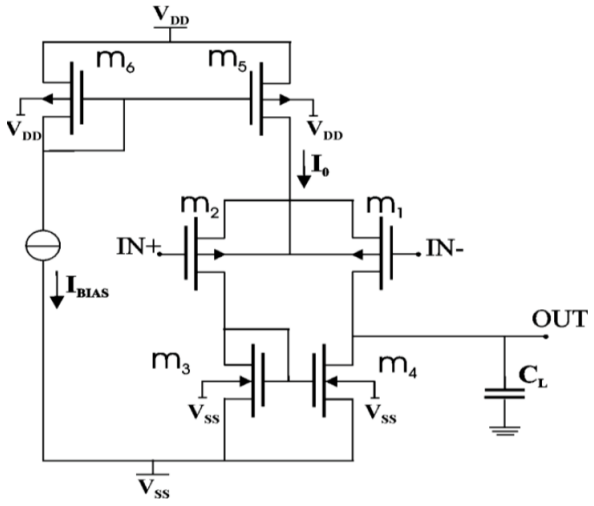

Figure 4.3 – OTA with PMOS differential pair

The transistor m1 and m2 have the same size and the transistor m3 and m4 too. We choose then a current $I_D(m5) = I_0 = 500\ nA$, we have then $I_D(m1, m2, m3, m4) = I_0/2 = 250\ nA$. We fix also the gain band width (GBW) to 10 kHz and a load capacitance $C_L = 1\ pF$. We can use the expression of the unity gain frequency express $g_m(m1, m2)$:

$$g_m(m1, m2) = GBW \cdot C_L = 10 \cdot 10^{-9} \cdot \Omega^{-1} \tag{4.4}$$

We have the value of g_m and the current flowing on the transitors m1 and m2 we can now determine their inversion coefficient and then deduce the $\frac{W}{L}$ of the differential pair :

$$\frac{g_m}{I} = \frac{1}{nU_T} \cdot \frac{2}{\sqrt{1 + 4IC} + 1} \tag{4.5}$$

$$\frac{W}{L}(m1, m2) = \frac{I_0/2}{I_{spec_\square} \cdot IC} \tag{4.6}$$

We know that the output resistance is related to the length of the transistor m1 and m4 due to the channel length modulation,eq. 4.7, moreover if we do the small signal analysis we can also link the gain A_0 to R_{out}, eq 4.8. Finally, to size the NMOS current mirror we fix the overdrive voltage $V_{ov} = 200\ mV$ and deduce the W/L thanks to Eq 4.9.

$$L(m1, m4) = I_0/2 \cdot R_{out} \left(\frac{1}{U_{aN}} + \frac{1}{U_{aP}} \right) \tag{4.7}$$

$$A_0 = R_{out} \cdot g_m(m1, m2) \tag{4.8}$$

$$\frac{W}{L}(m3, m4) = \frac{2n \cdot I_0/2}{\mu_n C_{ox} V_{ov}^2} \tag{4.9}$$

The final dimension of the transistors are resumed in the next table :

$W_1 = W_2 = 1.47\ \mu m$	$L_1 = L_2 = 5.31\ \mu m$
$W_3 = W_4 = 12.05\ \mu m$	$L_3 = L_4 = 5.31\ \mu m$
$W_5 = 1.25\ \mu m$	$L_5 = 3.2\ \mu m$

Table 4.2 – OTA transitor dimension

4.3 Overall circuits

4.3.1 Bandgap Voltage Reference

The final circuits is composed of the PTAT circuits using a current mirror to copy the current in the two branches, these two transistor (M3,M4) are biased thanks to the beta-multiplier current source, in fact in each branch we use a current of 250 nA. The operational amplifier equalize the voltage V_A and V_B and therfore produce a PTAT current. This current is copied in the third branch (right one) and converted to a PTAT voltage thanks to the resistance R_2 and then added to the base-emitter voltage of the PNP bipolar transistor.

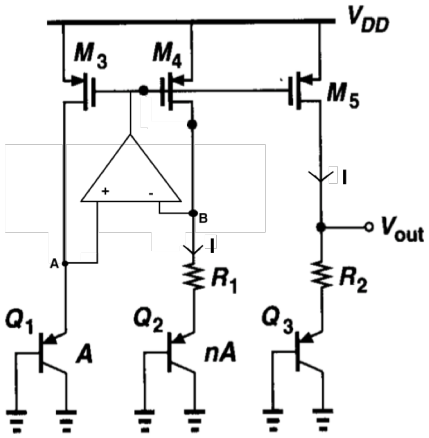

Figure 4.4 – Bandgap Voltage Reference

$$V_{ref} = V_{BE3} + \frac{R_2}{R_1}\Delta V_{BE} = V_{BE3} + \frac{R_2}{R_1} \cdot \frac{kT}{q} ln(n) \tag{4.10}$$

The final equation to cancel the temperature

$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{BE3}}{\partial T} + \frac{R_2}{R_1} \cdot \frac{k}{q} ln(n) \tag{4.11}$$

$$\frac{R_2}{R_1} = -\frac{\frac{\partial V_{BE3}}{\partial T}}{\frac{k}{q} ln(n)} \tag{4.12}$$

The final current consumption is $200\ nA + 3 \cdot 250\ nA + 500\ nA = 1.450\ \mu A$, the final voltage is quasi-independent of the temperature but the current generated on the third branch is PTAT, we have only a bandgap voltage, moreover for low power applications it's very interesting to have a voltage inferior to 1V, as it's usually used in low power device. The cancelation of the two temperature coefficient is done thanks to the quotient of the two resistance, so the cancelation doesn't depend on process varation, in fact if the process create an imprecision of +20 % on R_1,for instance, the resistance R_2 is also 20 % higher than the nominal value.

$W_3 = W_4 = W_5 = 625\ nm$	$L_3 = L_4 = L_5 = 3.2\ \mu m$
$R_1 = \Omega$	$R_2 = \Omega$
n = 4n = 4	

Table 4.3 – Bandgap Voltage Reference Dimensions

4.3.2 Sub-1V Bandgap Current and Voltage Reference

A problem with the bandgap circuits described so far is that they are not compatible with low power applications, that usually need a reference voltage sub 1V. The fundamental problem is that the previous circuits produce, in series, the CTAT voltage across a pn-junction and a PTAT voltage scaled to provide temperature- independence. Together, these voltages exceed 1 V. The solution is to sum currents : one CPTAT and one PTAT, passing them through a resistor to form a temperature-insensitive reference voltage below 1 V. A low-voltage bandgap circuit based on this idea is shown in Fig. 4.5. The feedback loop formed by the amplifier and current mirror Q1 /Q2 ensures that the voltages at the drains of Q1 and Q2 are very well matched and equal to the base-emitter voltage drop across diode D , V_{BE1} , which is inversely proportional to absolute temperature.

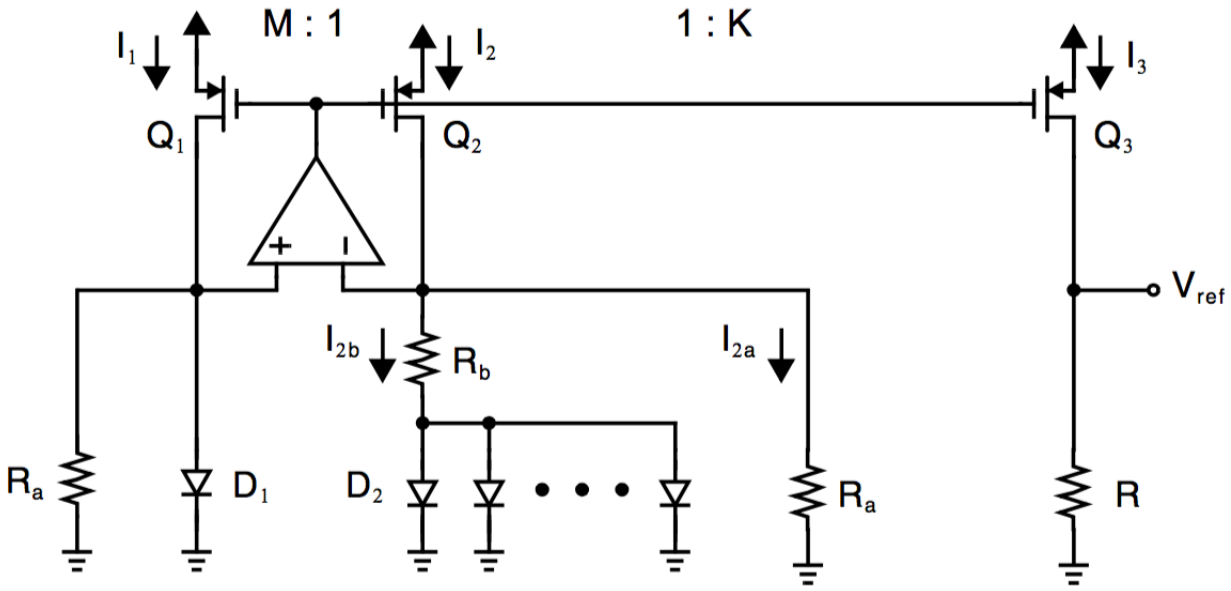

Figure 4.5 – Bandgap Voltage and Current Reference

The CTAT voltage V_{BE1} and PTAT ΔV_{BE} are converted into the currents I2a and I2b by the resistors Ra (4.13) and Rb,(4.13) respectively. These two currents are summed at the drain of Q2 and mirrored to device Q3 . The resulting current then passes back through resistor R to yield the reference output.

$$I_{2a} = \frac{V_{BE1}}{R_a} \tag{4.13}$$

$$I_{2a} = \frac{\Delta V_{BE}}{R_b} \tag{4.14}$$

The values M, N, Ra, and Rb are chosen to ensure that the inverse temperature coefficient of the first term is pre- cisely cancelled by the positive temperature coefficient of the second term. Notice that nowhere are there DC volt- ages exceeding VBE, so this circuit has been used with supply voltages as low as 0.8 V. The values of K and R can be chosen to scale the actual value of the reference potential

at Vref, while the values of N, Ra and Rb are chosen to cancel the negative and positive temperature coefficients of the first and second terms in (4.15).

$$V_{ref} = V_{BE1}\frac{KR}{R_a} + \frac{kT}{q}ln(N)\frac{KR}{R_b} \tag{4.15}$$

5 Results after Simulation

5.1 Dependence to VDD

5.2 Temperature Dependence

5.3 Simulation Post route

Conclusion

Annexes

A Evolution of V_{BE} with respect to temperature

The details of the calculation of the dependence of V_{BE} to temperature. We fisrt devellop the temperature dependence :

$$V_{BE} = \frac{k_B T}{q} \cdot ln\left(\frac{I_C}{I_S}\right) \tag{A.1}$$

$$I_S \ \alpha \ \mu \ kT \ n_i^2 \tag{A.2}$$

$$\mu \ \alpha \ \mu_0 \ T^m \tag{A.3}$$

$$n_i^2 \ \alpha \ T^3 \cdot exp\left(\frac{E_g}{kT}\right) \tag{A.4}$$

With μ the mobility of the carriers, n_i the intrinsic carrier concentration of silicon and $E_g \approx 1.12eV$ the bandgap energy of silicon.

We introduce a parameter b, which is a proprtionnality factor :

$$I_S = bT^{4+m} \cdot exp\left(\frac{E_g}{kT}\right) \tag{A.5}$$

Once we have devellop the expression with respect with T, we start to derivate the expression :

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial U_T}{\partial T} \cdot ln\left(\frac{I_C}{I_S}\right) + \frac{\partial I_S}{\partial T} \cdot \frac{U_T}{I_S} \tag{A.6}$$

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m} \cdot exp\left(\frac{E_g}{kT}\right) + bT^{4+m}\left(exp\left(\frac{E_g}{kT}\right)\right) \cdot \frac{E_g}{kT^2} \tag{A.7}$$

$$\frac{U_T}{I_S}\frac{\partial I_S}{\partial T} = (4+m)\frac{U_T}{T} + \frac{E_g}{kT^2} \cdot U_T \tag{A.8}$$

We obtain finally :

$$\frac{\partial V_{BE}}{\partial T} = \frac{U_T}{T} ln\left(\frac{I_C}{I_S}\right) - (4+m)\frac{U_T}{T} - \frac{E_g}{kT^2} \cdot U_T \tag{A.9}$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)U_T - E_g/q}{T} \tag{A.10}$$

B Output resistance of Beta Multiplier Current Source

We can first draw the small signal schematic :

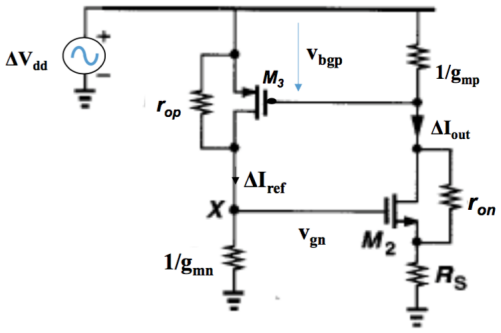

FIGURE B.1 – Small Signal Analysis

We have the in the right branch :

$$\Delta V_{DD} = \frac{\Delta I_{out}}{g_{mp}} + R_s \cdot \Delta I_{out} + r_{on} \cdot (\Delta I_{out} - g_{mn}(M2) \cdot v_{gn} + n \cdot g_{mn}(M2) \cdot R_S \Delta I_{out}) \tag{B.1}$$

$$\Delta V_{DD} \approx 3 \cdot r_{on} \Delta I_{out} - 2 \cdot r_{on} g_m v_{gn} \tag{B.2}$$

We have the in the left branch :

$$\frac{\Delta V_{DD} - v_{gn}}{r_{op}} + g_{mp} \frac{\Delta I_{out}}{g_{mp}} = g_{mn} v_{gn} \tag{B.3}$$

$$g_{mn}\ v_{gn} \approx \frac{\Delta V_{DD}}{r_{op}} + \Delta I_{out} \tag{B.4}$$

Finaly we have :

$$\frac{\Delta I_{out}}{\Delta V_{DD}} \approx \frac{1}{r_{on}} + \frac{2}{r_{op}} \tag{B.5}$$

C ANNEXE C