Environment setup

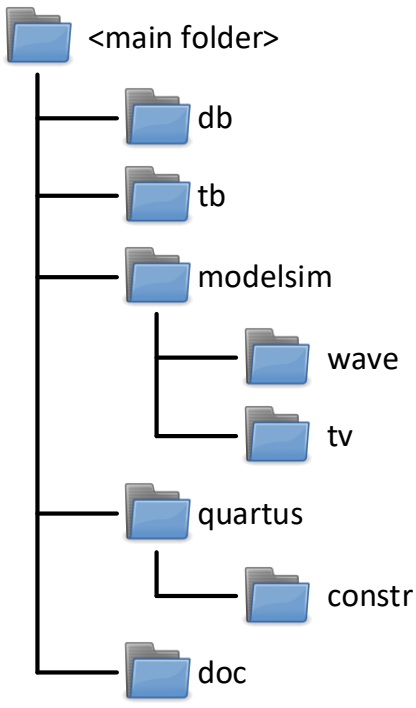
Before using the environment you need to satisfy the following requirements:

- Add (permanently) the path of the Quartus and Modelsim executables to the PATH environment variable
  - for Quartus, the path of the folder containing the quartus/quartus.exe executable
  - for Modelsim, the path of the folder containing the vsim/vsim.exe executable

- Python (versions 2.x or 3.x), with packages
  - os
  - sys
  - shutil
  - glob

Environment guide

Structure of the environment:



The **doc/** folder contains all the documents related to the project development and this environment. Please, put here also the project report upon delivery.

The **db/** folder must be used for the RTL design files.

The **tb/** folder must be used for the testbench files.

Create and add a folder named **model/** for the high-level model files.

The **modelsim/** and **quartus/** folders are intended to be used for the Modelsim and Quartus tools, respectively. They include Python scripts and sub-folders that facilitate the use of these tools.

- **modelsim/**
  - Use **tv/** and **wave/** sub-folders to include test vectors and waveforms, respectively.
  - **build.py** script: it automatically creates a Modelsim project in the modelsim/ folder that includes all the SystemVerilog files that are in the db/ and tb/ folders.
  - **clean.py** script: it cleans the modelsim/ folder by removing all files except tv/ and wave/ sub-folders, build.py script and the clean.py script itself.

- **quartus/**
  - Use **constr/** sub-folder to include constraints file(s). It also includes the **automatic_virtual_pin.tcl** script by default, which can be used in Quartus to automatically perform the virtual pins assignment to all top-level ports except the clock port. For this purpose, the clock port must be named clk.
  - **build.py** script: by exploiting the **quartus.build** file, it automatically creates a Quartus project in the quartus/ folder that includes all the SystemVerilog files that are in the db/ folder, all the constraints file(s) in the constr/ sub-folder, the automatic_virtual_pin.tcl script in the constr/ sub-folder, and select the FPGA device 5CGXFC9D6F27C7. Upon launch, the script prompts for the **top-level name**.
  - **clean.py** script: it cleans the quartus/ folder by removing all files except constr/ sub-folder, build.py script, quartus.build file, and the clean.py script itself.

Note: before delivering the project for the exam, **please run the clean scripts inside folders quartus/ and modelsim/**, so that Modelsim and Quartus projects files are not included within the delivery, but they are included all and only the files relevant to the project, i.e.

- **model file(s)** inside **model/** (content of model/ not affected by clean scripts)
- **design file(s)** inside **db/** (content of db/ not affected by clean scripts)
- **testbench(es) file(s)** inside **tb/** (content of tb/ not affected by clean scripts)
- **project report** inside **doc/** (content of doc/ not affected by clean scripts)
- **testvector(s) file(s)** in **modelsim/tv/** (content of modelsim/tv/ not affected by clean scripts)
- **constraint(s) file(s)** in **quartus/constr/** (content of quartus/constr/ not affected by clean scripts)