Designing a Pulse Width Modulation Brightness Controller for a Nixie Tube Display

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1 Background

This writing sample is compiled from working notes about a personal electronics project: an alarm clock with a Nixie tube display that incorporates time, data, alarm, and snooze functions, and uses the 60 Hz power line utility frequency as a stable time base with exceptionally low long-term drift. For an extra challenge, this project is restricted to using only components and design techniques that existed in the 1970s when Nixie tubes were in common use; namely, 74xx-series discrete logic and discrete bipolar transistors. This writing sample presents the design and simulation of the display brightness control circuit, which uses pulse width modulation (PWM) to control the brightness of the Nixie tubes. The display brightness control circuit is based around the NE555, a multipurpose timer IC introduced in 1972.

1.1 Controlling Brightness with Pulse Width Modulation

Pulse width modulation brightness control is a technique that exploits the flicker fusion threshold of the human eye – the frequency at which a flickering light appears steady to a human observer – to convert a rapidly flickering display into a steady perceived brightness. To control display brightness using pulse width modulation, the display is rapidly enabled and disabled by a square wave with variable duty cycle. If the frequency of the square wave is faster than the flicker fusion threshold, the eye and brain filter out the flickering, and the display appears to have a consistent brightness.[1] The perceived brightness of the display is proportional to the duty cycle of the square wave. If the duty cycle of the square wave is small, the display will appear dim. Likewise, if the duty cycle of the square wave is large, the display will appear bright.

1.2 Nixie Tube Basics

A Nixie tube is a cold-cathode display tube that operates on the same principle as a neon lamp. Applying a high voltage between the tube's anode and cathode electrodes causes a brightly-glowing ionized plasma to form in the shape of the cathode. Cathode electrodes can be made in the shape of numerals, letters, or other symbols, and the color of the glow is determined by the low-pressure gas mixture inside the tube. This project uses the IN-12A Nixie tube, a Russian-made numeric indicator tube with one anode and ten cathodes shaped like numerals from 0 to 9.

Nixie tubes, have a finite turn-on time, called the striking time, between when the striking voltage is applied and when the tube is illuminated. The striking time is defined as the delay between when the striking voltage is applied and when the voltage across the tube collapses from the striking voltage to the steady-state voltage. Figure 1 illustrates the transient turn-on behavior of an IN-12A Nixie tube. The IN-12A takes approximately 80 µs to reach steady state after the striking voltage is applied.

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[1] The ability of humans to detect a flicker also depends on the modulation depth (the difference in intensity between when the light is on and off), average amplitude, and wavelength, plus physiological factors like age, fatigue, and dark adaptation.
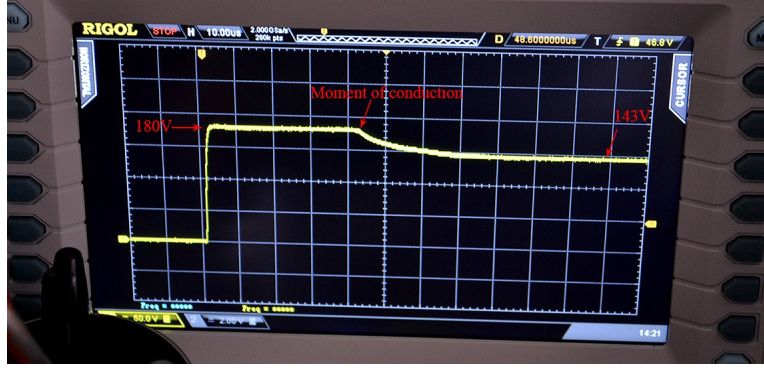
Figure 1: Transient anode voltage of an IN-12A Nixie tube. Source: Hackaday

1.3 Perceived Nixie Tube Brightness

We typically assume that pulse width modulation provides constant linear control of perceived brightness. However, the finite striking time of a Nixie tube produces two dead zones in the brightness control curve. A dead zone is a region of operation where the tube's perceived brightness does not respond to changes in PWM duty cycle. Figure 2 plots the perceived brightness of an ideal perceived brightness and actual perceived brightness display and a Nixie tube display versus PWM duty cycle. The two dead zones appear as flat regions in the brightness control curve.
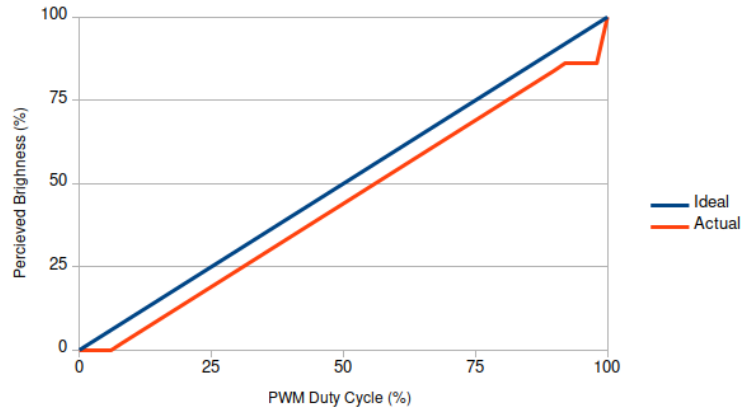

Figure 2: Plot of desired brightness and actual brightness versus PWM duty cycle for a Nixie tube display. The Nixie tube's finite turn-on time creates two dead zones (flat regions) in the brightness curve.

The first dead zone appears at low brightness settings when the tube is only on for a very short amount of time each cycle. If the PWM pulse width is less than the striking time, the tube will simply not illuminate. This creates a flat region in the brightness control curve where the tube will not respond to changes in PWM duty cycle because it is always off. The second dead zone appears at very high brightness settings, when the tube is only off for a short amount of time each cycle. At very high brightness settings, the PWM signal attempts to turn the tube off and on again faster than the tube can respond. The tube can turn off almost instantly; however, once the tube is off, it requires the entire striking time to turn back on again. This creates a flat region in the brightness control curve at high PWM duty cycles, where the striking time, not the PWM signal, dictates the display's duty cycle. Increasing the brightness setting beyond this point will not produce any change in brightness until the PWM duty cycle reaches 100% (tube always on), at which point the tube's perceived brightness will suddenly jump up to 100%. For the best user experience, we will design a display brightness circuit that restricts the PWM duty cycle to the linear brightness region between the two dead zones.

2 Designing the Display Brightness Circuit

Our analysis of Nixie tube operation in the previous section allowed us to identify some design requirements for our display brightness circuit. We desire a circuit that outputs a signal with the following characteristics:

- CMOS-compatible square-wave output

- Constant output frequency

- Variable output pulse width (to control brightness)

- Programmable minimum and maximum pulse width (to prevent dead zones)

- Output pulse width is a linear function of brightness knob position (for ease of use)

The 555 timer circuit in Figure 3 might be a good starting point. This circuit is frequently posted on electronics hobby forums claiming to be a PWM brightness controller without any analysis or explanation about how it works. We will analyze this circuit, discover how it works, and develop a set of design equations that allow us to select component values.
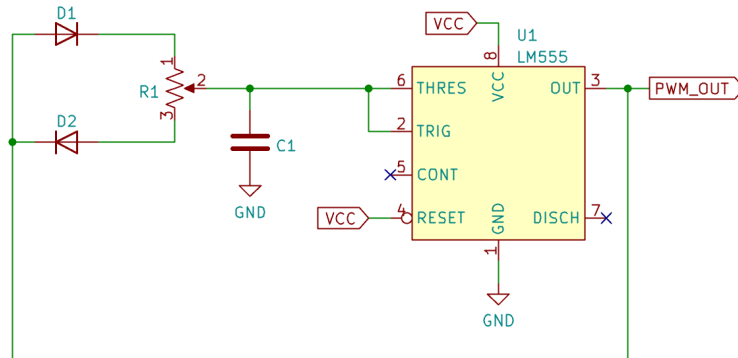
Figure 3: A pulse width modulation generator circuit using a 555 timer.

2.1 Theory of Operation

The 555 is a multipurpose timer IC that can be configured as a timer, an oscillator, a pulse generator, or a delay circuit using a few external components. In this case, the timer is configured as a free-running oscillator. Figure 4 is a functional block diagram of the 555 timer.
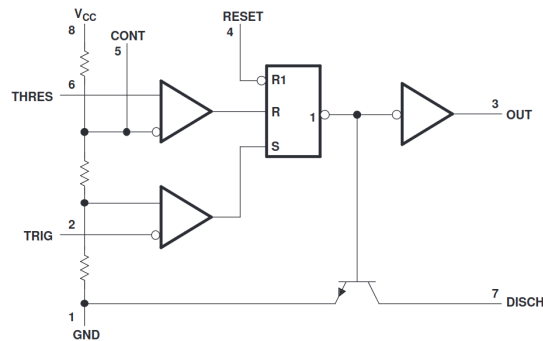
Figure 4: Functional block diagram of the 555 timer. Source: Texas Instruments

The 555 timer contains two comparators, an SR latch, and an output buffer, as well as a bipolar transistor that can be used as an open-collector switch. By default, an internal resistor divider programs the threshold voltage of the top comparator to 2/3 of the power supply voltage and the threshold voltage of the bottom comparator to 1/3 of the power supply voltage. In our circuit, the THRES and TRIG pins (the comparator inputs) are tied together and connected to timing capacitor C_1, which is charged and discharged by the timer output pin. Diodes D_1 and D_2 force the capacitor to charge through one half of the potentiometer and discharge through the other half of the potentiometer. To analyze this circuit, we replace the two halves of potentiometer R_1 with resistors R_{1a} and R_{1b} as shown in Figure 5.
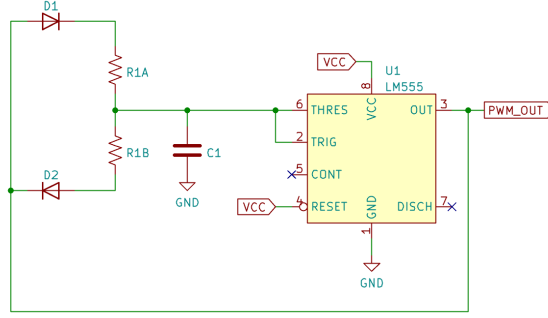

Figure 5: Equivalent circuit of the PWM brightness controller in Figure 3.

Capacitor C_1 begins charging when the timer output goes high. When the timer output is high, C_1 charges through diode D_1 and R_{1a} (the top half of the potentiometer) until the capacitor voltage exceeds the threshold voltage of the top comparator, causing the top comparator to assert the RESET input of the SR latch. Clearing the latch forces the timer output low, and C_1 discharges through diode D_2 and R_{1b} (the bottom half of the potentiometer) until the capacitor voltage drops below the threshold voltage of the bottom comparator, causing the bottom comparator to assert the SET input of the SR latch. Setting the latch forces the timer output high, and the charging cycle begins again. Adjusting the potentiometer position changes the ratio of R_{1a} to R_{1b}, allowing users to increase or decrease the ratio of charge time to discharge time and change the output pulse width.

2.2   Design Equations

To analyze this circuit, let us first establish a mathematical relationship between R_{1a} and R_{1b}, the the two halves of potentiometer R_1. Let b, the brightness setting, correspond to the position of the potentiometer. We say that b can take values between 0 and 1, where 0 corresponds to the minimum potentiometer position (minimum brightness) and and 1 corresponds to the maximum potentiometer position (maximum brightness). Since the ratio of R_{1a} to R_{1b} is set by the potentiometer position, we can write:

$$R_{1a} = bR_1$$
$$R_{1b} = (1-b)R_1 \tag{2.1}$$

At the minimum brightness setting ($b = 0$), the resistance of R_{1a} is zero, and the resistance of R_{1b} is maximized. The capacitor charges almost instantly, but discharges very slowly. This generates a PWM waveform with a duty cycle approaching 0%. At the maximum brightness setting ($b = 1$), the resistance of R_{1a} is maximized, and the resistance of R_{1b} is zero. The capacitor charges very slowly, but discharges almost instantly. This generates a PWM waveform with a duty cycle approaching 100%.

2.3   Deriving Capacitor Charge and Discharge Time

In order to calculate the charge and discharge times, we need an expression for $v_{C1}(t)$, the voltage across capacitor C_1 as a function of time. From circuit theory, we remember that the voltage across a capacitor in

a series RC circuit can be expressed as

$$v_{C1}(t) = \tau \frac{dv_{C_1}(t)}{dt} \tag{2.2}$$

where τ is the time constant. The expression in Equation 2.3 is an ordinary differential equation whose solution has the form

$$v_{C_1}(t) = A \exp \frac{-t}{\tau} + B \tag{2.3}$$

where A and B are constants defined by the boundary conditions of the system; in this case, the initial and final conditions of the capacitor. This form of the solution is valid for both charging and discharging RC circuits - the only difference will be the values of A and B.

Equation 2.3 can be used to solve for the charge and discharge times. To start, we define the charge time t_H as the length of time the output is high and the capacitor is charging. Similarly, we define the discharge time t_L to be the length of time the output is low and the capacitor is discharging. Since the charge and discharge paths see different series resistances, they will have different time constants. Let τ_H be the time constant for the charging path, and let τ_L be the time constant for the discharging path. From Figure 5, we can see by inspection that:

$$\begin{aligned} \tau_H &= R_{1a}C_1 = bR_1C_1 \\ \tau_L &= R_{1b}C_1 = (1-b)R_1C_1 \end{aligned} \tag{2.4}$$

We consider the charging case first. The charging case has a boundary condition $v_{C_1}(0) = \frac{1}{3}V_{CC}$ because the capacitor voltage is equal to the threshold voltage of the lower comparator immediately before charging starts. The charging case also has a boundary condition $v_{C_1}(\infty) = (V_{CC} - V_F)$, where V_F is the forward voltage of diode D_1, because if the timer output were to never go low again, the capacitor would charge up to one diode drop below the power supply voltage. Applying these boundary conditions to equation 2.3, we obtain the solution for the charging capacitor:

$$v_{C_1}(t) = (V_{CC} - V_F) + \left(-\frac{2}{3}V_{CC} + V_F\right) \exp \frac{-t}{\tau_H} \tag{2.5}$$

We use this equation to solve for t_H, the length of time the timer output is high and the capacitor is charging. At the end of the charging cycle, we know $v_{C_1}(t_H) = \frac{2}{3}V_{CC}$, the threshold voltage of the top comparator. We write:

$$\frac{2}{3}V_{CC} = (V_{CC} - V_F) + \left(-\frac{2}{3}V_{CC} + V_F\right) \exp \frac{-t_H}{\tau_H} \tag{2.6}$$

Solving equation 2.6 for t_H yields:

$$t_H = -\tau_H \ln\left(\frac{\frac{1}{3}V_{CC} - V_F}{\frac{2}{3}V_{CC} - V_F}\right) \tag{2.7}$$

The discharging case has boundary conditions $v_{C_1}(0) = \frac{2}{3}V_{CC}$ and $v_{C_1}(\infty) = V_F$. Applying these boundary conditions to equation 2.3, we obtain the solution for the discharging capacitor:

$$v_{C_1}(t) = V_F + \left(\frac{2}{3}V_{CC} - V_F\right) \exp \frac{-t_L}{\tau_L} \tag{2.8}$$

We use this equation to solve for t_L, the length of time the timer output is low and the capacitor is discharging. At the end of the discharge cycle, we know $v_{C_1}(t_L) = \frac{1}{3}V_{CC}$, the threshold voltage of the bottom comparator. We write:

$$\frac{1}{3}V_{CC} = V_F + \left(\frac{2}{3}V_{CC} - V_F\right) \exp \frac{-t_L}{\tau_L} \tag{2.9}$$

Solving equation 2.9 for t_L yields:

$$t_L = -\tau_L \ln\left(\frac{\frac{1}{3}V_{CC} - V_F}{\frac{2}{3}V_{CC} - V_F}\right) \tag{2.10}$$

Note that equations 2.7 and 2.10 share the same logarithmic term. For neatness, we can replace this term with a constant k, where:

$$k = \ln\left(\frac{\frac{1}{3}V_{CC} - V_F}{\frac{2}{3}V_{CC} - V_F}\right) \tag{2.11}$$

This allows us to greatly simplify the expressions for t_H and t_L.

$$t_H = -k\tau_H$$
$$t_L = -k\tau_L$$
(2.12)

2.4 Deriving PWM Frequency and Duty Cycle

We can now use the expressions in 2.12 to write equations for PWM frequency and duty cycle. The PWM frequency f_{PWM} is given by

$$f_{PWM} = \frac{1}{t_H + t_L} = \frac{-1}{k(\tau_H + \tau_L)}$$
(2.13)

Substituting our expressions for τ_H and τ_L into this equation yields

$$f_{PWM} = \frac{-1}{kR_1C_1}$$
(2.14)

This result says that the PWM frequency is set by the total value of R_1 and C_1 and is independent of the potentiometer position. Changing the brightness setting only adjusts the PWM duty cycle, not the PWM frequency.

We can also write an expression for the PWM duty cycle. Duty cycle is given by

$$DC = \frac{t_H}{t_H + t_L} = \frac{\tau_H}{\tau_H + \tau_L}$$
(2.15)

Substituting our expressions for τ_H and τ_L into this equation yields:

$$DC = \frac{bR_1C_1}{bR_1C_1 + (1-b)R_1C_1} = b$$
(2.16)

Equation 2.15 says the PWM duty cycle is only a function of potentiometer position, and isn't dependent on any circuit parameters. This is a useful result, but it isn't quite what we need. In Section 1.3, we discussed the need to limit the minimum and maximum PWM duty cycle to prevent dead zones in the brightness control curve caused by the finite Nixie tube striking time. Can we modify the circuit in Figure 3 to allow us to program a minimum and maximum duty cycle?

2.5 Limiting the Minimum and Maximum Duty Cycle

One option for setting fixed minimum and maximum duty cycles is shown in Figure 6. Adding resistor R_2 in series with the potentiometer wiper forces a minimum resistance in both the charge and discharge paths regardless of the potentiometer position. The minimum resistance prevents the capacitor from charging or discharging instantly, thereby setting a minimum and maximum duty cycle. Since the minimum resistance in the charge and discharge paths is the same, the duty cycle limits are symmetric.
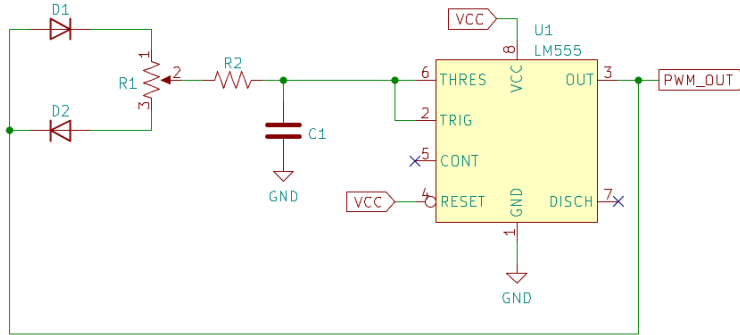

Figure 6: Modified PWM brightness control circuit. R_2 sets the minimum and maximum duty cycle limit.

For the circuit in Figure 6, the PWM frequency and duty cycle are given by

$$f_{PWM} = \frac{-1}{k\left(\tau_H + \tau_L\right)} = \frac{-1}{k\left(R_1 + 2R_2\right)C_1} \tag{2.17}$$

$$DC = \frac{\tau_H}{\tau_H + \tau_L} = \frac{bR_1 + R_2}{R_1 + 2R_2} \tag{2.18}$$

The minimum duty cycle limit is found by setting $b = 0$:

$$DC_{min} = \frac{R_2}{R_1 + 2R_2} \tag{2.19}$$

The maximum duty cycle is found by setting $b = 1$

$$DC_{max} = \frac{R_1 + R_2}{R_1 + 2R_2} = \left(1 - DC_{min}\right) \tag{2.20}$$

Figure 7 shows a further modification to the PWM brightness circuit to allow the minimum and maximum duty cycle limits to be programmed independently. Instead of a single common resistor, two resistors R_{2a} and R_{2b} are added in series with the potentiometer arms. R_{2a} sets the minimum charge time (minimum duty cycle), and R_{2b} sets the minimum discharge time (maximum duty cycle).
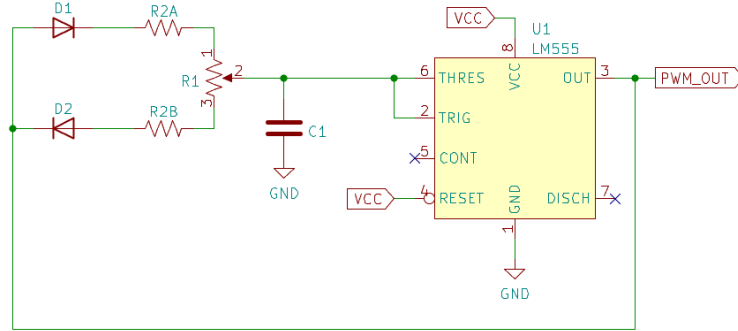

Figure 7: PWM brightness control circuit with independent minimum and maximum duty cycle limits.

For the circuit in Figure 7, the PWM frequency and duty cycle are given by

$$f_{out} = \frac{-1}{k\left(R_1 + R_{2a} + R_{2b}\right)C_1} \tag{2.21}$$

$$DC = \frac{bR_1 + R_{2a}}{R_1 + R_{2a} + R_{2b}} \tag{2.22}$$

3 Design Example

We will now design a PWM brightness circuit for a display that uses IN-12A Nixie tubes. Assume that the power supply voltage is 5 V, the IN-12A striking time is 80 µs. The system architect has requested that the brightness curve have no dead zones. The system architect has also specified that diodes D_1 and D_2 are 1N4148 small-signal diodes and R_1 is a single-turn potentiometer. For simplicity, we will use the circuit in Figure 6, which uses a single resistor to program the minimum and maximum PWM duty cycle.
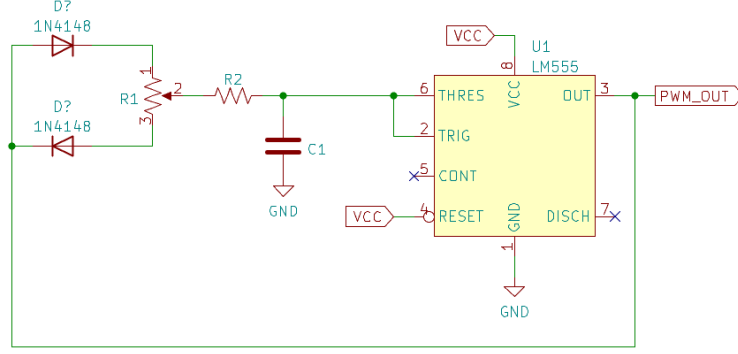
Figure 8: Initial PWM brightness circuit.

We begin by choosing a value for potentiometer R_1. Potentiometers are expensive and come in a smaller range of values than chip resistors, so we should select a common value for R_1 that is easy to source. Choosing $R_1 = 10$ kΩ is a good starting point.

Next, we choose our minimum and maximum duty cycle limits. We want to achieve the widest brightness range possible while still keeping the Nixie tube in a region of linear brightness control. We start by arbitrarily choosing the minimum duty cycle to be 0.1, or 10%. Since the circuit in Figure 6 produces symmetric duty cycle limits, the maximum duty cycle is therefore $(1 - 0.1) = 0.9$, or 90%. Is this bright enough? Nixie tube displays are very bright – often too bright for use in a dark room – so limiting the display to 90% brightness may actually be desirable. We then use equation 2.19 to calculate R_2 using our chosen value for R_1 and the minimum duty cycle limit of 0.1. Rearranging equation 2.19 and solving for R_2 yields:

$$R_2 = R_1 \left(\frac{0.1}{1 - 0.2} \right) = 0.125 \times 10 \text{ kΩ} = 1.25 \text{ kΩ} \tag{3.1}$$

Choose $R_2 = 1.24$ kΩ, the closest 1% standard resistor value.

We now have enough information to determine the PWM frequency. In order to prevent dead zones in the brightness curve, the minimum PWM pulse width must be greater than the Nixie tube striking time. The IN-12A has a striking time of 80 µs. For additional margin, we choose the minimum PWM pulse width to be 100 µs. Since we chose the minimum PWM duty cycle to be 0.1 (10%), the PWM frequency can be calculated using:

$$f_{PWM} = \frac{0.1}{100 \text{ µs}} = 1.0 \text{ kHz} \tag{3.2}$$

Is a 1 kHz PWM frequency acceptable? If the PWM frequency is too low, some users may notice flickering, especially when the display is moving in their peripheral vision. In general, PWM frequencies greater than 500 Hz seem to be tolerable by most users, so a 1 kHz PWM frequency should prevent visible flickering.

Another potential issue with PWM brightness control is that low PWM frequencies can sometimes produce audible buzzing in large Nixie tubes. This effect is caused by mechanical vibration of the electrodes, and larger Nixie tubes (with larger cathodes) are more susceptible than small Nixie tubes. The IN-12A is a physically small tube, so its mechanical self resonant frequency is likely high enough that a 1 kHz PWM frequency will not cause an audible hum. However, we don't have any concrete information about how to evaluate this risk, so will continue the design and make a note to revisit this issue later.

At this point in the design process, we need a value for the diode forward voltage V_F. When we derived our design equations, we assumed that V_F was constant. In reality, V_F is a logarithmic function of I_F, the current flowing through the forward-biased diode to charge or discharge C_1. Figure 9 is a plot of V_F versus I_F from the 1N4148 data sheet.
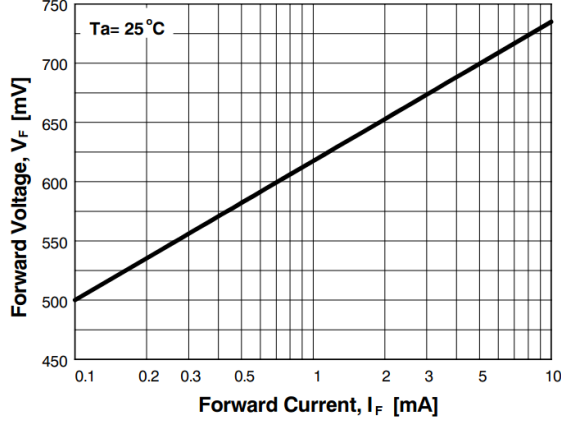
Figure 9: Plot of forward voltage V_F versus forward current I_F for a 1N4148 diode. Source: ONSEMI

Instead of attempting to derive an equation for V_F in terms of capacitor voltage or current, we can simply estimate the average value of V_F during the charging or discharging cycle. To do this, we start with an initial guess for V_F, estimate the average value of I_F during the charging or discharging cycle, then look up V_F from the curve in Figure 9. We then update our guess with the new value of V_F and repeat the process. We will converge on a reasonable estimate of V_F in one or two iterations.

For our initial guess, let's assume $V_F \approx 0.65V$. To obtain an average value of I_F, we consider the case when $b = 0.5$ (50% brightness). The average value of I_F is approximately

$$I_{F_{avg}} \approx \frac{0.5V_{CC} - V_F}{0.5R_1 + R_2} \tag{3.3}$$

Substituting our initial guess for V_F yields

$$I_{F_{avg}} \approx \frac{0.5V_{CC} - V_F}{0.5R_1 + R_2} \approx \frac{2.5 \text{ V} - 0.65 \text{ V}}{5 \text{ k}\Omega + 1.24 \text{ k}\Omega} \approx 300 \text{ µA} \tag{3.4}$$

We then use the plot of V_F versus I_F in the data sheet to find a new guess for V_F. From the data sheet, we see that a 1N4148 has $V_F \approx 0.56$ V for $I_F \approx 300$ µA. We iterate through this process one more time using the formula in Equation 3.3:

$$I_{F_{avg}} \approx \frac{0.5V_{CC} - V_F}{0.5R_1 + R_2} \approx \frac{2.5 \text{ V} - 0.56 \text{ V}}{5 \text{ k}\Omega + 1.24 \text{ k}\Omega} \approx 310 \text{ µA} \tag{3.5}$$

Returning to the data sheet, we see that V_F is still approximately 0.56 V for $I_F \approx 310$ µA – the graph is too small to resolve a 10 µA change. Iterating beyond this point won't improve our estimate. We assume $V_F \approx 0.56$ V and continue with the design process.

We are ready to calculate C_1 First, we use Equation 2.11 to solve for the constant k:

$$k = \ln\left(\frac{\frac{1}{3}V_{CC} - V_F}{\frac{2}{3}V_{CC} - V_F}\right) = \ln\left(\frac{1.107}{2.773}\right) = -0.919 \tag{3.6}$$

We then rearrange Equation 2.17 to solve for C_1:

$$C_1 = \frac{-1}{k\left(R_1 + 2R_2\right)f_{PWM}} = \frac{-1}{-0.919 \times 12.48 \text{ k}\Omega \times 1 \text{ kHz}} = 73.6 \text{ nF} \tag{3.7}$$

Choose $C_1 = 75$ nF, the closest 5% standard capacitor value.

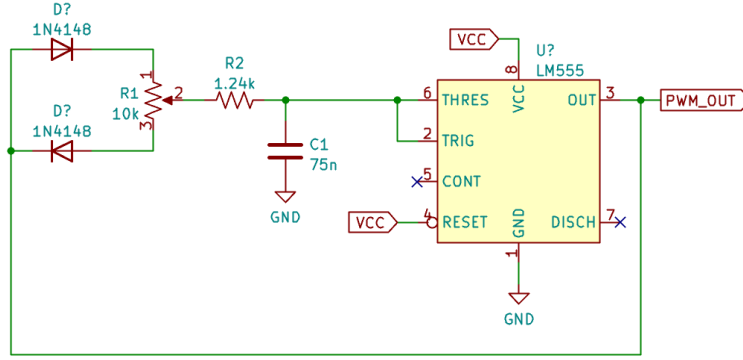Figure 10 is our first pass at designing the PWM brightness control circuit.

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Figure 10: First-pass PWM brightness control circuit design.

Figure 11 plots the simulated PWM output waveform for $b = 0$ (minimum brightness) and $b = 1$ maximum brightness. The output frequency is approximately 1.2 kHz, slightly higher than designed. Some frequency error was expected because our calculation for C_1 used an average value of V_F, and we can correct this by increasing C_1. Note that the PWM output is clean and square, and the circuit correctly limits the minimum and maximum duty cycles to 10% and 90%.
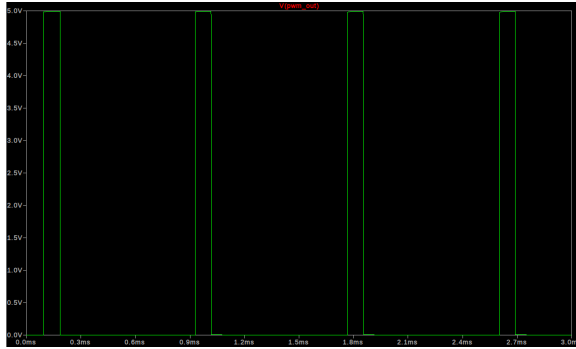
(a) 10% duty cycle (b = 0)
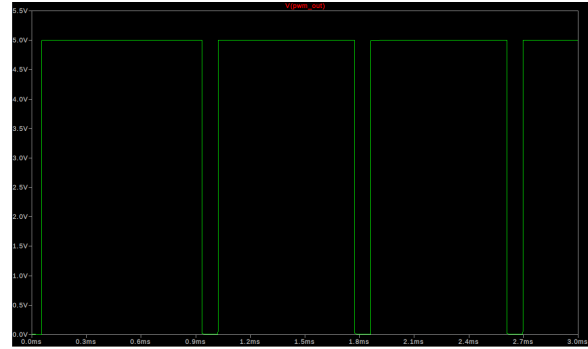
(b) 90% duty cycle (b = 1)

Figure 11: Simulated PWM output waveforms for the circuit in Figure 10.

Figure 12 is a plot of the simulated PWM frequency versus potentiometer position. We expected the PWM frequency to be constant for all brightness settings. In reality, however, the varies slightly with potentiometer position, with a local minimum at $b = 0.5$ and maxima at $b = 0$ and $b = 1$. This is also caused by a changing V_F. When $b = 0.5$, the resistance in the charging path and the discharging path is equal, and both diodes have the same forward current. As a result, V_F is the same for both diodes. However, as we move away from $b = 0.5$, the resistances in the charging path and discharging path become more and more unequal, and one of the diodes sees more current than the other. As a result, the diode in the high-current path will develop a larger forward voltage.
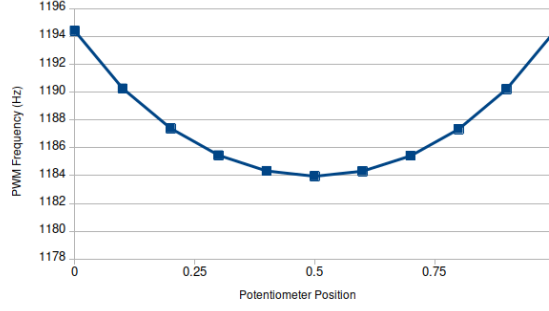
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Figure 12: Simulated PWM frequency versus potentiometer position for the circuit in Figure 10.

Figure 13 is the final PWM brightness control circuit. The total timing capacitance is increased from 82 nF to 88.8 nF (implemented using 82 nF and 6.8 nF in parallel) to compensate for the frequency shift due to incorrectly estimating V_F. The PWM output frequency is now 1.0 kHz at 50% duty cycle. We also add power supply decoupling capacitors C_2 and C_3, which should be appropriately sized for the power supply voltage and ripple frequency.
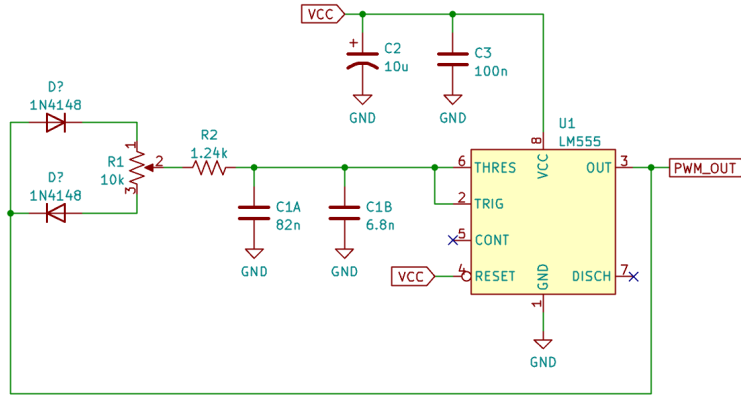

Figure 13: Simulated PWM frequency

Figure 14 plots the simulated PWM frequency and frequency error of the final PWM brightness circuit. Total frequency variation is less than 1% over the entire tuning range.

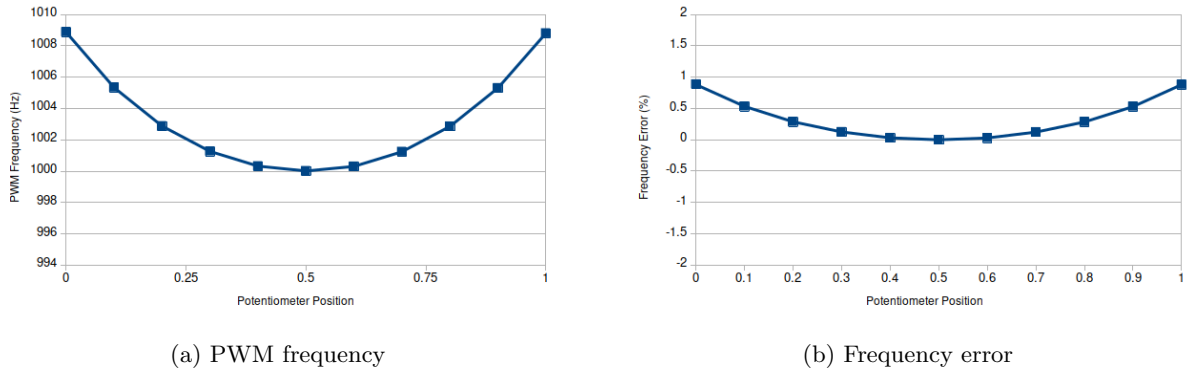(a) PWM frequency

(b) Frequency error

Figure 14: Simulated PWM frequency and frequency error for the circuit in Figure 13. Frequency error is less than 1% over the entire duty cycle range.

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Figure 15 plots the simulated PWM duty cycle and percent duty cycle error of the final PWM brightness circuit. The duty cycle curve increases very linearly with potentiometer position, resulting in a smooth, monotonic brightness curve with no dead zones. The minimum and maximum duty cycle are correctly limited to 10% and 90% to prevent dead zones caused by finite striking time, and the duty cycle error is less than ±2% over 80% of the tuning range - more than satisfactory for our application.
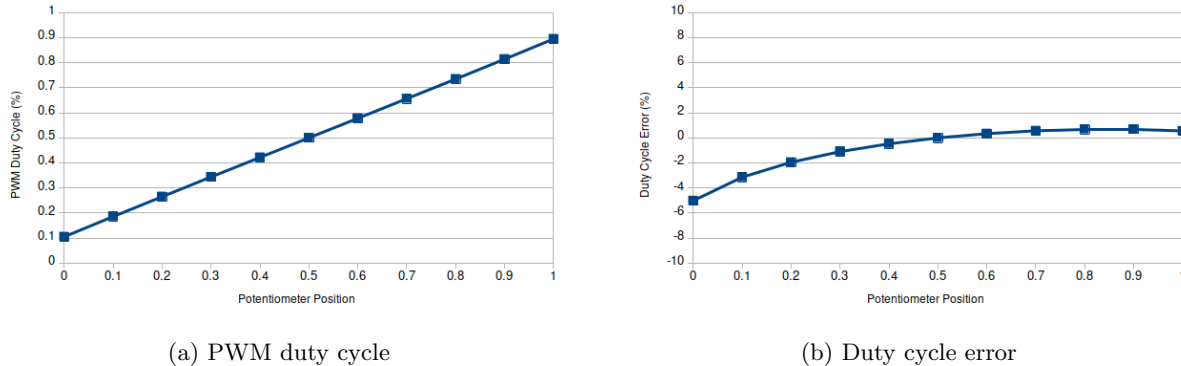

(a) PWM duty cycle

(b) Duty cycle error

Figure 15: Simulated PWM output frequency and percent frequency error for the circuit in Figure 13. Duty cycle error is generally less than ±2%

4   Summary

This analysis serves to prove that the PWM brightness circuit in Figure 13 is a viable candidate for use controlling a Nixie tube display. We analyzed the circuit, developed a set of design equations, picked component values, simulated the circuit, and identified the dominant sources of error in our design. PWM output frequency error is less than 1%, and PWM duty cycle error is generally less than 2%. However, there are some additional caveats to this analysis that warrant further investigation.

First, the circuit was simulated in LTSpice, an Analog Devices product. Due to model incompatibility and licensing issues, the LTSpice model of the NE555 (a Texas Instruments part) is an ideal macromodel, and does not include pin input capacitance or output driver on resistance (which is important, because the voltage at the 555 timer output changes depending on the amount of current it has to sink or source). If we were to build and test this circuit using the component values determined in Section 3, the measured duty cycle tuning range would be unchanged, but the measured PWM output frequency would be lower than the simulated PWM output frequency. In the final design, replace C_{1b} with a small trim capacitor to allow the PWM frequency to be adjusted after the PCB is assembled. Additionally, some 555 timer data sheets also suggest decoupling the CONT pin to ground with a 10 nF capacitor, which would help reduce noise and switching transients on the comparator threshold voltage nodes. I omitted this capacitor in my simulations because the ideal NE555 macromodel doesn't need it, but I recommend including it in real designs.

Second, this circuit was simulated with the output of the 555 timer driving an open circuit. As a result, the waveform is nice and square, and the rising and falling edge rates are very fast. In the final system, the output of the 555 timer will be loaded by an as-yet-undetermined number of 74xx series CMOS logic gates. Once the output load is determined, make sure to simulate the circuit again to check PWM frequency and output rise and fall times, and adjust the timing capacitor if needed.

Third, we have not examined how changes in temperature affect the performance of this circuit. Almost every component in this circuit has some sort of temperature dependence. Since this is a writing sample, a full breakdown of the temperature dependence of these circuits is outside the scope of this document; however, this circuit is intended to go in an alarm clock, which doesn't have to operate over the same temperature range as, say, a satellite. The extra margin we built in to the minimum duty cycle requirement is probably enough to absorb changes in PWM frequency and minimum pulse width caused by temperature and keep the brightness curve free of dead zones.