EX/MEM Data Memory
MEM/WB WriteBack

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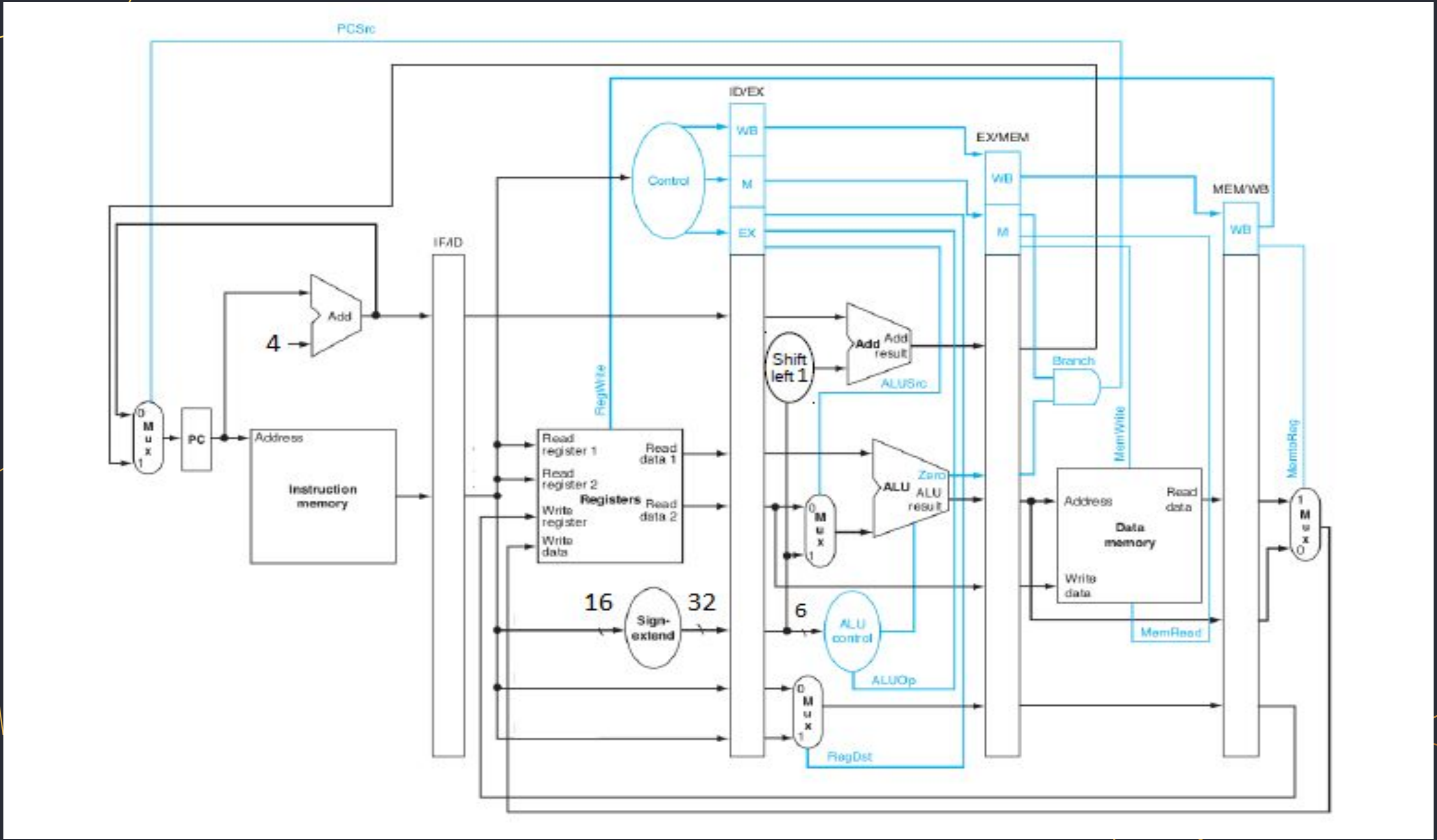
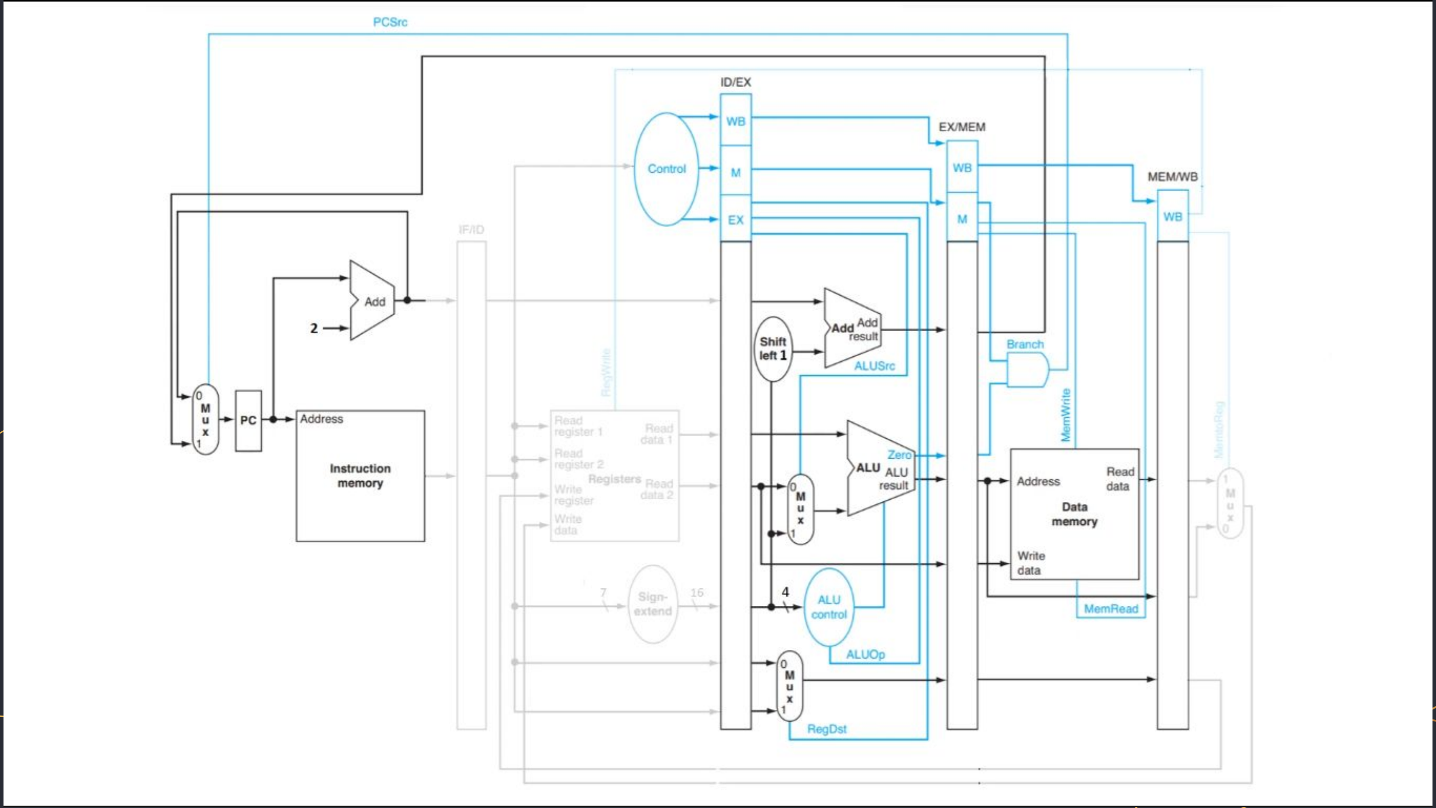
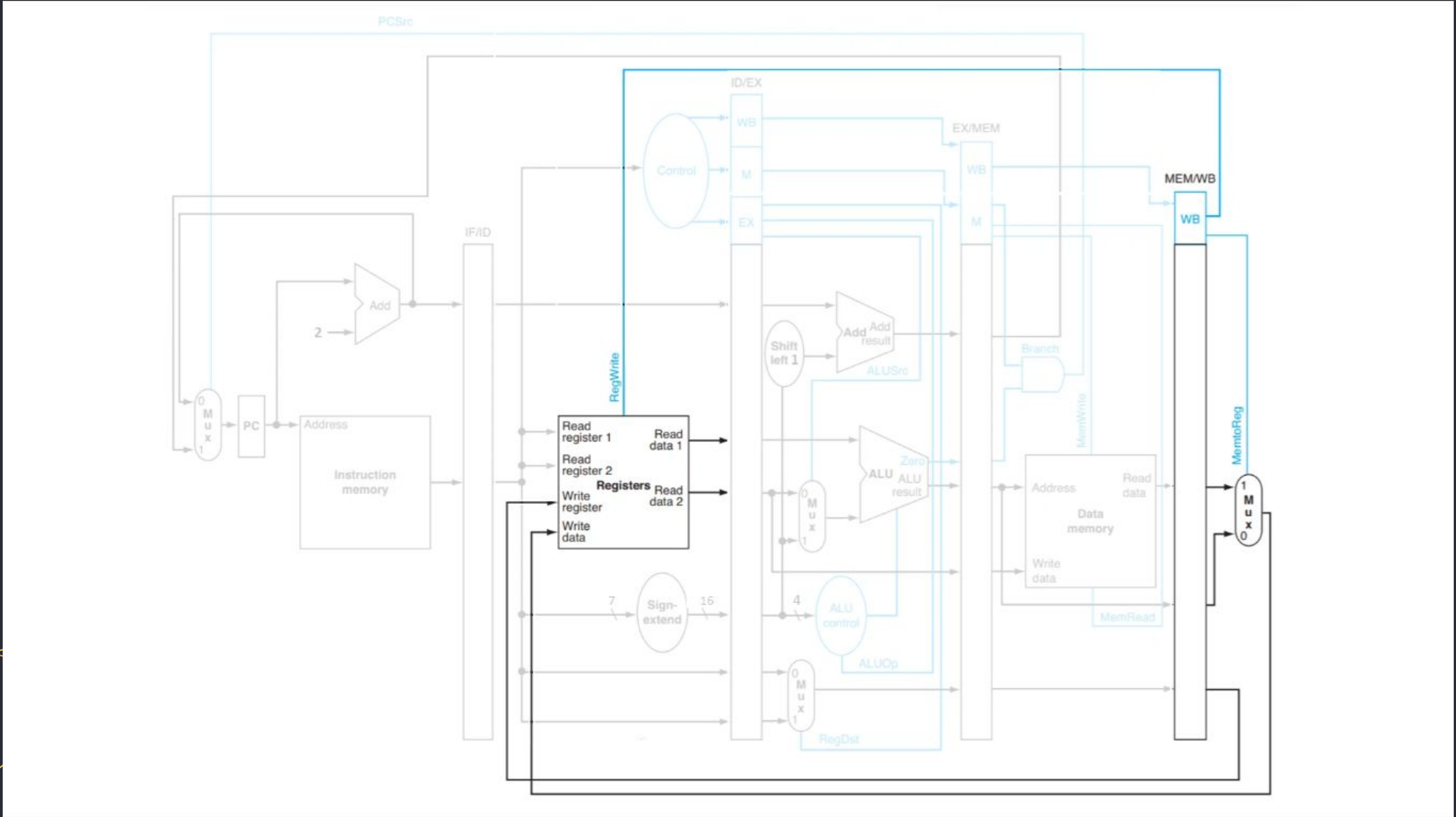
1. OVERVIEW OF MIPS PIPELINE



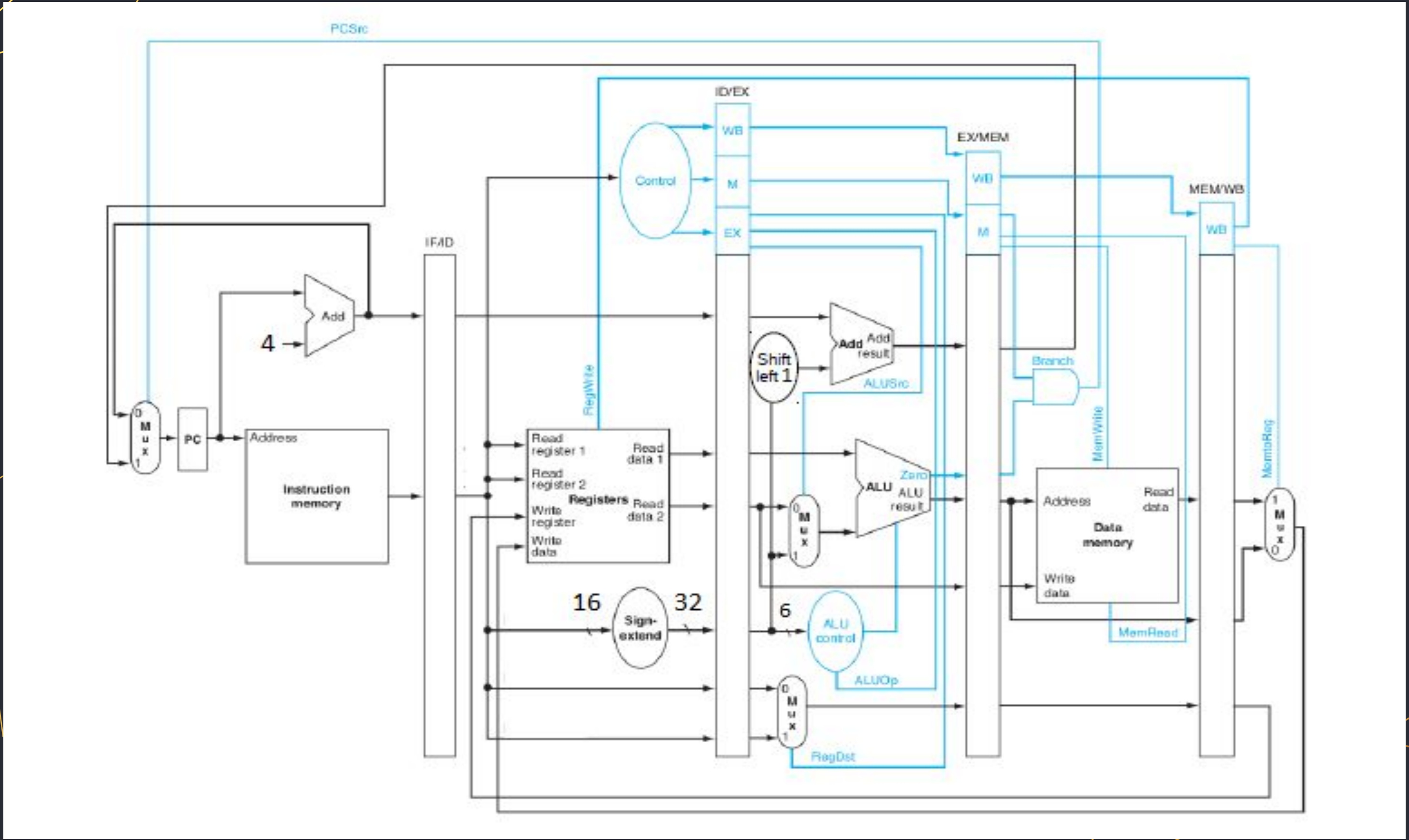
2. EX/MEM & Data Memory



3. MEM/WB & WriteBack



4. INTEGRATING ALL MODULES



5. INPUTS & OUTPUTS

Finally, it’s time to instantiate the modules and connect them together. Modules which need to be instantiated and connected are as follows:

EX/MEM Register:

- Inputs: clk(1), hit(1), branchTarget(32), zeroFlag(1), ALUResult(32), readData2(32), writeReg(5), MemRead(1), MemWrite(1), Branch(1), RegWrite(1), MemToReg(1)
- Outputs: branchTargetOut(32), zeroFlagOut(1), ALUResultOut(32), readData2Out(32), writeRegOut(5), MemReadOut(1), MemWriteOut(1), BranchOut(1), RegWriteOut(1), MemToRegOut(1), hitOut(1)

Data Memory::

- Inputs: clk(1), address(32), writeData(32), MemRead(1), MemWrite(1)
- Outputs: readData(32)

5. INPUTS & OUTPUTS (Cont'd)

MEM/WB Register:

- Inputs: clk(1), hit(1), readData(32), ALUResult(32), writeReg(5), RegWrite(1), MemtoReg(1)
- Outputs: hitOut(1), readDataOut(32), ALUResultOut(32), writeRegOut(5), RegWriteOut(1), MemtoRegOut(1)

WriteBack:

- Inputs: MemtoReg(1), readData(32), ALUResult(32)
- Outputs: writeData(32)