**Template Test Plan Document**

**Module Name/Internal ID: ASMD\_MULT**

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# **1.** **Revision**

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev** | **Comments** | **Date** | **Approval: Team/Date** |
| 1.0 | Initial Creation |  |  |

# **2.** **Required Documents**

|  |  |  |
| --- | --- | --- |
| **ID** | **Name** | **Revision** |
|  |  |  |

# **3.** **Supplemental Documents**

|  |  |  |
| --- | --- | --- |
| **ID** | **Name** | **Revision** |
| ASM | Algorithmic\_state\_machine (Wikipedia) | https://en.wikipedia.org/wiki/Algorithmic\_state\_machine |

# **4.** **Acronyms**

|  |  |
| --- | --- |
| **Abbreviation** | **Definition** |
| ASMD | Algorithmic state machine with DataPath |

**Table Of Contents**

**1**

**1**

**1**

**1**

**2**

**2**

**2**

**3**

**3**

**3**

# **5.** **Scope**

This document describes in detail, the test plan and test results for the ASMD\_MULT module.

# **6.** **Functional Verification**

ASMD\_MULT\_TP001: Verify that the module implements the interfaces described in the following table:

Verifies: ASMD\_MULT\_F001

Methods: visual inspection, compilation warnings, synthesis.

Results:

|  |  |  |  |
| --- | --- | --- | --- |
| **Port** | **Direction** | **Width** | **Description** |
| clk | input | 1’b1 | Input Clock Signal |
| rst | input | 1’b1 | Input Synchronous Reset Signal |
| start | Input | 1’b1 | Input module start signal |
| word0 | input | [word-length]’b1 | Input word 0 |
| word1 | input | [word-length]’b1 | Input word 1 |
| ready | Output | 1’b1 | Module ready output signal |
| produce | Output | [word-length\*2]’b1 | Module multiplication product output |

ASMD\_MULT\_TP002: Verify that module implements the parameters described in the following table:

Verifies: ASMD\_MULT\_F002

Methods: visual inspection, compilation warnings, synthesis.

Results:

|  |  |  |
| --- | --- | --- |
| **Name** | **Default Value** | **Description** |
| word\_length | 4 | Input word size in bits |

ASMD\_MULT\_TP003:

Verifies: ASMD\_MULT\_F003.

Methods: simulation:

1. Set baudrate to a standard rate

2. Drive reset to 1

3. Verify state goes to idle

4. Verify ready is 1

5. Verify product goes to 0 after next clock cycle

6. Verify multiplier goes to 0 after next clock cycle

7. Verify multiplicand goes to 0 after next clock cycle

Results:

ASMD\_MULT\_TP004:

Verifies: ASMD\_MULT\_\_F004.

Methods: simulation:

1. Set baudrate to a standard rate

2. Drive word0

3. Drive word1

4. Assert reset

5. Verify state goes to idle

6. Verify ready is 1

7. Verify product goes to 0 after next clock cycle

8. Verify multiplier goes to 0 after next clock cycle

9. Verify multiplicand goes to 0 after next clock cycle

10. Assert empty to value other than 1

11. Assert start

12. Verify ready is deasserted

13. Verify load\_words goes to 1

14. Deassert reset

Results: