Template Test Plan Document

Module Name/Internal ID: ASMD\_MULT

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# Revision

| Rev | Comments | Date | Approval: Team/Date |
| --- | --- | --- | --- |
| 1.0 | Initial Creation |  |  |

# Required Documents

|  |  |  |
| --- | --- | --- |
| ID | Name | Revision |
|  |  |  |

# Supplemental Documents

|  |  |  |
| --- | --- | --- |
| ID | Name | Revision |
| ASM | Algorithmic\_state\_machine (Wikipedia) | https://en.wikipedia.org/wiki/Algorithmic\_state\_machine |

# Acronyms

|  |  |
| --- | --- |
| Abbreviation | Definition |
| ASMD | Algorithmic state machine with DataPath |

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# Scope

This document describes in detail, the test plan and test results for the ASMD\_MULT module.

# Functional Verification

ASMD\_MULT\_TP001: Verify that the module implements the interfaces described in the following table:

Verifies: ASMD\_MULT\_F001

Methods: visual inspection, compilation warnings, synthesis.

Results: Ports visually verified and there were no reported errors with port connection during simulation.

|  |  |  |  |
| --- | --- | --- | --- |
| Port | Direction | Width | Description |
| clk | input | 1’b1 | Input Clock Signal |
| reset | input | 1’b1 | Input Synchronous Reset Signal |
| start | Input | 1’b1 | Input module start signal |
| word0 | input | [word-length]’b1 | Input word 0 |
| word1 | input | [word-length]’b1 | Input word 1 |
| ready | Output | 1’b1 | Module ready output signal |
| product | Output | [word-length\*2]’b1 | Module multiplication product output |

ASMD\_MULT\_TP002: Verify that module implements the parameters described in the following table:

Verifies: ASMD\_MULT\_F002

Methods: visual inspection, compilation warnings, synthesis.

Results: Parameter visually verified, there were no reported errors during simulation, and simulation verifies size.

|  |  |  |
| --- | --- | --- |
| Name | Default Value | Description |
| word\_length | 4 | Input word size in bits |

ASMD\_MULT\_TP003:

Verifies: ASMD\_MULT\_F003.

Methods: simulation:

* 1. Assert reset
  2. Verify ready is 1
  3. Verify product is 0 after next clock cycle

Results: Successful simulation with no reported errors.

ASMD\_MULT\_TP004:

Verifies: ASMD\_MULT\_F004.

Methods: simulation:

* 1. Assign word0
  2. Assign word1
  3. Assert reset
  4. Verify ready is 1
  5. Assert start
  6. De-assert start
  7. Verify correct product

Results: Successful simulation with no reported errors.