Template Test Plan Document

Module Name/Internal ID: ASMD\_MULT

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# Revision

| Rev | Comments | Date | Approval: Team/Date |
| --- | --- | --- | --- |
| 1.0 | Initial Creation | 9/21/2023 |  |

# Required Documents

| ID | Name | Revision |
| --- | --- | --- |
| LGCR\_ASMD\_MULT | ASMD\_MUTIPLIER Logic Requirements Document | 1.0 |

# Supplemental Documents

| ID | Name | Revision |
| --- | --- | --- |
| ASM | Algorithm\_state\_machine (Wikipedia) | https://en.wikipedia.org/wiki/Algorithmic\_state\_machine |

# Acronyms

| Abbreviation | Definition |
| --- | --- |
| ASMD | Algorithmic State Machine with DataPath |

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# Scope

This document describes in detail, the test plan and test results for the XXX module.

# Functional Verification

ASMD\_MULT\_TP001: Verify that the module implements the interfaces described in the following table:

Verifies: ASMD\_MULT\_F001

Methods: visual inspection, compilation warnings, synthesis.

Results:

| Port | Direction | Width | Description |
| --- | --- | --- | --- |
| clk | input | 1’b1 | Input Clock Signal |
| rst | input | 1’b1 | Input Synchronous Reset Signal |
| start | Input | 1’b1 | Input module start signal |
| word0 | input | [word-lenght]’b1 | Input word 0 |
| word1 | input | [word-lenght]’b1 | Input word 1 |
| ready | Output | 1’b1 | Module ready output signal |
| produce | Output | [word-lenght\*2]’b1 | Module multiplication product output |

ASMD\_MULT\_TP002: Verify that module implements the parameters described in the following table:

Verifies: ASMD\_MULT\_F002

Methods: visual inspection, compilation warnings, synthesis.

Results:

| Name | Default Value | Description |
| --- | --- | --- |
| word\_length | 4 | Input word size in bits |

ASMD\_MULT \_TP003: Verify that the module implements the following:

Upon assertion of reset:

* assert ready.
* Assign product to zeros.

Verifies: ASMD\_MULT \_F003

Methods: compilation warnings, simulation.

Results:

ASMD\_MULT \_TP004: Verify that the module implements the following:

Upon assertion of start:

* deassert ready.
* Calculate the product of word0 \* word1.
* Assert ready only when the multiplication computation is complete.
* Output the multiplication computation on the product output port.

Verifies: ASMD\_MULT \_F004.

Methods: compilation warnings, simulation.

Results: