**MORGAN STATE UNIVERSITY**

**DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING**

**EEGR471 Design of Integrated Circuits**

Fall 2023

Credits: 3

COURSE SYLLABUS

**Instructor:** Idris Somoye

**Office:** MEB, RM 244

**Telephone No.**

**Email Address:** idris.somoye@morgan.edu

**Office Hours:**

**Text Book**

[1] SystemVerilog for Verification: A Guide to Learning the Testbench Language Features 3rd ed. 2012 Edition

[2] Digital System Test and Testable Design: Using HDL Models and Architectures 2011th Edition, Kindle Edition

Other reference material as provided via Canvas

**Catalog Description**

This course will provide practical knowledge of common faults in digital systems throughout the design process from conceptual to silicon, and how to effectively reduce and/or mitigate those faults. It includes techniques used in digital systems verification and validation such as, logic simulation and testbench creation, fault models, test pattern generation, design for testability, and built-in self-test.

**Prerequisite:** EEGR 211, EEGR 409, EEGR 463

**Course Requirements**

This course is an elective course for all engineering undergraduate students, especially those with computer engineering, digital design, embedded systems, and hardware/software co-design interest. This course relates heavily to the EEGR409/463. In conjunction with the other courses, this course will help the student develop a breadth of understanding in integrated circuits. Students are expected to prepare and participate in the lectures. Lectures will selectively cover material in the text and will draw from other reference sources.

Homework assignments will consist of selected problems from the text and/or other sources. As this topic has a large applied element, class projects will be an important element of the learning experience for this topic. These projects will be accomplished using python and C programming languages, as well as SystemVerilog HDL language. Projects will represent a significant portion of the grade. Quizzes will be announced or unannounced, in class or online. One examination will be given during the course. A comprehensive final project will be assigned in lieu of the final exam. Students will need to propose the final project and get the instructor’s approval. Week 7 of the course is dedicated for the final project proposals in the class. Depending on the scope of the project, working in a group is possible, given that the tasks of individuals are well defined in the project proposal. The final project will be presented in the last session of the class.

**Course Objectives**

Upon successful completion of the course, the student should be able to generate and execute on, an effective test-plan for a digital logic design. Learning outcomes include design specification review, RTL simulation & verification, post-synthesis verification, and post manufacturing testing.

Prefabrication:

**CO1:** Gain insight into the economics of testing and verification, including the cost of ASICs and the consequences of under-verified designs.

**CO2:** Develop and interpret in-depth Integrated circuit requirement and test plans, including proper engineering judgment in tradeoffs between expected coverage and verification timelines.

**CO3:** Create a standard methodology simulation testbench utilizing layered testing and exploratory frameworks such as cocotb, in order to verify complex multi-module systems

Post Fabrication

**CO4**: Demonstrate an understanding of DFT principles, including common fault types in manufacturing, how faults manifest in physical devices, methods of detecting faults, and ways to mitigate certain faults.

**CO5**: Utilize Design for testability techniques such as scan-chains and JTAG to verify IC functionality.

**Schedule**

| **Course Schedule/Session Format** | | |
| --- | --- | --- |
| **Content** | **Date** | **Topic** |
| Module 1 | 8/24/2023 | **Introduction**  Introduction to large scale logic design and verification. |
| Module 2 | 08/31/2023 | **Requirements and Test Plans** |
| Module 3 | 9/7/2023 | **Logic Simulation** |
| Module 4 | 9/14/2023 | **TestBenches** |
| Module 5 | 9/21/2023 | **Frameworks** |
| Module 6 | 9/28/2023 | **Layers** |

| Module 7 | 10/5/2023 | **Object Oriented Programming for Logic Simulation** |
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| Module 8  Mid term exam | 10/12/2023 | Exam |
|  | | |
| Module 9 | 10/19/2023 | **Design-Under-Test(DUT) & Testers** |
| Module 10 | 10/26/2023 | **Faults & Fault Modeling** |
| Module 11 | 10/29/2023 | **DFT, SCAN** |
| Module 12 | 11/2/2023 | **JTAG 1** |
| Module 13 | 11/9/2023 | **JTAG 2** |
| Module 14 | 11/16/2023 | Final project presentations and discussion |

**Class Policy**:

1. Take home assignments are due at the beginning of the class one-week after the

assignment is given. HAVE a cover page with your name on your homework

preferably on the standard 8½”X 11” letter size papers. All out-of-the class

assignments must be computer generated printouts. Random assigned

problems will be graded. A sample of cover page is attached with this handout.

2. Grades will be provided for every assignments and weighted accumulation of all

grades during the semester will determine the final letter grade.

3. Quizzes will be given randomly and unannounced. Lowest quiz grade MAY be

dropped when calculating the final grade.

4. NO makeup examination, assignment, and quiz.

5. It is students’ RESPONSIBILITY to maintain the schedule of assignments and

covered materials.

6. Students are REQUIRED to attend every class ON TIME and attendance will be

taken at the beginning of class and a percentage of meeting grades will be based

on the attendance and punctuality. Two absences without acceptable excuses

will exclude the student from “A” grade. Perfect attendance will bring in a positive

impact on the consideration of a student’s final grade.

7. Students are expected to follow academic honesty and ethics. Adapting any

unfair means during examinations, home-works and quizzes will result in an F

grade for the semester.(See Academic Dishonesty Policy)

8. Individual examination grades MAY be adjusted with median transformation

method. Final letter grade MAY be adjusted on the portfolio grading system.

9. An incomplete and/or wrong answer to a question receives “ZERO” for that

problem. A partial credit MAY be given based on the professional judgment of the

grader, and is NOT negotiable.

10. Students are expected to understand and abide by the code of student conduct

and disciplinary procedures of Morgan State University policy including the

amendment approved in 2000, 2002, 2003, and 2017.

**Academic Dishonesty Policy**

Academic dishonesty is not valued in the School of Engineering. Under no

circumstance(s) shall a student represent the original words or ideas of others as

your own. If any words or ideas used in a class posting or assignment submission

do not represent your original words or ideas, then the student committed

academic fraud. Therefore, all students are expected to conform to all University

standards of conduct in accordance with the Policy on Academic Dishonesty as

per the University Catalog. All work presented on examinations and assignments

must be of your own (or your team if one is allowed). Furthermore, cell phone

usage is prohibited during class. Smart electronic devices (i.e., phones, tablets,

laptops, MacBooks, etc.) will not be allowed for use on any quiz or exam. Any

deviation from this policy will be regarded as academic dishonesty 1 , including but

not limited to cheating, bribery, misrepresentation, conspiracy, fabrication,

collusion, duplicate submission, academic misconduct, improper

computer/calculator use, improper online/hybrid course use, disruptive behavior,

plagiarism, deception 2 , and professorial misconduct. 2 Consequently, the student

will receive a “F” for the exam, assignment and/or final grade as deemed

appropriate for any act(s) of academic dishonesty. The student has the right to

appeal the action taken by submitting in writing to the School of Engineering

Judicial Committee to request for a hearing on the academic fraud allegation(s)

within the same semester by emailing soesss@morgan.edu.

**Grading**

**Homework and Lab assignments 50%**

**Midterm Exam 20%**

**Projects 30%**

**Grades: A (90-100%) , B (80-89%), C(70-79%), D (60-69%), F (0-59%)**

**NOTE: Any material submitted that is substantially copied from other students without citation or from the Internet will receive a zero grade.**

**Notes: Expectations and Requirements**

1. Students are expected to log on to Bb 3 times a week.

2. Students are expected to actively attend and engage in class.

3. Homework and other assignments are due by midnight of the given due date. Late penalty will be deducted for late submission.

4. A programming assignment might be given in lieu of a quiz.

5. Programming assignments are expected in the following format.

Project

docs

src

tb

6. Academic misconduct or cheating during an exam will result in an F grade for the course.

| Department of Electrical and Computer EngineeringEEGR 471.001Design of Integrated CircuitsFall, 2023Assignment # 1 Subject: Logic Requirements  (Design Logic Test Plan – TP) John M. Doe Date: August, 22, 2023 |
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