Objectives: Students will learn common faults in digital systems throughout the design process from conceptual to silicon, and how to effectively reduce and/or mitigate those faults. We will cover the techniques used in digital systems verification and validation, from fault models, logic simulation and testbench creation, test pattern generation, design for testability, and built-in self-test.

Upon successful completion of the course, the student should be able to:

1. Create an effective test-plan for a digital design which includes design specification review, RTL simulation verification, post-synthesis verification, and post manufacturing testing.
   1. Prefab
      1. Develop in depth Integrated circuit testplans.
      2. Create a standard methodology simulation testbench.
   2. Post-fab
      1. Demonstrate an understanding of scan-chains and other DFT principles.
      2. Utilize Design for testability techniques to verify IC functionality.