EEGR 471: Digital Systems Testing

Objectives: Students will learn common faults in digital systems throughout the design process from conceptual to silicon, and how to effectively reduce and/or mitigate those faults. We will cover the techniques used in digital systems verification and validation such as, logic simulation and testbench creation, fault models, test pattern generation, design for testability, and built-in self-test.

Upon successful completion of the course, the student should be able to generate and execute on, an effective test-plan for a digital design, which includes design specification review, RTL simulation verification, post-synthesis verification, and post manufacturing testing.

* 1. Prefab
     1. Develop and interprete in-depth Integrated circuit test plans.
     2. Create a standard methodology simulation testbench.
  2. Post-fab
     1. Demonstrate an understanding of DFT principles.
     2. Utilize Design for testability techniques to verify IC functionality.

Prerequisites: Digital Logic Design, HDL/RTL course, ASIC

Course Breakdown

* Weeks 1 - 6: Verification/Simulation
  + Week 1: (Digital Design/RTL Background). V&V background
    - Lab 1: terosHDL install, RTL schematic view.
      * testbench templates: verilator/Verilog/cocotob
  + Week 2: (V&V) overview. Simulation Introduction
    - Verilator, Pyverilog, Icarus Verilog
    - Simulation Algorithms
    - Lab2: Implement simple cycle/event-based simulator.
  + Week 3 and 4: Object Oriented Verification code
    - SystemVerilog
    - Lab 3: Create and execute test plan.
      * create test plan for one of the RV32I core modules.
      * create class based testbench in language of choice that.
  + Week 5 & 6: Post Synthesis and formal Verification
    - Post Synthesis Simulation & Functional Equivalency
    - Emulation
    - Lab 4: Post Synthesis:
      * Generate Netlist with Yosys.
      * Simulate generated netlist with testbench from lab 3.
      * Perform functional equivalence check on RTL vs Netlist.
* Weeks 7-16: Hardware Faults
  + Week 7,8: Fault Modeling, Detection and Mitigation
  + Week 9: Test Vectors
    - ATPGs
    - <https://github.com/AUCOHL/Fault>
  + Week 10 and 11: Scan Chain Overview & Insertion/ DFT
  + Week 12: JTAG
    - XJLink2 — USB JTAG controller
    - https://www.xjtag.com/products/hardware/xjlink-xjlink2-controller/
  + Week 13-16:
    - Lab work with XJLink2 — USB JTAG controller